THE pcb design MAGAZINE

April 2015

an I·Connect007 publication

The Future of Nickel in Nickel/Palladium/Gold Final Finishes — p.18

Plus:

Hunter's Two Newest CID Recipients Discuss Certification — p.46

Effective Decoupling Radius — p.52

SURFACE FINISHES

Looking Below the Surface

IPC Plating Sub-committee 4-14: Surface Finish Specifications

by George Milad, page 10

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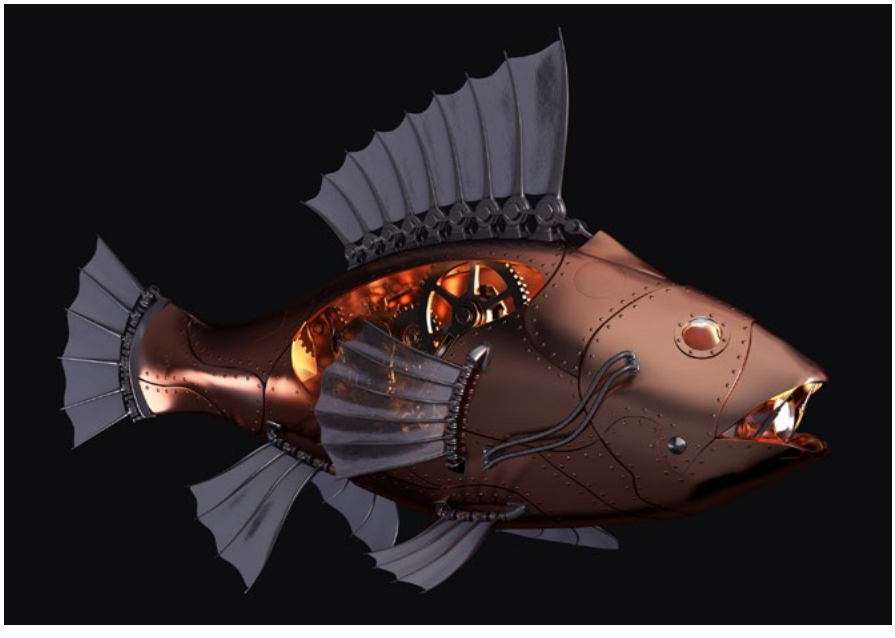
This Issue: SURFACE FINISHES

FEATURED CONTENT

For years, hot air solder leveling was the predominant surface finish in the PCB industry. But now, there's a veritable alphabet soup of available surface finishes, and each has its own advantages and disadvantages. This month, we focus on the latest in PCB surface finishes, with articles from George Milad and Rick Nichols, as well as columns and articles from our regular contributors.

10 Looking Below the Surface — IPC Plating Sub-committee 4-14: Surface Finish Specifications
by George Milad



18 The Future of Nickel in Nickel/Palladium/Gold Final Finishes
by Rick Nichols

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Df @ 10 GHz	0.0028 - 0.0036	0.0028, 0.0031 & 0.0034	0.0031*	0.0030*	0.0017
CTE Z-axis (50 to 260°C)	2.90%	2.80%	2.80%	2.90%	2.90%
T-260 & T-288	>60	>60	>60	>60	>60
Halogen free	No	No	No	Yes	No
VLP-2 (2 micron Rz copper)	Available	Available	Available	Standard	Standard
Stable Dk & Df over the temperature range	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C	-40°C to +140°C
Optimized global constructions for Pb-free assembly	Yes	Yes	Yes	Yes	Yes
Compatible with other Isola products for hybrid designs	For use in double-sided applications	Yes	Yes	Yes	Yes
Low PIM < -155 dBc	Yes	Yes	Yes	Yes	Yes

* Dk & Df are dependent on resin content NOTE: Dk/Df is at one resin %. Please refer to the Isola website for a complete list of Dk/Df values. The data, while believed to be accurate & based on analytical methods considered to be reliable, is for information purposes only. Any sales of these products will be governed by the terms & conditions of the agreement under which they are sold.

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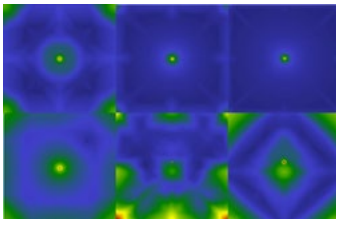
CONTENTS

ARTICLES

46 Hunter's Two Newest CID Recipients Discuss Certification
by Kelly Dack

52 Effective Decoupling Radius
by Kirk Fabbri

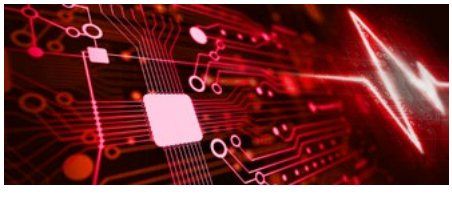


COLUMNS

8 Moore's Law Turns 50
by Andy Shaughnessy

30 Learning the Curve
by Barry Olney

36 RF Power Capabilities of High-Frequency PCBs
by John Coonrod



42 The Utility Belt
by Tim Haag

VIDEO INTERVIEW

45 Altium Talks 3D Flex Packaging Design

SHORTS

16 Removing Risk to Unleash the Full Potential of Nanomaterials

35 Breakthrough in Thermoelectric Materials

61 Driverless Cars to Renovate Automotive Industry

NEWS HIGHLIGHTS

40 PCB007

50 Mil/Aero007

62 PCBDesign007

EXTRAS

64 Events Calendar

65 Advertiser Index & Masthead

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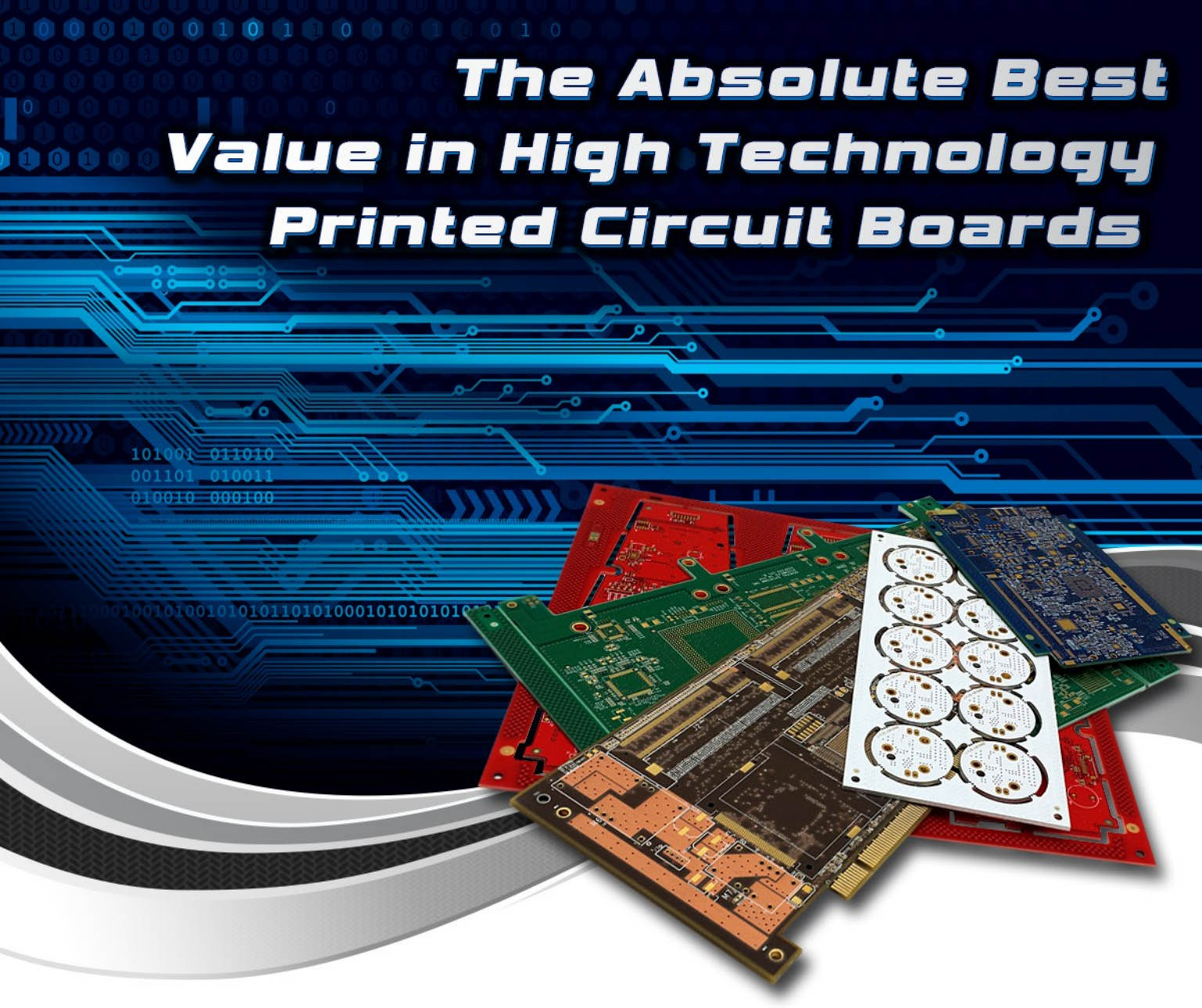

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THE SHAUGHNESSY REPORT

Moore's Law Turns 50

by Andy Shaughnessy
I-CONNECT007

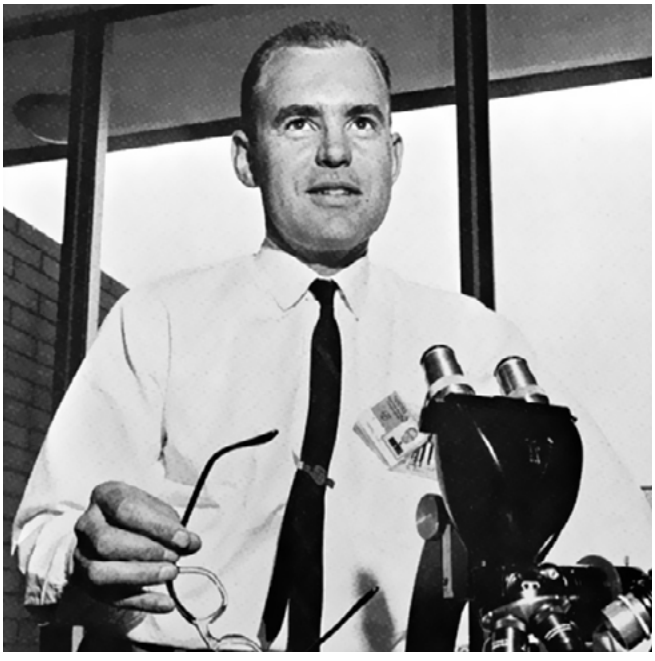
Let's all pause to wish Moore's Law a very happy 50th birthday, even as the vultures begin to circle overhead.

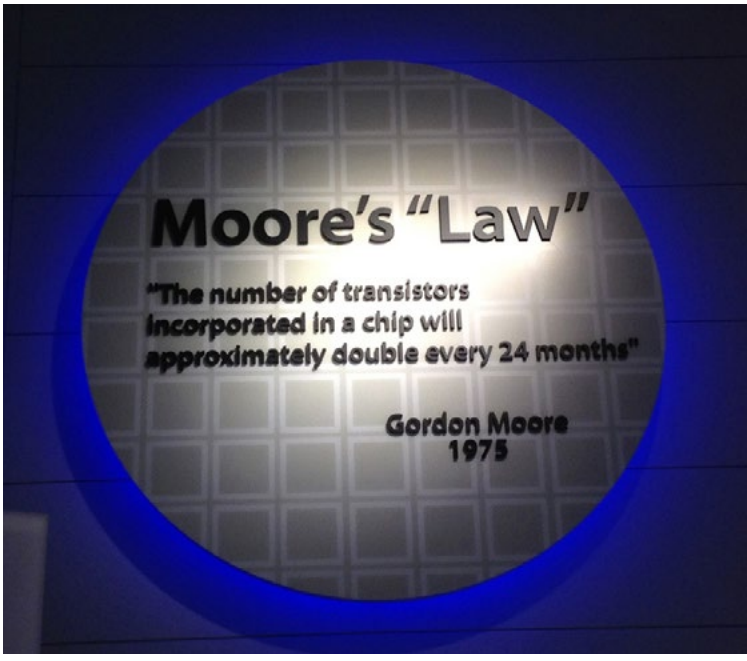
Fifty years ago, Dr. Moore was director of R&D at Fairchild Semiconductor, and Electronics Magazine asked him to make some predictions about the future of the semiconductor industry. On April 19, 1965, the magazine published his earthshaking article outlining what became known as Moore's Law.

In the article, titled "Cramming More Components onto Integrated Circuits," Moore posited that the number of components in a dense integrated circuit had doubled every year, and would continue at that rate for at least 10 years. Before he knew it, electronics companies around the globe were using Moore's Law for their technology roadmaps. It has become more than a target; it is one of the predominant driving forces in the electronics industry. In 1975, Moore amended his prediction from one year to approximately every two years. (Interestingly, Moore didn't come up with the term Moore's Law; that honor belongs to Caltech's Carver Mead.)

Moore went on to be a co-founder and CEO of Intel Corporation. He's had a great life; he and his wife created the Gordon and Betty Moore Foundation with a $5 billion endowment. In 2001, the couple donated $600 million to Caltech, the biggest single gift ever given to a college, and in 2007 they gave $200 million to Caltech and the University of California to fund the Thirty Meter Telescope, to be built on Mauna Kae in Hawaii.

But all this time, Moore knew his law would hit a manufacturing wall. He once said, "It can't





continue forever. The nature of exponentials is that you push them out and eventually disaster happens."

Now, as Moore's Law celebrates the big Five-O, technologists are predicting that the law will expire in the next decade. Chip companies are spending billions trying to identify the next material, or a new way to make chips.

What's After Silicon?

A handful of new technologies show promise. Silicon nanophotonics involves replacing the electrons on an IC with light particles, and we know that light can transmit data through fiberoptic cables. Why not use light to move data on a chip? Talk about energy-efficient. Sure, nanophotonics are years away, but there's plenty of ongoing research in photonics.

IBM is investing in carbon nanotubes (CNT), and plans to have a CNT chip commercially available by 2020. CNTs have been around for over a decade. They exhibit amazing thermal conductivity, but creating them has been prohibitively expensive. Let's see how IBM brings down the price point on CNT technology.

IBM is also working with synaptic computing. Last year, the company revealed TrueNorth, the world's first neurosynaptic computer chip, which is designed to operate much like the human brain. TrueNorth features 5.4 billion transistors, the most that Big Blue has ever fit onto one chip. Sure, the human brain has 100 billion neurons, but that's a good first step.

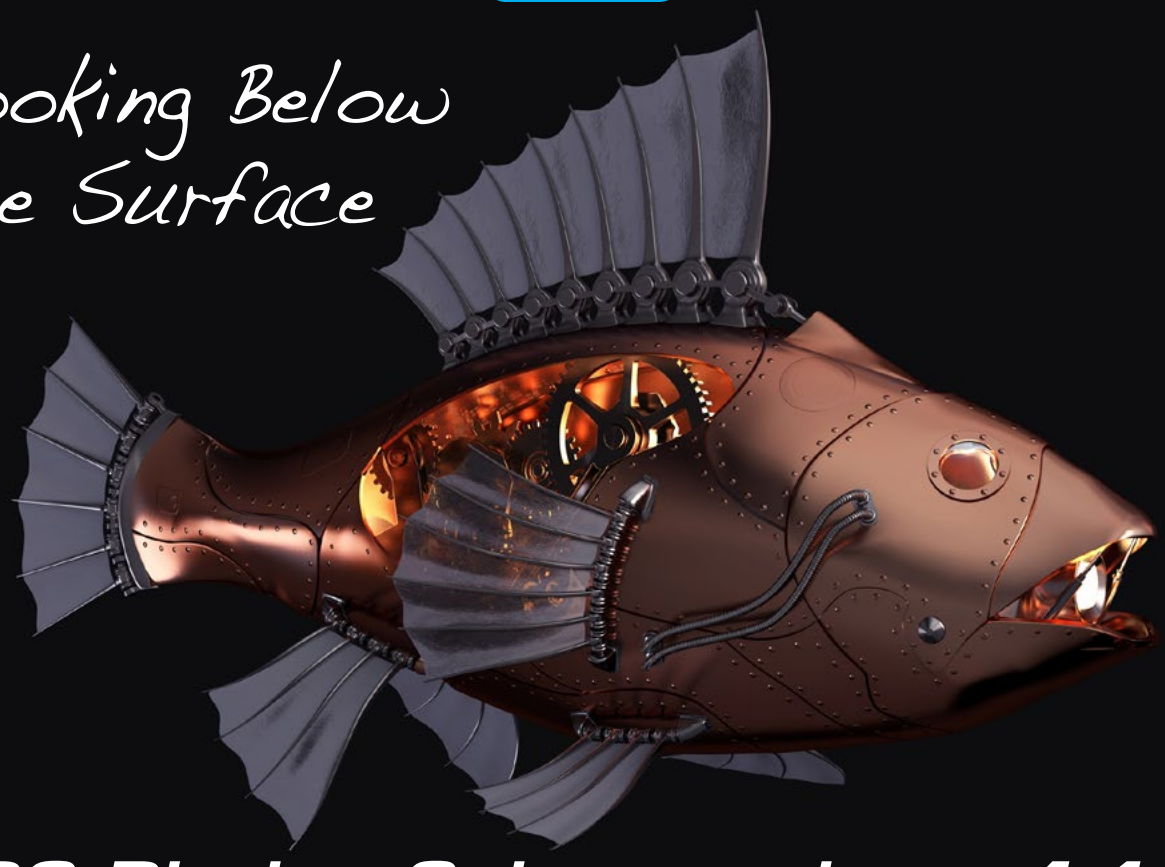
But my favorite is quantum computing, which is still in the early experimental stages. Quantum computation encodes data into quantum bits (qubits), which can exist in "superpositions," or more than one state at once. This means that a qubit can represent a one and a zero at the same time, which is pretty cool.

All of these are in their infancy, and years from being commercially available. The big trick will be to create materials and processes that fit into the manufacturing flow of today, as seamlessly as possible. Good luck with that.

In the end, the electronics industry will have to make some adjustments when Moore's Law reaches the end of its life. But it won't be the end of the world that some of the chip companies imagine it to be. So, let's sing a round of "Happy Birthday" to Moore's Law and hold off calling hospice just yet. **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 15 years. He can be reached by clicking here.

Looking Below the Surface



IPC Plating Sub-committee 4-14: Surface Finish Specifications

by George Milad
UYEMURA
CO-CHAIR, IPC PLATING SUB-COMMITTEE 4-14

This article was previously published in the February 2015 edition of The PCB Magazine.

IPC specifications are reference documents to be called out by designers and OEMs. Designers may take exception with one or more items in the specification to ensure that the product meets the requirements of its intended use. The acronym AAUBUS (as agreed upon between user and supplier) is part of any specification.

Specifications are consensus documents. They are agreed upon by a panel of interested industry participants composed of suppliers, manufacturers, assembly houses (CMs) and end users. The IPC Plating Sub-committee 4-14 is no exception.

When there is consensus, the committee documents it in a specification. In cases where no consensus is readily arrived at, the committee undergoes its own testing in what is commonly referred to as a round-robin (RR) study. In a RR investigation, an agreed upon test vehicle (TV) is designed and manufactured. TVs are then sent around to the different suppliers who deposit the agreed upon thicknesses to be investigated. The TVs are collected and the deposit thicknesses are verified and documented. The TVs are then coded. The TVs are sent around again to the different testing sites that test for the desired attribute like soldering, contacting and wire bonding capabilities of different finish thicknesses. The data is then collected, sorted out and documented. At this point, a new attempt at consensus is made and upon arrival, the thickness specification is set.

A draft is prepared after consensus is complete. The draft is then posted for peer review. Any IPC member can review the document and suggest technical or editorial changes. All comments are then reviewed and all issues resolved

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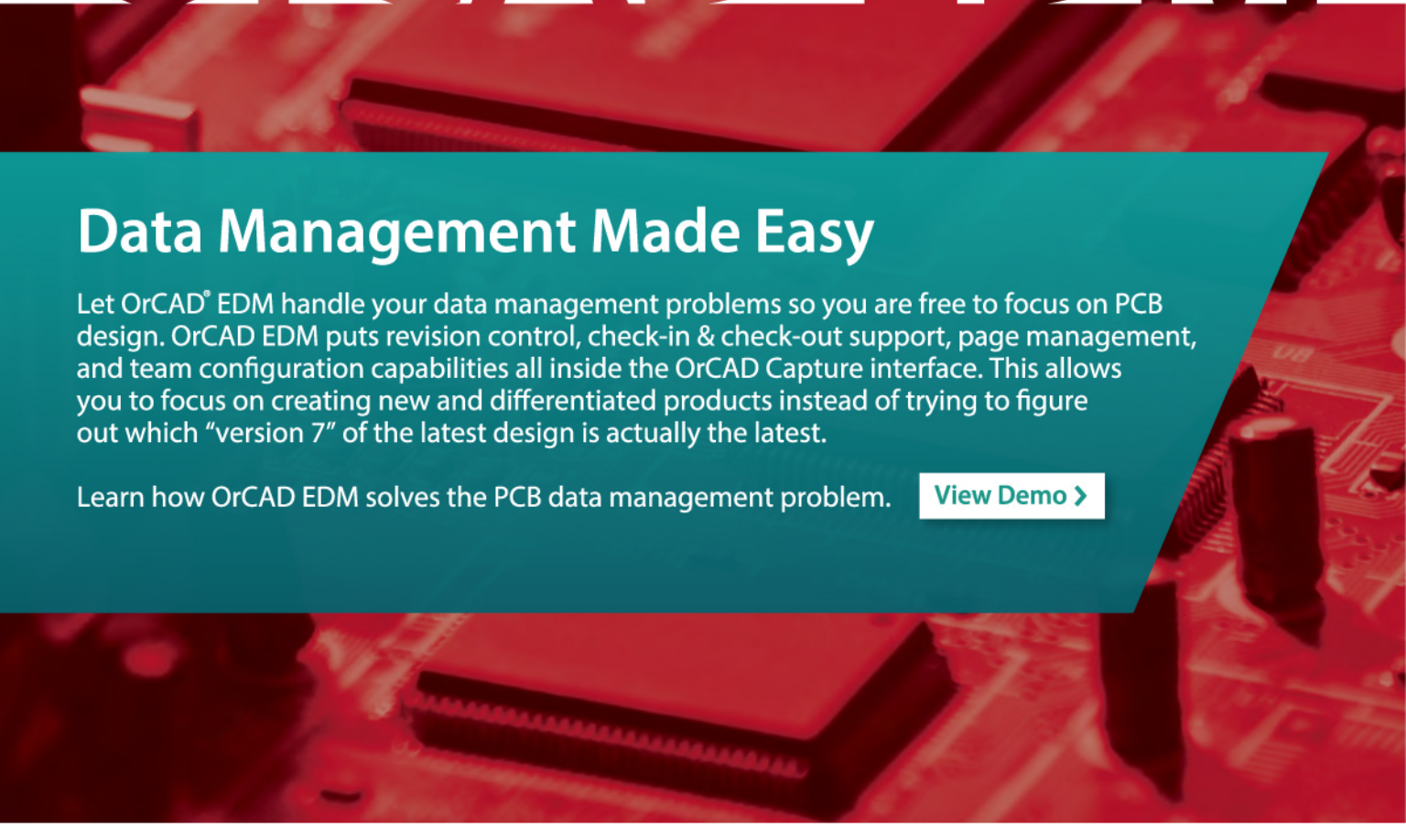

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before the final draft is issued. At this time the IPC takes on the task of publishing the document in its final format.

The IPC Plating Sub-committee 4-14 has been active since 2001. It is co-chaired by myself and Gerard O'Brien of ST and S Group. The IPC liaison is Tom Newton. The sub-committee has an extensive member list composed of OEMs, contract assemblers, board manufacturers, chemical suppliers, as well as labs and consultants.

The committee operates through one-hour, bi-weekly conference calls. Calls are held every other Wednesday at 11:00 a.m., EST, and everyone is welcome to participate. A notification e-mail is sent out before each conference call. All decisions pertaining to initiation and follow up on round-robin studies, evaluation of results, draft review, etc., are made during these calls, by those in attendance. The call minutes are documented and circulated.

> **ENIG is a coplanar surface finish composed of a nickel layer capped with a thin layer of gold. The ENIG surface finish is solderable, aluminum wire bondable, and an excellent contacting surface, with a minimum shelf life of 12 months under standard storage conditions.**

Since its inception, the IPC Plating Sub-committee 4-14 has issued the following:

- IPC-4552 ENIG Specification 2002
- IPC-4553 Immersion Silver specification 2005
- IPC-4554 Immersion Tin Specification 2007
- IPC-4553A Revised Immersion Silver 2009
- IPC-4554 Amended Tin Specification 2011
- IPC-4552 Amended ENIG Specification 2012
- IPC-4556 ENEPIG Specification 2013

Following is a discussion of each of the above:

Electroless Nickel/Immersion Gold (ENIG) IPC-4552, 2002

ENIG is a coplanar surface finish composed of a nickel layer capped with a thin layer of gold. The ENIG surface finish is solderable, aluminum wire bondable, and an excellent contacting surface, with a minimum shelf life of 12 months under standard storage conditions. The immersion gold layer protects the underlying nickel from oxidation/passivation over its intended shelf life. Thickness specifications are set to ensure the ability of the finish to meet the above criteria.

The ENIG IPC-4552 Specification was issued in 2002, and at the time of setting the specification for ENIG, no lead-free (LF) solder was in use. For thickness, IPC-4552 stated:

- *The EN thickness shall be 3–6 µm [118.1 to 236.2 µin] The IG minimum thickness shall be 0.05 [1.97 µin], at four sigma (standard deviation) below the mean; typical values for IG of 0.075 to 0.125 µm [2.955 to 4.925 µin]*

Although no upper limit was set, the specification had a statement for suggested typical values for IG of 0.075 to 0.125 µm [2.955 to 4.925 µin]. These values were erroneously interpreted to be the specification.

The ENIG specification was amended in 2012:

- The lower limit for thickness was reduced from 0.05 µm to 0.04 µm (1.6 µin) with the following restrictions:
  - Limited time from manufacturing to assembly
  - Demonstrate the consistency of the plating process
  - Ability to measure low gold thickness

Presently, the ENIG 4552 is in revision and should be out in 2015 (Revision A). The objective of the revision is to set new lower and upper thickness limits for the immersion gold, to determine if the restrictions in the amended ENIG

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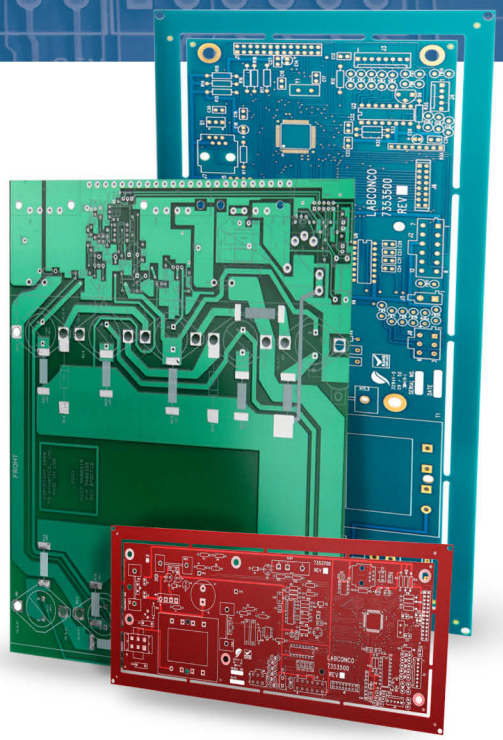

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spec could be lifted, to limit the typical pad size to be measured and to make the specification applicable to LF solder and LF conditioning. This entails an extensive RR study, presently in progress.

The intent is that the revised IPC-4552 Rev A would also include the following Additional Documents:

- Test method (TM) for stripping immersion gold during failure analysis
- Test method for determining the phos content of electroless nickel
- A corrosion chart setting acceptability criteria for nickel corrosion (black pad)

Immersion Silver (IAg)
IPC-4553 A, 2009

IAg is a thin, immersion silver deposit over copper. It is a multifunctional coplanar surface finish, applicable to soldering. It may also be applicable for some press-fit connections and as a contact surface. It has the potential to be suitable for aluminum wire bonding. The immersion silver protects the underlying copper from oxidation over its intended shelf life. Exposure to moisture and air contaminants, such as sulfur and chlorine, may negatively impact the useful life of the deposit. The impact can range from a slight discoloration of the deposit to the pads turning completely black. Proper packaging is a requirement to achieve a 12-month shelf life.

> **In 2009, the immersion silver specification was revised. At this time the lower thickness supplier has discontinued his product and the industry was left with a common thickness from multiple suppliers. This revised specification only had one thickness specified (eliminating reference to thin and thick).**

The Immersion Silver IPC-4553 Specification

In 2005, there were two distinct types of commercialized immersion silver with different thickness recommendations, referred to by the committee as "thin" and "thick." Each required its own thickness specification. This created much confusion as the terms were poorly defined.

The initial IPC-4553 Immersion Silver Specification specified two thicknesses and stated the following for thickness of deposit:

- *Thin Silver: 0.05 µm(2µin) minimum at -2σ from process mean as measured on a pad of area 2.25² µm (3600² mils). Typical value 0.07 µm (3µin) to 0.1 2µm (5µin)*
- *Thick Silver: 0.12 µm (5µin) minimum at -4σ from process mean as measured on a pad of area 2.25² µm (3600² mils). Typical value of 0.2 µm (8µin) to 0.3 µm (12µin).*

In 2009, the immersion silver specification was revised. At this time the lower thickness supplier has discontinued his product and the industry was left with a common thickness from multiple suppliers. This revised specification only had one thickness specified (eliminating reference to thin and thick). The revised specification now includes an upper thickness limit. Typical values were recommended within the specified limits. The pad size for taking the thickness measurement was also specified.

The IPC-4553 Rev A Immersion Silver Specification stated the following for thickness of deposit:

- The immersion silver thickness shall be 0.12 µin [5 µin] minimum to 0.4 µm [16 µin] maximum at ± 4σ from process mean. Typical value between 0.2 µm [8 µin] to 0.3 µm [12 µin] as measured on a pad of area 2.25 mm² or 1.5 mm X 1.5 mm [approximately 0.0036 in² or 0.060 in X 0.060 in] or equivalent.

Immersion Tin (ISn)
IPC-4554, 2007; amended 2012

The immersion tin (ISn) is a metallic finish deposited by a chemical displacement reaction that is applied directly to the basis metal of the printed board, which is copper. The immersion

tin is primarily used as a solderable surface for attachment of components. It may also be used when press-fit connections are employed and for zero insertion force (ZIF) edge connectors. The immersion tin finish protects the underlying copper from oxidation over the intended shelf life (storage of greater than six months) of this finish.

Immersion Tin IPC-4554 Specification

For immersion tin, the committee specified a lower limit for thickness. The relatively thick value of 1 micron (40µin) was chosen to ensure that enough virgin tin would be available at the surface for soldering after extended storage. It is well understood that tin forms an intermetallic (IMC) layer with the underlying copper, and that this layer continues to grow in thickness over time.

The immersion tin thickness will be:

• *µm (40 µin) minimum at -4σ from process mean as measured on a pad of area 2.25² µm (3600² mils) or equivalent. Typical value of 1.15 µm ((46 µin) to 1.3 µm (52µin).*

The Immersion Tin Specification IPC-4554 was amended in 2011. The amendment addressed solderability testing and specified the allowed stress testing conditions for the deposit and the type of fluxes to be used for both tin/lead and LF testing.

Electroless Nickel/Electroless Palladium/ Immersion Gold (ENEPIG) *IPC-4556, 2013*

ENEPIG is a coplanar tertiary layered surface finish plated over copper as the basis metal. ENEPIG consists of an electroless nickel base layer over which is plated an electroless palladium barrier layer followed by a deposit of a thin immersion gold as the final outer layer. It is a multifunctional surface finish, applicable to soldering and to gold, aluminum and copper wire bonding. It is also suitable as the mating surface for soft membrane and steel dome contacts. Additional applications include use in low insertion force (LIF) and zero insertion force (ZIF) edge connectors and for press-fit applications. The electroless palladium layer forms a diffusion barrier that impedes nickel diffusion to the gold surface. The immersion gold protects the palladium layer from reacting with contaminants prior to processing that might otherwise affect joining processes, such as wire bonding and soldering. ENEPIG has a minimum shelf life of 12 months under standard storage conditions. Thickness specifications are set to ensure the ability of the finish to meet all the attributed functionality.

> **ENEPIG is a coplanar tertiary layered surface finish plated over copper as the basis metal. ENEPIG consists of an electroless nickel base layer over which is plated an electroless palladium barrier layer followed by a deposit of a thin immersion gold as the final outer layer.**

The ENEPIG IPC-4556 Specification

This is the last specification issued by the committee. The document produced is very comprehensive and includes a wealth of information from the RR studies that were conducted.

The Appendix contains a documentation of these studies, each authored by the principal who conducted the testing. It also includes a section on the proper methods of equipment setup for a reliable measurement of very thin layers of metal deposits.

The thickness specification for ENEPIG states:

• *Nickel: 3 to 6 µm [118.1 to 236.2 µin] at ± 4 sigma (standard deviations) from the mean.*

• *Palladium: 0.05 to 0.15 µm [2 to 12 µin] at ± 4 sigma (standard deviations) from the mean.*

• *Gold: minimum 0.025 µm [1.2 µin] at - 4 sigma (standard deviations) below the mean. No upper limit was set for IG.*

All measurements to be taken on a nominal pad size of 1.5 mm x 1.5 mm [0.060 in x 0.060 in] or equivalent area.

Organic Solderabilty Preservative (OSP)
IPC Specification (NONE)

OSPs are organic coatings that form a complex organo-metallic complex with the copper surface of the PWB. This complex preserves the solderability of the copper surface through assembly.

A wide variety of OSPs have evolved with the increasing complexity of the PWB. Initially, all that was required was a single thermal excursion for soldering leads into component holes, Then came surface mount that required at least two thermal excursions (one per side); add on top of that the need to hand solder an occasional rework. The biggest relevant evolution is lead-free assembly. LF assembly temperature at 260˚C is approximately 35˚C higher than eutectic soldering (225˚C). The manufacturers of OSP have developed new OSPs to meet the market demands. These have a greater ability to withstand increasing number of thermal excursions and higher temperature, as needed for LF.

OSP products include benzotriazoles, imidazoles, benzimidiazoles and phenyl benzimidazoles. Some of the newer OSPs have additives occasionally referred to as "oxygen scavengers." These additives can stretch the performance window of the specific OSP. The more thermally robust coatings have significantly higher decomposition temperatures than the peak assembly reflow temperature. They require contact with appropriate flux and/or molten solder to penetrate the coating. They have longer shelf life, survive multiple reflow cycles and are more lead-free assembly compatible.

After more than one year of struggling with a specification for OSP, no consensus was reached, and no specification was set forth. This was due to the wide assortment of organic products that were used for solderability preservation for the various applications, each with its own thickness recommended values.

Acknowledgement

To date, all committee activities have been voluntary and acknowledgement is in order for the members and equally important for their respective companies that allow for the time invested by their employees. **PCBDESIGN**

George Milad is the national accounts manager of technology at Uyemura International Corporation. He may be reached by clicking here.

Removing Risk to Unleash the Full Potential of Nanomaterials

The EU-funded NANOREG project is developing the next generation of reliable and comparable experimental data on the environmental, health and safety aspects of nanomaterials. NANOREG, which began in March 2013, has already successfully established the basic conditions for its R&D work and will now move on to deliver on its key objectives.

Nanomaterials are chemical substances or materials that are manufactured at an incredibly small scale (down to 10 000 times smaller than the diameter of a human hair). Experts believe they have the potential to contribute significantly to Europe's industrial competitiveness, and are already used in hundreds of products.

In order to fully capitalise on this potential market however, the safety of nanomaterials must be beyond reproach. As these nanomaterials are often unique and have never been on the market before, assessments must be done on a case-by-case basis using globally recognised and approved methods.

Regular meetings have also been set up with policy makers in partner countries, along with global standardisation institutions in countries like the US, Canada, Australia, Japan and Russia. The long term objective of NANOREG is to ensure that the innovative and economic potential of nanomaterials is not put at risk simply because health and safety issues have not been fully addressed.

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The Future of Nickel in Nickel/ Palladium/ Gold Final Finishes

by Rick Nichols
ATOTECH DEUTSCHLAND GMBH

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Final finishes can be subdivided into metallic and organic finishes. For the purpose of this article, the focus will be on the metallic finishes using the combinations of nickel (Ni) and/or palladium (Pd) and/or gold (Au). Variations on this theme are used extensively in the electronics market of today. The Ni/Pd/Au mutations are the inevitable result of technical requirement changes coupled with true and perceived acceptance within the industry. One such optimization is the phosphorus contents in the Ni and Pd layers. This subtlety will not be focused on in this article as the impact on the key topics is negligible.

This subgroup of metallic final finishes can also be further divided by their application bias. Traditional ENIG processes are biased towards using a protection layer to ensure extended lifetime reliability by protecting the base copper.

- Electroless nickel/immersion gold (ENIG)—*the workhorse*
- Electroless nickel/electroless palladium (pure palladium and phosphor containing palladium)/immersion gold (ENEPIG)—*the all-purpose solution*

The next-generation surface finishes need to be biased towards satisfying lifetime requirements in combination with enhanced technical performance.

- Electroless palladium/autocatalytic gold (EPAG)—*fine-line, high-frequency, solder and bonding application*

This broad segregation implies the inclusion or exclusion of Ni. This Ni protection layer (4–7 µm) has a physical impact on line and space capability whilst simultaneously having a negative impact on high-frequency applications.

The symbiotic relationship between technology influences and the resultant require-

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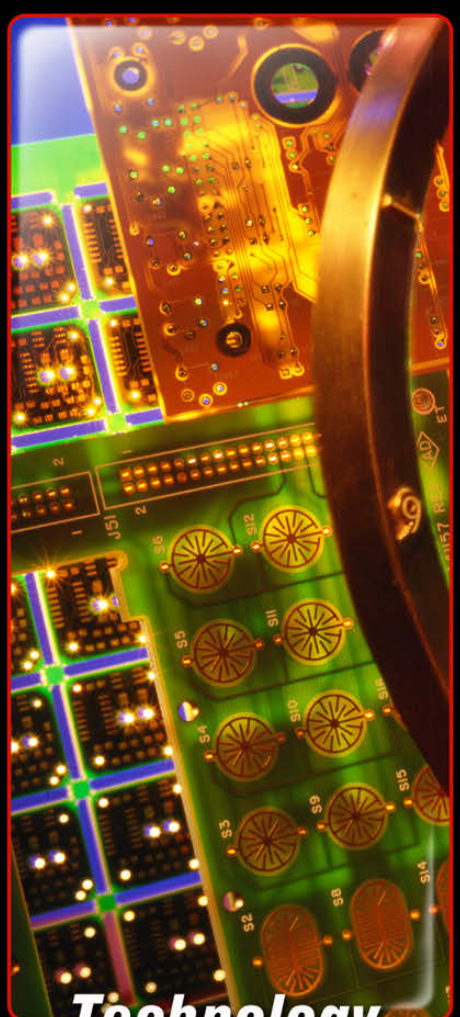

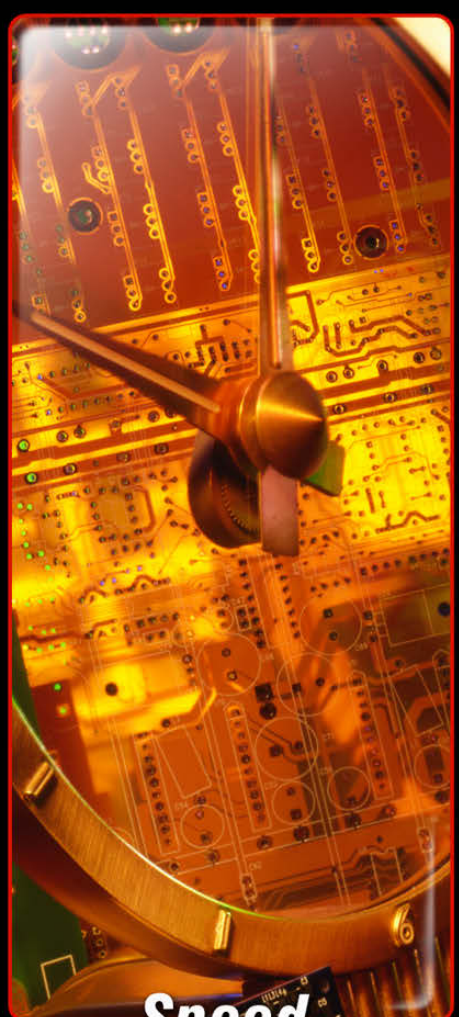

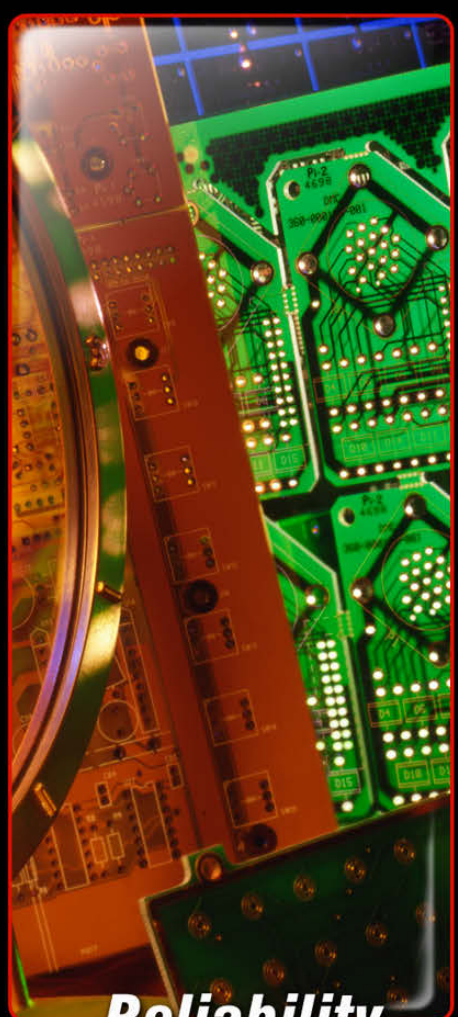

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ments for the final finish is the driving force for this article. It is also the intention of this article to highlight the superiority of the direct palladium processes in achieving the expected requirements of the future.

Generic Technical Requirements

Regardless of the surface finish, there exist perceived and accepted minimum requirements for total functionality. The established standards will inevitably be augmented and many technology sectors will adopt their own performance criteria and expectations as the future era of high-frequency and fine-line applications become more necessary. It is also apparent that the new requirements will also include more economic wire bonding materials.

Despite being vital, solderability satisfies only part of the surface finish requirements. The surface finish must also provide adequate protection of the underlying copper circuitry from the time of substrate fabrication until packaging and assembly (copper corrosion on fine-line technology has the potential to impact significantly on signal integrity). The surface finish should not add to solder joint reliability concerns by contributing to the formation of undesirable intermetallic compounds (IMCs) or adversely affecting their growth. In other words, the bondability must be ensured.

Whilst negating all responsibility for looking into the future, some trends can be predicted as a result of integration trends. Circuit features continue to shrink and maintaining

	Process	ENIG	ENEPIG	EPAG	
	Thickness	Ni: 5µm AU: 0.07µm	Ni: 5µm Pd:0.1µm Au: 0.06µm	Pd: 0.1µm AU: 0.1µm	
Soldering	Multiple Soldering (> 3x soldering steps)	★	★	★	
	Solder Spread (Eutectic Solder)	★	★	★	
	Solder Spread (Lead Free Solder)	★	★	★	
	Solder Joint Reliability (Eutectic Solder)	★	▲	★	
	Solder Joint Reliability (Lead Free Solder)	▲	★	★	
Wire Bondng	Al Wire	★	★	★	
	Au Wire	▼	★	★	
	Pure Cu Wire	●	○	▲	
	Cu-Pd Wire	●	★	★	
	Ag Wire	▼	★	★	Future Considerations
High Frequency capability (Skin Effect)	Media and Sensor Technology	○	○	★	
Fine Line and Pitch Capability (>30:30µm)	Portable Media and Sensor Technology	●	●	★	
Shelf Life	Shelf Life Prior to Assembly	≥ 12 Months	≥ 12 Months	≥ 12 Months	
Very Good ★	Good ▲	Sufficient ○	Limited ▼	No ●	

Figure 1: The generic capabilities of Ni, Pd and Au final finishes. Note: Electroless palladium/immersion gold (EPIG) has not been included due to the process's copper corrosion and poor wire bonding attributes.

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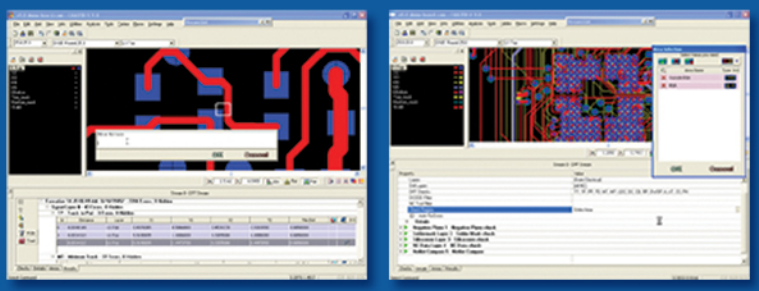

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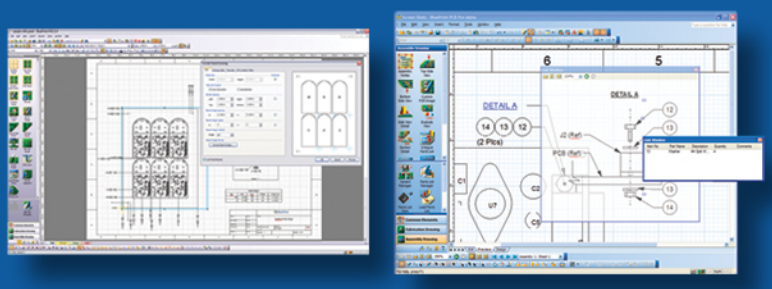

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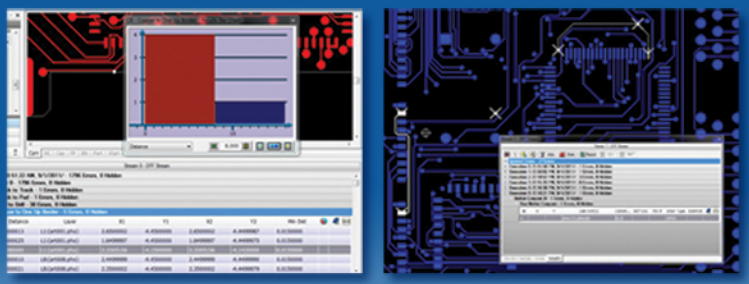

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signal integrity becomes even more challenging. This has a direct impact on assembly, and in response future surface finishes need to accommodate newer adaptations of thermocompression bonding as the established solder technologies are also at the edge of their capabilities.

Topics and Considerations for Future Final Finishes

Fine-line Technology

The concept of fine-line technology already has to factor in the impact of etching to arrive at the required line and space. For example, to achieve 10 µm line and space the circuit will be designed at 12 µm line and 9 µm space. After such painstaking front-end design, final finishes are faced with the challenge of maintaining this integrity as far as possible. With future fine-line technology hinting at 5/5 and even 2/2 the final finish can no longer afford µm scale protection layers such as Ni at 4–7 µm.

A further pitfall of the Ni inclusive technologies is their susceptibility to Ni spread and resultant shorting, even at an abnormally low Ni thickness (the low Ni is required to achieve the line and space criteria).

High-Frequency Capabilities

The widespread use of smartphones and tablets to support daily employment and leisure activities is tangible evidence of the future appetite for high data flow capabilities which necessitates by virtue high-frequency capabilities. Based on history, it is clear that this insatiable appetite will continue to expand.

At very high frequencies surface finishes with a nickel layer become critical. It is known that nickel plated on copper will cause an ad-

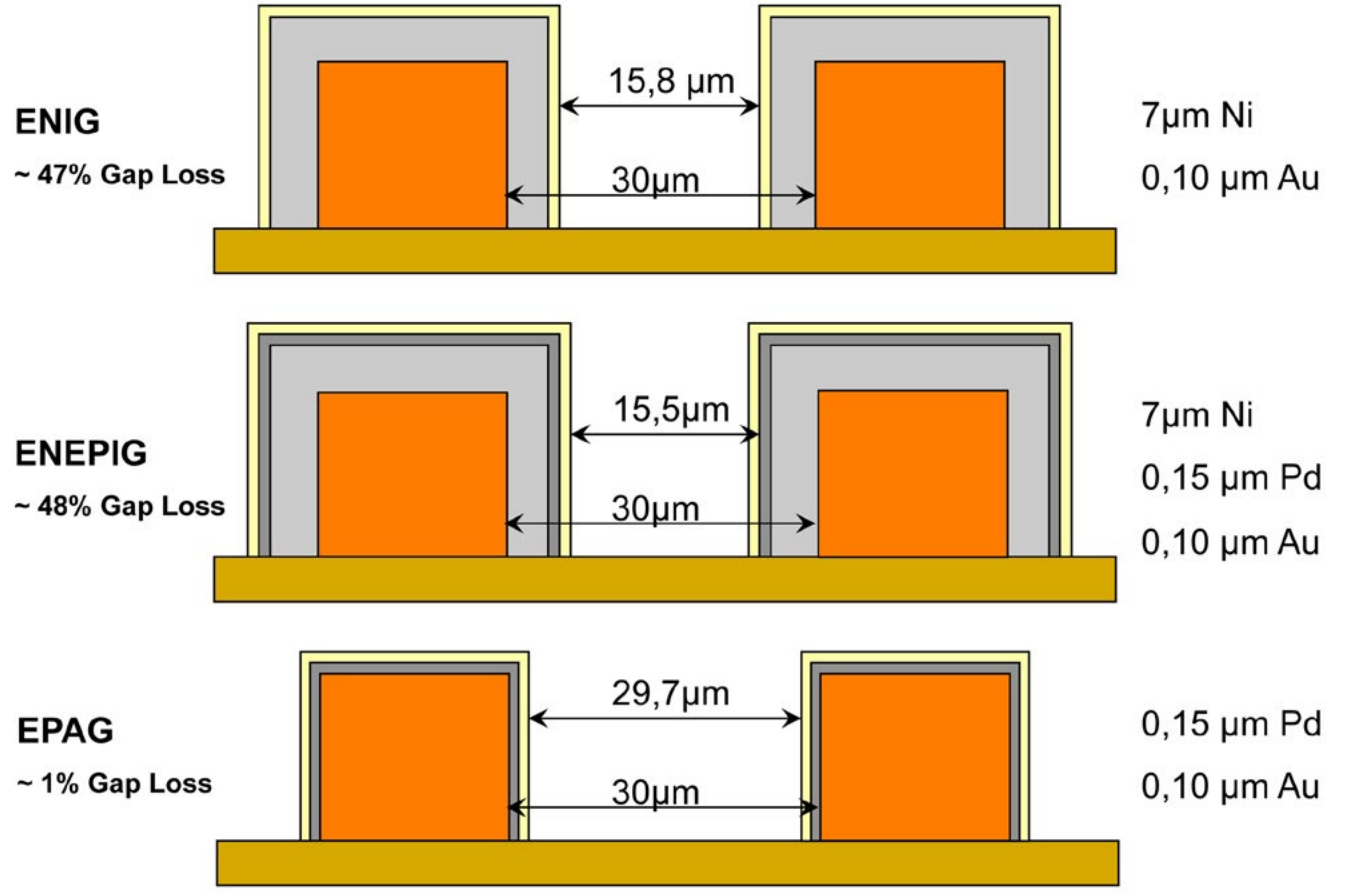

Figure 2: The impact of established Ni containing finishes on line and space.

ditional loss to signal propagation due to the so called "skin effect." Initially proposed by Horace Lamb in 1883 for spherical conductors, it was then applied to conductors of any shape by Oliver Heaviside in 1885 (Wikipedia). In laymen's terms, the theory promulgates that induced electromagnetic fields (eddy currents) caused by alternating current will orientate the highest current density flow to the outside of the conductor. This is referred to as the skin effect. In turn, different conductor properties (electrical and magnetic) in conjunction with differ-

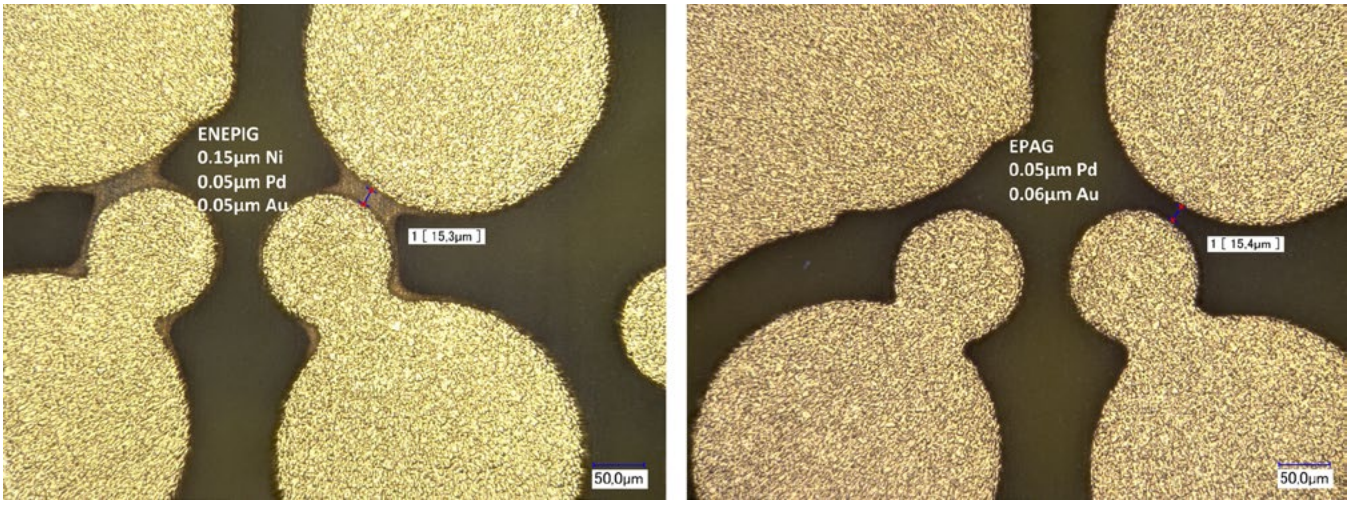

Figure 3: The potential for spreading when using a Ni inclusive finish.

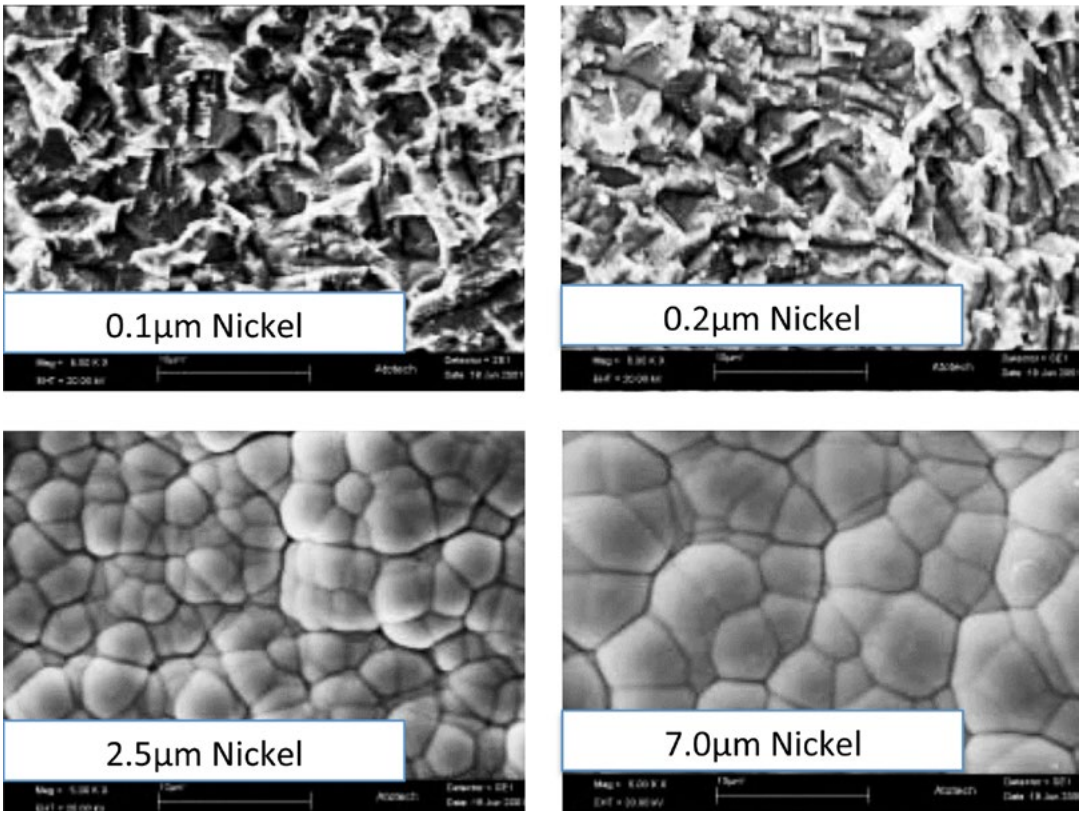

Figure 4: The impact of frequency on skin depth (δ) with reference to process application.

ent frequencies will exhibit different skin depths (δ). With a given conductor property the skin-depth decreases exponentially with the increase of frequency.

The inclusion of Ni at 4–7 µm ensures that the primary signal will pass through the outer Ni skin. Not only is nickel a poorer conductor than copper, the effective area for the signal to pass through is greatly reduced. This is rather like placing your thumb over the end of a hose pipe, the resultant water flow is reduced and the directional flow is greatly disturbed.

The skin effect is one of the reasons why the electronics industry needs to entertain the notion of nickel-free surface finishes.

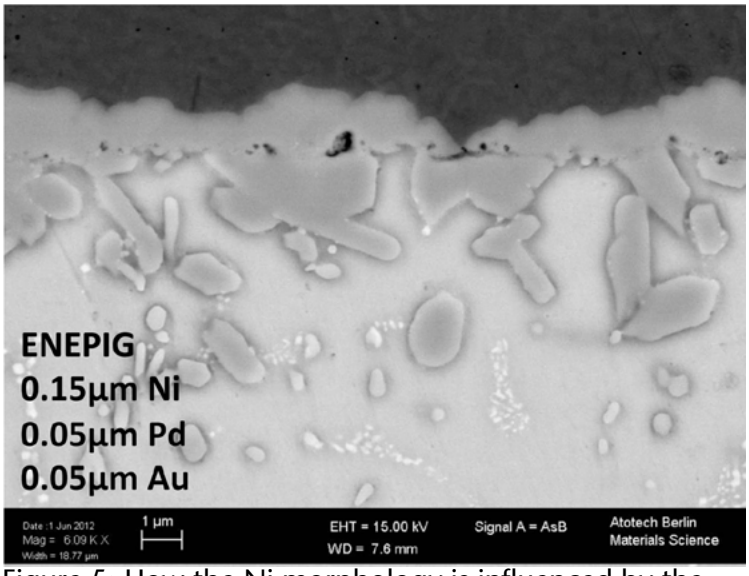

Figure 5: How the Ni morphology is influenced by the layer thickness.

ENIG

Thousands of words have already been written about the workhorse, ENIG, and many panels have been processed successfully using it. This is an established process that fulfils the requirements of many existing and past applications but falls short of the requirements promised in the future. As such this process will not feature further in this article unless to make a comparison.

ENEPIG with Thin Ni

Although in terms of words and production, the above is equally true for the "the all-purpose solution" (ENEPIG) process, this is the most promising of the Ni inclusive processes. In addition to performing well generically there a frequent question is raised within the industry:

Why can't this process fulfil future requirements by employing a thin Ni layer?

Ni is employed as a barrier layer due to its dense crystal formations. The surface morphology, in turn is created by thicker Ni plating. This is the background for the IPC (4552 – ENIG and 4556 – ENEPIG), minimum thickness requirement of 3µm.

Higher Ni thicknesses positively influence the integrity of solder joints. By reducing the Ni layer to conform to dimensions dictated by EPAG, dramatic quality issues are encountered. Early indications of this can be found by examining the intermetallic compound (IMC) by SEM. Whilst the IMC created using EPAG has no detrimental impact to the solder joint, the IMC created using EN (low thickness) EPIG displays evidence of demarcation lines.

Demarcation lines are cosmetically alarming and create concerns for the end-user. This is not an acceptable situation. The impact of demarcation lines, in terms of quality, can be demonstrated using a drop test. The drop test is a simulation of a handheld device being dropped.

According to the drop test, the performance of the EPAG system is superior to that of the thin Ni ENEPIG process. In addition to the poor drop test performance, the thin Ni layer becomes superfluous as a protection layer due to the low thickness and resultant poor morphology.

Silver Wire Bonding

Wire bonding is a field that is evolving like any other. Bonding speed, wire hardness and cost are all in the mix. Some 3D packaging philosophies mean that wire bonding is here to stay unless it is replaced completely by flip-chip derived bonding technology. Reduction in cost without yield and capacity loss is a ma-

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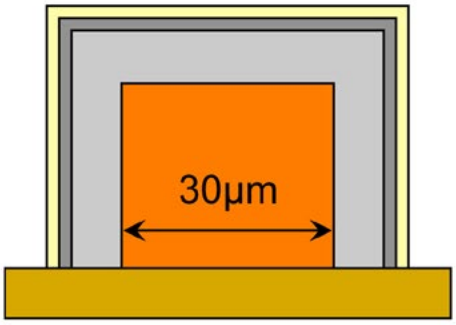
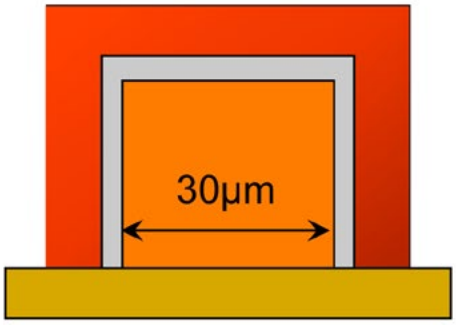
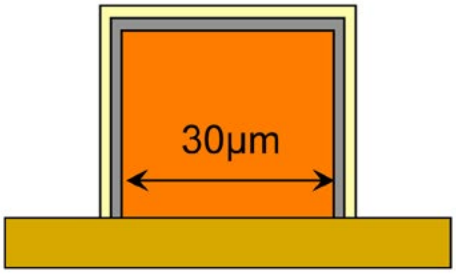
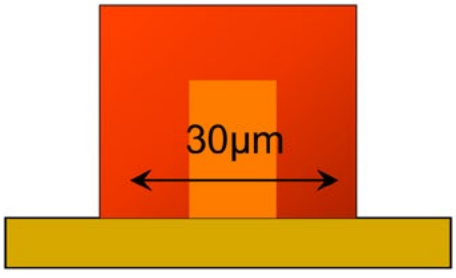
ENEPIG		
δ µm	~17	~1.7
High CD area µm² : Conductor µm²	~81%	~11%
EPAG		
δ µm	~210	~21
High CD area µm² : Conductor µm²	100%	~91%

Figure 6: The impact of low Ni on demarcation lines.

jor driver in this field. Pure copper wire bonding is one candidate for cost reduction, but this can result in other complications like component and equipment damage due to the forces and energy required. Gold, on the other hand, is the preferred and established medium, but recent exploration into silver wire bonding is proving potentially viable. The high potential for silver as a technical replacement for gold is the comparable softness of the metals. Figure 1 demonstrates that ENEPIG and EPAG are both able to deliver confidence in silver wire bondability. Additional to the technical similarities, silver also complies, in some way, to cost saving.

EPAG exhibits a wide working window with good performance indicators for silver wire bonding. Well known OEMs are also championing this direction for wire bonding. The results for Cu wire bonding are also acceptable.

A Look into the Future

The roadmaps, available in the public domain, according to the following OEMs, IPC, iNEMI, ITRS and Jisso, predict fine-line technology. This, by definition, has a knock on impact to pitch miniaturization. This applies equally to organic and inorganic substrates.

As part of flip-chip bonding technology, the tried and tested reflow bonding is limited with

THE FUTURE OF NICKEL IN NICKEL/PALLADIUM/GOLD FINAL FINISHES *continues*

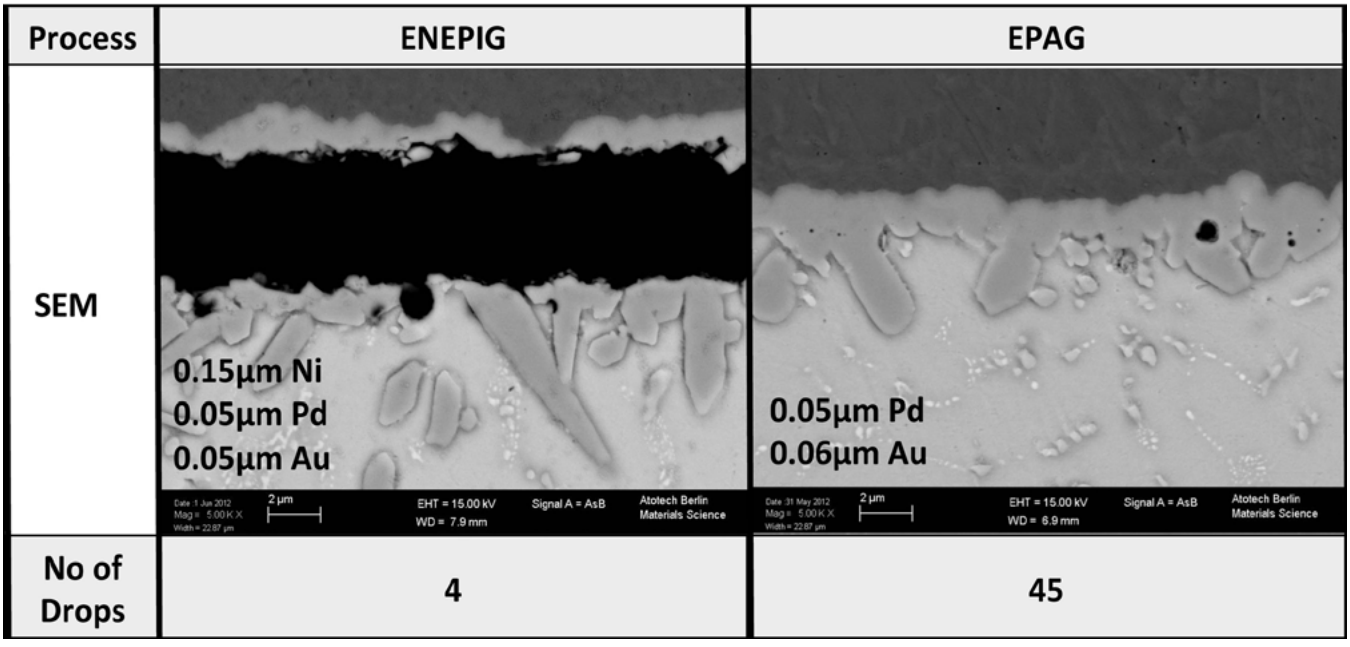


Figure 7: The performance comparison of the low Ni ENEPIG compared to the EPAG process.

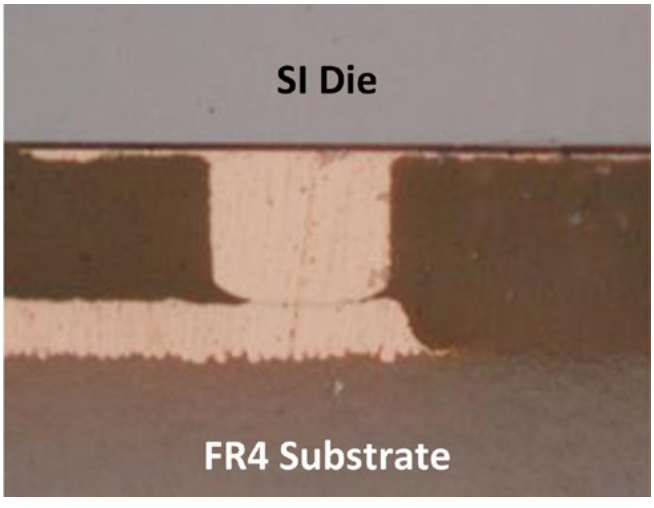


Figure 8: Performance of EPAG for AG wire bonding.

regard to in/out (I/Os) density. With the value of real estate becoming so important, the space utilized by reflow bonding techniques is becoming an obstacle. When discussing real estate, it is common to solve the issue with an expansion in the Z-axis. In the property market this is fine, but in the portable electronics market this direction is also becoming crucial. The Z-axis constraints are high-speed signal transfer and signal integrity. The reflow process requires the application of solder. Aside from this procedure being already at the application limit, the utilization of solder does not lie within the remit of controlled Z-axis expansion and is also a comparatively poor conductor compared to copper or other more noble metals. Here we have established that not only will the I/Os increase in density (decrease in pitch), but the pillar height (standoff height) will also become paramount to future developments. To this end Atotech is cooperating with Georgia Institute of Technology to assess the viability of using EPAG as the pillar and pad finish for thermo-compression bonding.

There exists a prior art to thermo-compression bonding (TCB). These can be characterized in Figure 9.

Although the prior art technologies are proven, there are some viable benefits in using EPAG as the copper interconnect. Not only can the key performance indicators or benefits can be compared to direct Cu-Cu bonding, but can be improved upon.

Conclusion

Although ENIG and ENEPIG still have a place in a supplier's portfolio, the future is look-

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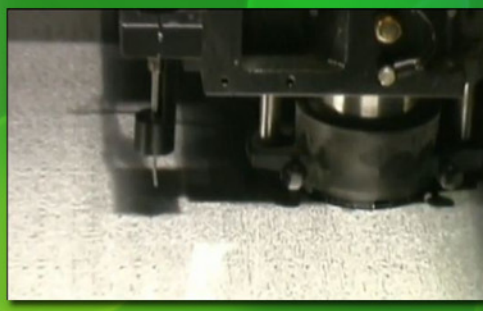

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		Prior Art		EPAG as Low T°C Cu interconnect
		Current Direct Cu-Cu Bonding R&D	Curent Cu pillar with Solder-Cap Process	
Pitch		Pure Cu interconnection <10µm	Cu: Solder interconnect ~ 25µm	Cu interconnect <10µm
Properties	Electromigration	> 1000 hours @10^{-6} A/cm², 130°C	10^{-4} - 10^{-5} A/cm²	> 1000 hours @10^{-6} A/cm², 130°C
Manufacturing Considerations	Bonding T°C	> 250°C	~ 260°C	< 200°C
	Bonding t (s)	600	<60	30
	Bonding Pressure	High	Low	High
	Bonding Environment	Noble atmosphere or vacuum	Air	Air
	Non-Coplanarity Offset	<< 1µm (no bump collapse in solid-state bonding)	>3µm (high risk of bridging)	>3µm (bumping collapse under pressure, minor lateral deflection)

Figure 9: The characteristics of prior art TCB compared to EPAG. (The highlights are in green.)

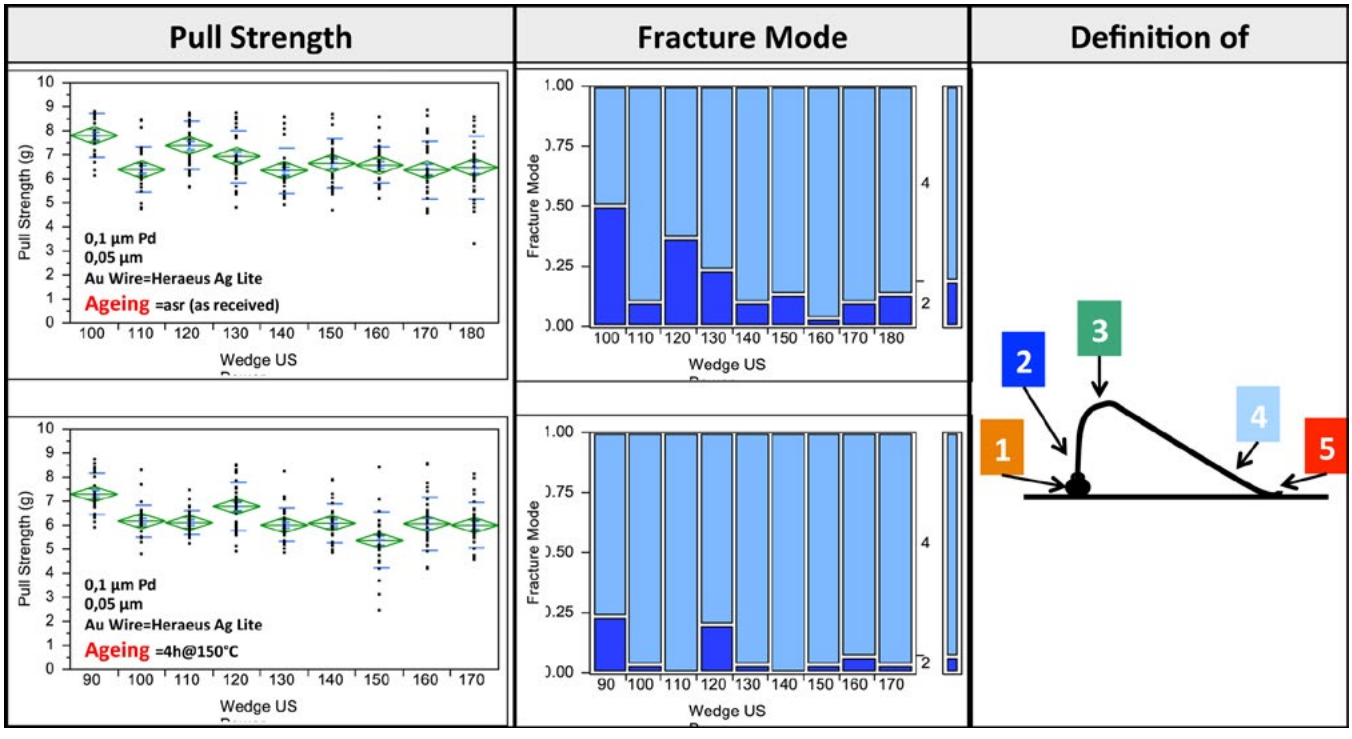

Figure 10: This demonstrates initial results achieved at the Georgia Institute of Technology (TCB at 190C – 3s – 365MPa with perfect electrical yield [1-2Ω]).

ing bright for the EPAG process. Hinged on the discussions above it is apparent that Ni presents some difficulties when considering its suitability within the scope of future requirements. The target of this article is to highlight the superiority of the EPAG process in ascertaining the goals of the future. **PCBDESIGN**

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Learning the Curve

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD

Currently, power integrity is just entering the mainstream market phase of the technology adoption life cycle. The early market is dominated by innovators and visionaries who will pay top dollar for new technology, allowing complex and expensive competitive tools to thrive. However, the mainstream market waits for the technology to be proven before jumping in. Power distribution network (PDN) planning was previously overlooked during the design process, but it is now becoming an essential part of PCB design. But what about the learning curve? The mainstream market demands out-of-the-box, ready-to-use tools.

The mainstream market, representing more than 65% of the total EDA software market, wants established technology at an affordable price. The majority of high-end tools require a PhD to drive. However, the mainstream market demands tools that are intuitive and can be used by any member of the development team from EEs to PCB designers to achieve quick results.

Inadequate power delivery can exhibit intermittent signal integrity issues. These include high crosstalk and excessive emission of electromagnetic radiation, degrading performance and reliability of the product. The PDN must accommodate variances of current transients with as little change in power supply voltages as possible. So the goal of PDN planning is to design a stable power source for all the required power supplies. As with stackup planning, the PDN design is required before a single IC is placed on the board.

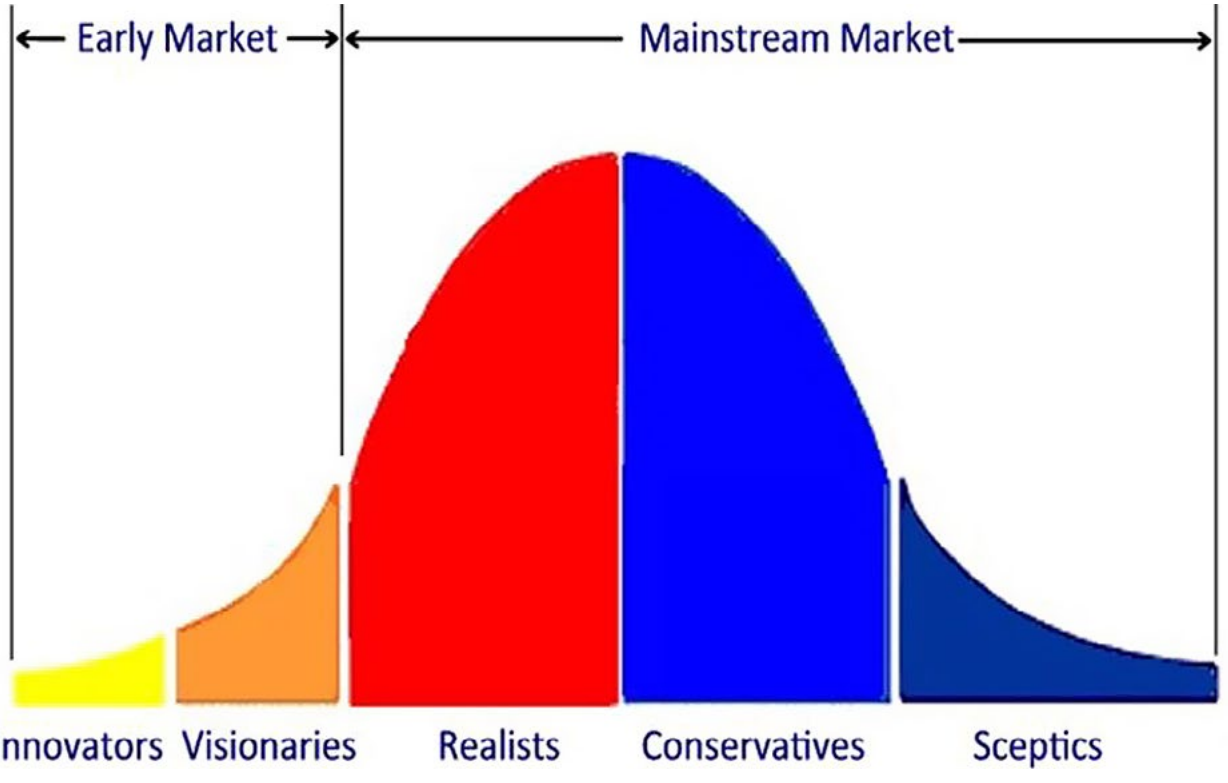

Figure 1: Technology adoption life cycle (Geoffrey A. Moore's Crossing the Chasm).

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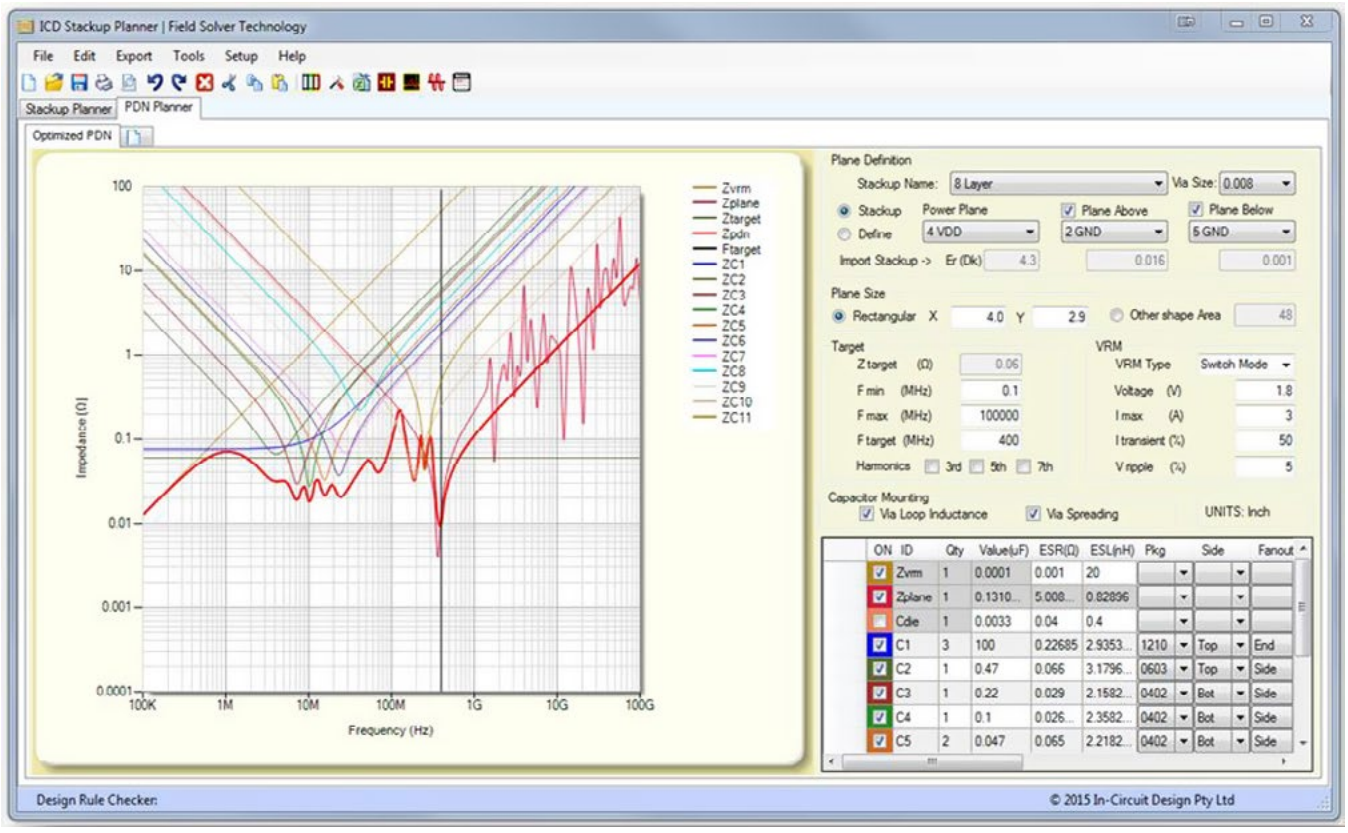


Figure 2: PDN with optimized decoupling.

Also, the same PDN connections (planes) that are used to transport high-transient currents are used to carry the return currents for critical signal transmission lines. If high-frequency switching noise exists on the planes, coupling may occur, resulting in ground bounce, bit failure or timing errors. Many failures to pass electromagnetic compliancy (EMC) are due to excessive noise on the PDN coupling into external cables and radiating emissions.

If you are not familiar with a PDN plot (AC impedance vs. frequency), it can be awfully daunting at first. Figure 2 shows the ICD PDN Planner with a typically 400MHz fundamental frequency and with an optimized capacitor selection. Please refer to my previous series PDN Planning and Capacitor Selection to understand the effects of bypass and decoupling capacitors on the PDN, as this column will focus on the plane resonance.

The AC impedance (thick red curve) should be below the target impedance up to the maximum bandwidth. For a 400MHz fundamental frequency, the maximum bandwidth is 2GHz to take in the 5th harmonic. But I am frequently asked one question: Does it have to be low all the way up to 2GHz?

In Figure 2, you will notice the ringing in the top right corner of the plot. This is the plane resonance. As the frequency approaches half wavelength, the planes (power and ground) act as an unterminated transmission line and start to resonate. This resonance is not a problem unless it falls on the fundamental frequency or one of the odd harmonics. A Fourier series expansion of a square wave is made up of a sum of odd harmonics. If the waveform has an even mark-to-space ratio then the even harmonics cancel.

Figure 3 illustrates the typical electromagnetic (EM) radiation spectrum analyzer plot for a 400MHz DDR2 data signal. The fundamental frequency generally has little radiation, but then increases up to the 5th harmonic and re-

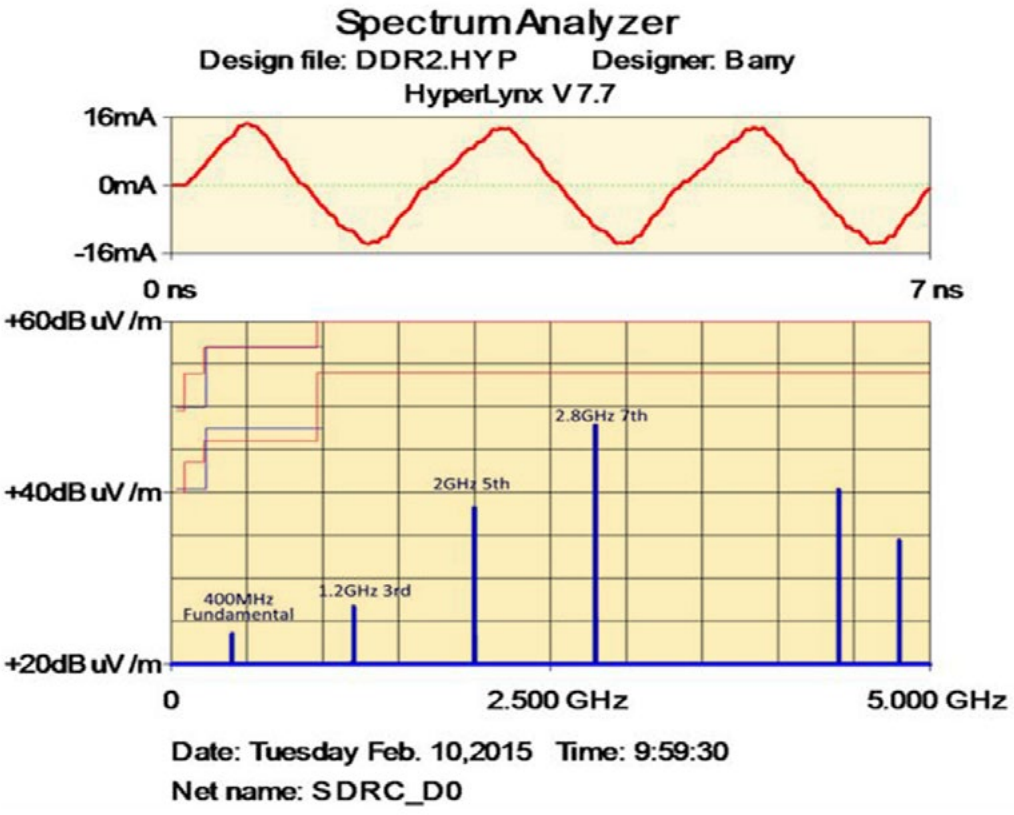


Figure 3: EM radiation from a DDR2 data signal @ 400MHz.

duces again with the higher harmonics. But I have seen cases where even the 11th harmonic—4.4GHz in this instance—can create problems.

So what does this EM radiation have to do with the PDN analysis? If the AC impedance is high at the fundamental frequency or at any of the odd harmonics, then the board will radiate. In Figure 4, I have superimposed the EM radiation on the PDN plot. Look at where both the radiation and plane resonance peak. If these coincide, then you will have excessive radiation at that particular frequency. In this case, the fundamental 400MHz has a very low impedance so it will not be an issue. But, the 7th harmonic is high and the 5th is borderline. Fortunately, the amplitude diminishes as the frequency decreases.

I have pointed out a possible issue on the 5th and 7th harmonics in Figure 4, so how do we fix it? Decoupling capacitors are only effective below 1GHz, so no matter how many are added, to the PDN, they will not reduce the 2 and 2.8GHz peaks. However, above 1GHz, there are a number of ways to reduce the AC impedance:

1. On-die capacitance. Capacitors are placed on the IC itself by the manufacturer and generally cannot be changed. However, in some cases, the capacitors are on the top of the IC. It may be possible to piggyback parallel capacitors to increase their effect.

2. Reduce the loop inductance of the decoupling capacitors. This can be achieved by moving the decaps to the top side of the board so that the fanout vias have less distance to travel to the power and ground planes in the substrate. The loop inductance can also be reduced by using multiple vias per land and spacing them close to each other to reduce the loop area. But this reduced inductance has minimal effect above 1GHz.

3. Select a material with lower dielectric constant. This will push the plane resonance to a higher frequency.

LEARNING THE CURVE *continues*

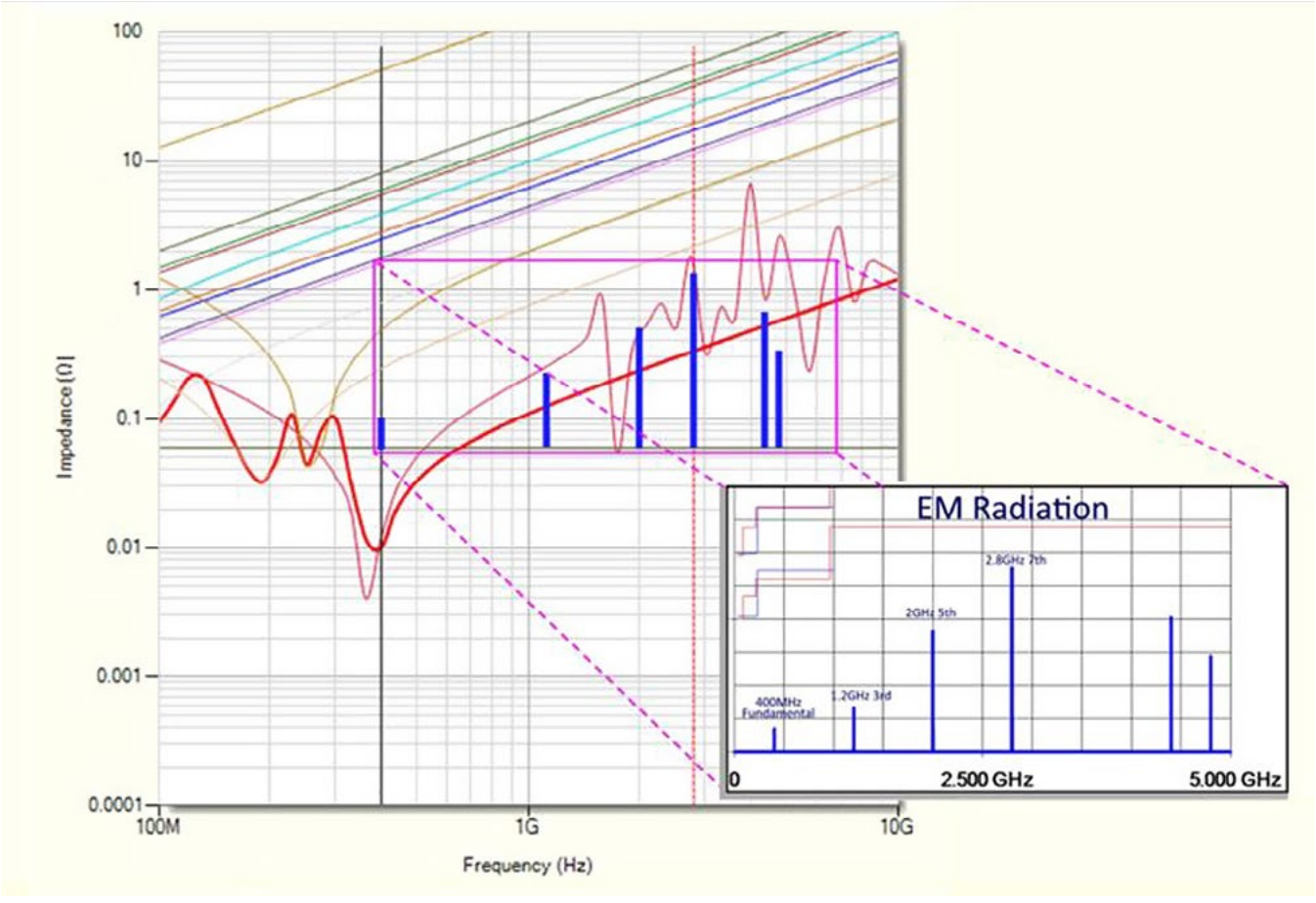


Figure 4: EM radiation overlapped on the PDN plane resonance.

4. Increase the planar capacitance. This is where the tight integration between the ICD Stackup Planner and PDN Planner comes into play. You can add, say, 3M embedded capacitance materials between the planes and then import this stackup back into the PDN Planner. This material typically has 20nF/in^2 capacitance and significantly reduces the AC impedance above 1GHz. Ultra-thin laminates are very expensive, but another option is to put two plane pairs, of twice the dielectric thickness, in parallel to achieve the same effect at a lower cost.

5. Modify the plane area (capacitance). Obviously, a DDR2 1.8V plane will not cover the entire area of the board. By reducing this area to as small as possible (2-square inches) the self-resonance of the plane will be moved up in frequency, reducing the AC impedance at the higher frequency and shifting the peaks. Reducing the plane area however, will also reduce the overall attenuation by increasing the characteristic impedance. Also, keep the area as square as possible. If you create a thin rectangular shape, then the plane resonances will increase due to the different standing wave ratios of the X and Y directions being uneven, thus creating more parallel resonance peaks.

The optimization of the PDN is a trial-and-error process that needs to be done in conjunction with the stackup materials to fully exploit all avenues. Suppressing the plane resonance peaks at the odd harmonics, to provide a low impedance profile at higher frequencies, also helps to minimize electromagnetic emissions.

Points to Remember

- The mainstream market waits for the tech-

nology to be proven before jumping in.

• This market, representing more than 65% of the total EDA software market, wants established technology at an affordable price.

• Inadequate power delivery can exhibit intermittent signal integrity issues.

• The PDN must accommodate variances of current transients with as little change in power supply voltages as possible.

• The AC impedance should be below the target impedance up to the maximum bandwidth (5th harmonic).

• As the frequency approaches half wavelength, the planes act as an unterminated transmission line and start to resonate. This resonance is not a problem unless it falls on the fundamental frequency or one of the odd harmonics.

• The fundamental frequency generally has little radiation but then increases up to the 5th harmonic and reduces again with the higher harmonics.

• If the AC impedance is high at the fundamental frequency or at any of the odd harmonics, the board will radiate.

• Above 1GHz, there are a number of ways to reduce the AC impedance. The most effective being increasing planar capacitance and modifying the plane area. **PCBDESIGN**

References:

1. Barry Olney's Beyond Design columns: PDN Planning and Capacitor Selection, Part 1 & Part 2; Power Distribution Network Planning

2. Geoffrey Moore: Crossing the Chasm

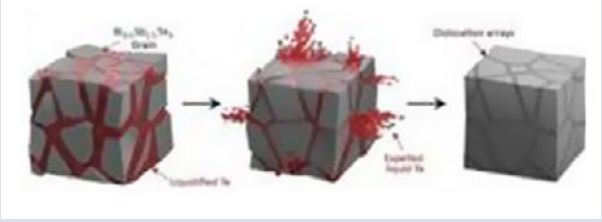
For information on the ICD Stackup and PDN Planner, click here.

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. The company developed the ICD Stackup Planner and ICD PDN Planner software, is a PCB Design Service Bureau and specializes in board level simulation. To read past columns, or to contact Olney, click here.

Breakthrough in Thermoelectric Materials

French physicist Jean Charles Athanase Peltier discovered a key concept necessary for thermoelectric (TE) temperature control in 1834. His findings were so significant that TE devices are now commonly referred to as Peltier devices. Since his work, there have been steady advancements in materials and design. Despite the technological sophistication Peltier devices, they are still less energy efficient than traditional compressor/evaporation cooling.

In the 1960s, Peltier devices were primarily made from Bismuth-Telluride (Bi2Te3) or Antimony-Telluride (Sb2Te3) alloys and had a peak efficiency (zT) of 1.1, meaning the electricity going in was only slightly less than the heat coming out. Since the 1960s there have been incremental advancements in alloy technology used in Peltier devices.



TE alloys are special because the metals have an incredibly high melting point. Instead of melting the metals to fuse them, they are combined through a process called sintering which uses heat and/or pressure to join the small, metallic granules.

The applications for such a material are abundant. As new fabrication techniques are developed, Peltier cooling devices may be used in place of traditional compression refrigeration systems. More importantly, as electrical vehicles and personal electronic devices become more ubiquitous in our daily lives, it is becoming increasingly necessary to have more efficient systems for localized electrical power generation and effective cooling mechanisms. This new thermoelectric alloy paves the way for the future of modern TE devices.

RF Power Capabilities of High-Frequency PCBs

by John Coonrod
ROGERS CORPORATION

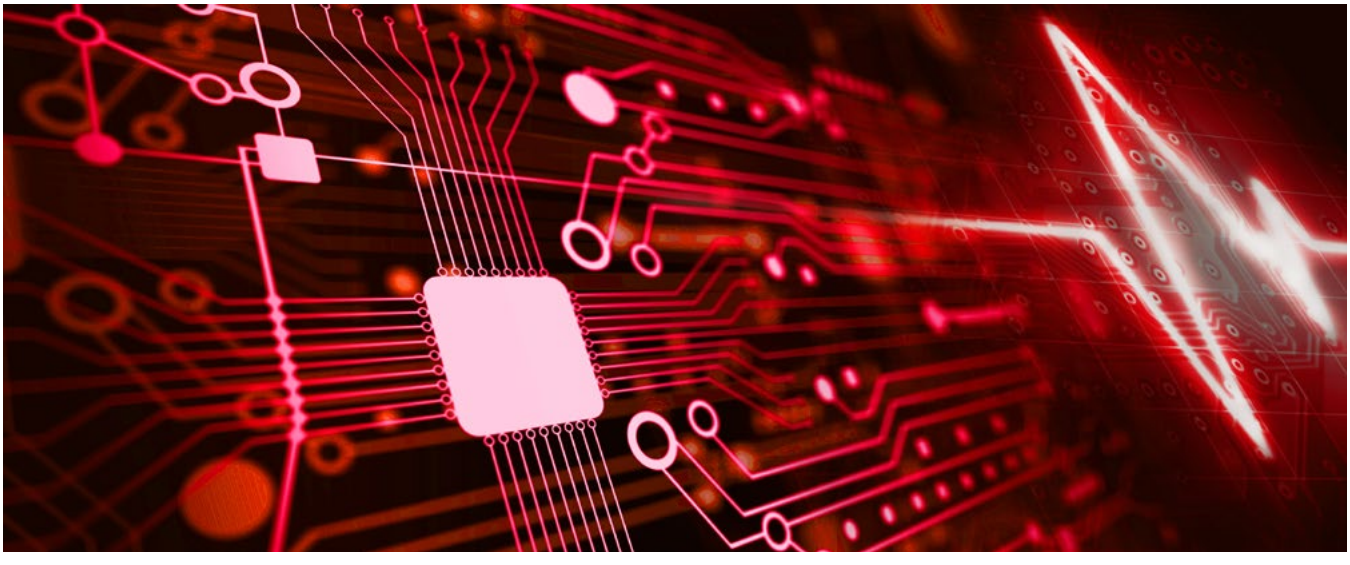
I often hear this question: "How much RF power can be applied to a high-frequency PCB?"

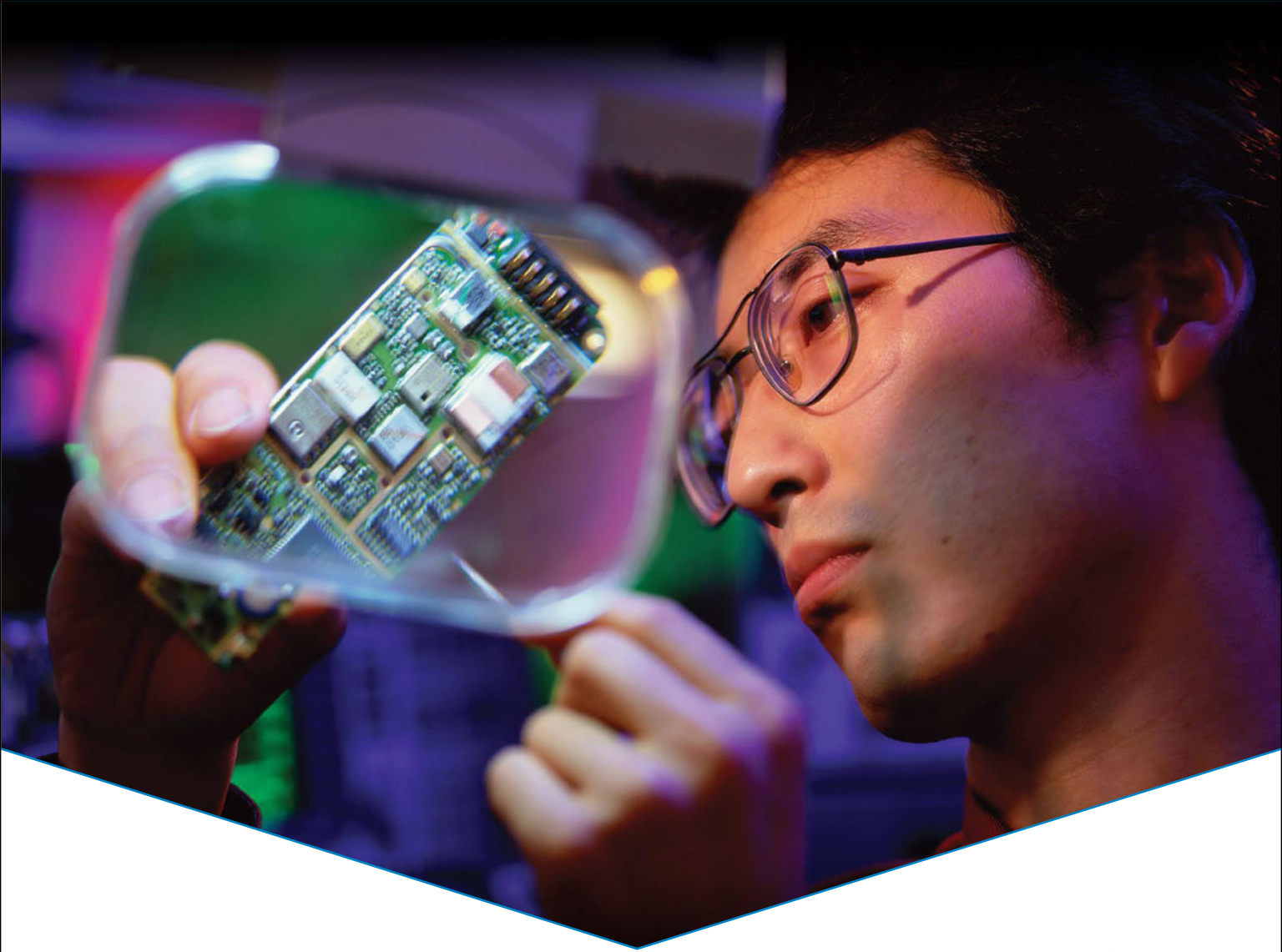
My answer sometimes surprises engineers. I tell them that they can put as much RF power into the PCB as they want, with the assumption that the PCB does not exceed its maximum operating temperature (MOT). MOT refers to the maximum temperature to which a circuit can be exposed without degradation of critical properties. The actual RF power limit of a PCB is based on the MOT of the circuit, and that is dependent on the circuit material, the PCB construction and fabrication process.

The relative thermal index (RTI) is a rating given to UL-rated circuit materials for the maximum temperature to which the raw material can be exposed indefinitely without degradation in material properties. But when the raw material is made into a circuit, MOT is the rating that is most applicable to the power-handling capability of a circuit. The MOT is always less than a circuit material's RTI. When reviewing the maximum RF power-handling capability of a PCB, MOT is used as the maximum temperature of which a circuit can be exposed over long periods of time.

For example, a circuit with a heat rise of +70°C above an ambient of +25°C must endure a temperature of +95°C indefinitely. The RF power which creates this heat rise is acceptable if the circuit has a MOT rating of +105°C. But if the circuit's heat rise is greater than +80°C above ambient, the applied RF power level that created the heat rise would not be acceptable.

When considering circuit heating due to applied RF power, modeling the heat rise of high-frequency PCBs can be difficult. Many variables influence heat rise, and they must be taken into account. Insertion loss is the total RF loss of a high-frequency PCB and is equal to the summation of conductor loss, dielectric loss, radiation loss and leakage loss. Insertion loss is the cause of the heat generated when RF power is applied. A circuit with a high level of insertion loss will generate more heat than a circuit with lower insertion loss, when considering the same





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RF POWER CAPABILITIES OF HIGH-FREQUENCY PCBS *continues*

amount of applied RF power. Insertion loss can also be difficult to model, because there are subcomponents that make up insertion loss. Typically, the major contributors to insertion loss are dielectric loss and conductor loss.

Dielectric loss is related to the dissipation factor (Df) and the tangent delta (tanδ) of the material. A material with higher Df causes higher dielectric loss, which in turn can cause higher insertion loss and high temperature rise with applied RF power. Conductor loss is far more complicated than dielectric loss, with several components making up conductor loss. In general, a circuit using copper with a rough surface will have more conductor losses than a circuit using smooth copper. Additionally, there is a circuit thickness relationship, and a thinner circuit will be more prone to conductor loss variables than a thicker circuit. The thicker circuit is more dominated by dielectric loss.

One major consideration for understanding RF power capabilities of a high-frequency PCB is to understand the impact of insertion loss. Generally, a circuit material and design will be chosen to minimize insertion loss, but there are tradeoffs and other issues to consider.

All circuit materials exhibit a property known as thermal conductivity: the measure of the ability to pass heat energy through that material. An extremely good thermal conductor is copper, which has a thermal conductivity value of 400 W/m/K. However, most substrates used for high-frequency PCBs have thermal conductivity values that are considered a thermal insulator or a very poor thermal conductor. Most high-frequency circuit materials have thermal conductivity values in the range of 0.2–0.4 W/m/K. A value of 0.5 W/m/K or higher is considered good for thermal conductivity for a PCB dielectric material.

Now, let's consider at quick tradeoff. There are some extremely low-loss PTFE materials which can be designed so the circuit will have minimal insertion loss. This means the circuit will generate less heat when RF power is applied and a designer may assume that higher power levels could be applied. However, many PTFE materials have very low thermal conductivity and even though there is less heat generated, the heat cannot efficiently get out of the circuit, so the circuit may heat more than expected.

One major consideration for understanding RF power capabilities of a high-frequency PCB is to understand the impact of insertion loss. Generally, a circuit material and design will be chosen to minimize insertion loss, but there are tradeoffs and other issues to consider.

Another tradeoff to consider is the thickness of the circuit. As an example, a double-sided circuit, which is a simple microstrip circuit bonded to a heat sink, will stay cooler if the circuit is thin, as opposed to thick, when using the same materials and same applied RF power. The thinner circuit has a shorter heat flow path from where the heat is generated at the signal conductor, through the dielectric and to the ground plane below which is attached to the heat sink.

There are several additional tradeoffs to consider, but a quick summary would show that the optimum circuit would use a material with low dielectric loss and smooth copper, which gives low insertion loss and generates less heat. Additionally, the optimum material would have high thermal conductivity and would be relatively thin.

A few high-frequency materials meet these criteria. When working with RF and microwave designs, consulting your materials provider can save you time and money. These companies have plenty of information about thermal conductivity, insertion loss, heat flow, overall thermal management, and much more. **PCBDESIGN**

John Coonrod is a senior market development engineer for Rogers Corporation. To read past columns, or to reach Coonrod, click here.

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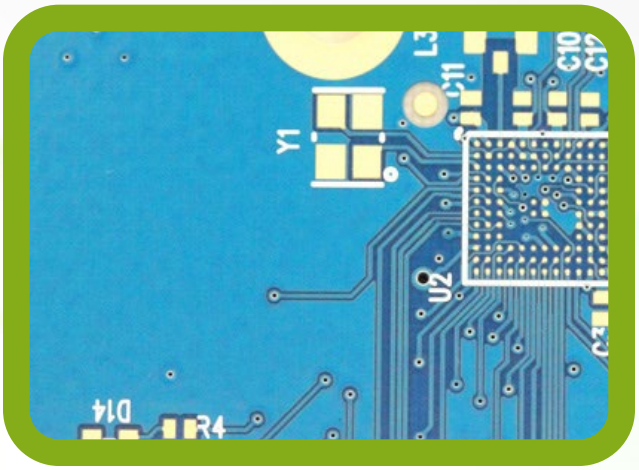

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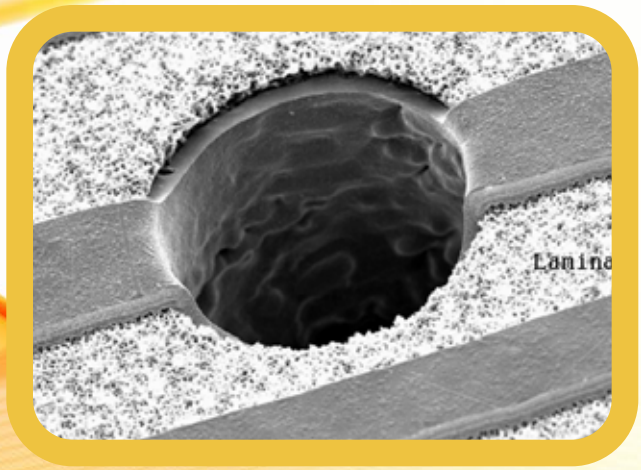

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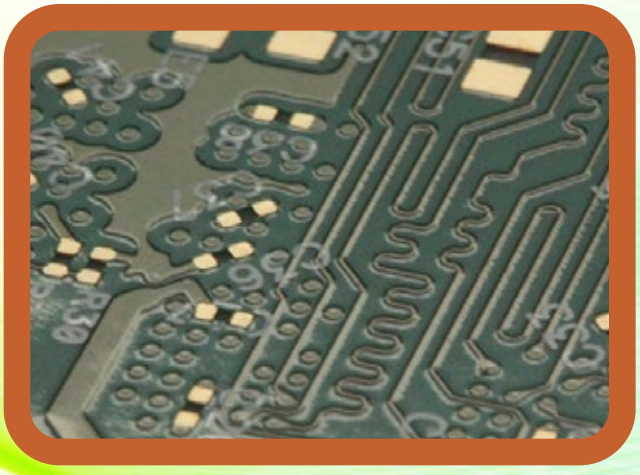

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News Highlights

How 3D Printing will Impact PCB Fabrication

In the near future, we will enter an era where electronic devices are printed, rather than assembled. They will be fabricated layer-by-layer as a single object, rather than assembled from separate mechanical, electrical, and optical parts. This article describes the implications that 3D printing will have on PCB manufacturing.

Material Witness: Low-Flow Prepregs—Defining the Beast!

The term "low flow" should make sense to both suppliers and users of the products. A low-flow prepreg flows sufficiently to wet out and adhere to bonding surfaces and to fill innerlayer copper details, but does not flow so much as to fill in cutout areas in a heat sink or run unevenly out of the interface between rigid and flexible elements of a rigid-flex PWB.

Raising a Unified Voice for an Advanced Manufacturing Economy

The electronics manufacturing industry is an important sector in the global economy, and John Hasselmann, VP of Government Relations at IPC, is an advocate for policies that will help our industry, as well as the prosperity and welfare of billions of people.

Reliability and Harmonization of Global Standards at Forefront of EIPC Efforts

At IPC APEX EXPO 2015, I-Connect007 Technical Editor Pete Starkey caught up with EIPC's Michael Weinhold and Alun Morgan, who were happy to discuss both recent and ongoing focuses for EIPC, namely, reliability. Also touched on was the importance of the alignment of global standardization processes, especially for Asia.

FlexTech Honors Flex Electronics Firms

FlexTech Alliance awarded Thin Film Electronics, Vitex Systems and Pacific Northwest National Laboratories (PNNL), and California Polytechnic Institute's Graphic Communication Department with the 7th annual FLEXI Awards for Innovation, R&D, and Leadership in Education awards, respectively.

Schmoll Keeping an Eye on the Future—and on LDI

In this interview, Thomas Kunz, who has been at the helm of Schmoll Maschinen as president since 1993, discusses the company's lengthy history in mechanical engineering (more than 70 years!), current global scope, and what he sees as a steady progression in directions that make the most sense to customers, which include laser direct imaging.

IPC Volunteers Recognized at APEX

IPC presented Committee Leadership, Distinguished Committee Service and Special Recognition awards at IPC APEX EXPO® at the San Diego Convention Center in February. The awards were presented to individuals who made significant contributions to IPC and the industry by lending their time and expertise through IPC committee service.

IPC Opens Latest Statistical Programs

IPC's global statistical programs for the laminate, solder, process consumables and assembly equipment industries are now open to new participants for 2015. The deadline for IPC members to sign up is April 15. Participation is free to IPC-member companies as a benefit of membership.

Shennan Circuit Gets Top Supplier Award

"Having a network of strong-performing suppliers that share our commitment to delivering exceptional quality and cost-effective solutions is essential to meeting our customers' needs," said Wayne Flory, vice president, material & supply for Rockwell Collins. "Shennan has been a strong-performing supplier since we started working with the company nearly ten years ago."

HDI Leads Rigid PCB Growth in 2014

High-density interconnect was still a main engine of growth in rigid PCB field in 2014, and is expected to maintain the momentum in 2015. As mobile phone screens become larger, PCBs for mobile phones have to react accordingly. To ensure light weight and thinness of mobile phones, the demand for more advanced anylayer HDI increases tremendously.

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TIM'S TAKEAWAYS

The Utility Belt

by Tim Haag
INTERCEPT TECHNOLOGY

Back in school, I had planned on a career in music, specifically playing jazz clarinet or saxophone. But that didn't happen. Instead, I enjoyed a long career as a circuit board designer that eventually lead to my current career as a customer support and training manager.

Even though a career in music was never realized, many of the lessons learned during my musical training have helped me in this career. One of those lessons came from a grizzled old saxophone teacher who taught improvisational jazz. He drilled us on the basics of music: scales, chords, arpeggios, etc.

As he said, "You always want to have something in your pocket to pull from on those nights when you just aren't feeling as creative as usual." He was talking about having some basic jazz patterns to fall back on while improvising, but the same general concept can be applied in our industry: Make sure you have some good basic tools in your utility belt to help you out when you need them.

The utility belt is a great thing to have. Batman would be long dead without his, and Tim "The Tool Man" Taylor would be useless without his. But for a circuit board designer, a utility belt is equally important.

All of us at one time or another will have questions about the CAD system we use, and one essential tool to have in your utility belt is a list of people you can go to for help. At the top of this list should be your CAD system's friendly customer support staff (like me), so make sure that your company has current and up-to-date access to your CAD system's technical support.

I couldn't begin to tell you the many times that I have helped customers with a simple answer to a perplexing question. Just the other day I had a customer who was really stuck. He obviously knew our software well, but he was missing that one piece of information that he needed to break through the log-jam. I was able

Figure 1: What's in your toolbelt?

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to answer his question and with that he resolved his problem. I really didn't do anything too special for him, but my simple answer opened up for him a whole new direction that he could take, and that got him unstuck.

In the same vein, another important tool in your utility belt is a solid understanding of your CAD application. Knowing what you are doing when you hit the keyboard can save you lots of time and frustration, and will make you much more efficient at your job. Read the help manuals, seek out other users as mentors, spend time with the online tutorials, and even sign up for training if needed. And as you come up to speed on your design tools, be flexible and adapt to the process that your specific CAD application is designed for. Let me tell you from personal experience, it's extremely unproductive to berate the support staff because you were expecting the "View All" menu command to be in a different location than where it actually is. Using the excuse "Well, that's the way my old CAD system worked!" isn't very helpful. Instead, get well acquainted with your system and become the super user that others will look up to for help.

"It's also important to have resources to help you with design questions. Perhaps you're stuck trying to lay out a circuit with unusual requirements, or you are unfamiliar with a new type of technology. It is always a good idea to have lot of different people available that you can go to for help."

It's also important to have resources to help you with design questions. Perhaps you're stuck trying to lay out a circuit with unusual requirements, or you are unfamiliar with a new type of technology. It is always a good idea to have lot of different people available that you can go to for help. Just recently I was trying to come up with a way to help a customer with a library process problem. The answer was right in front of me, but I was so focused on doing it a certain way that I never considered a different approach. A quick conversation with a co-worker turned on the light of inspiration for me that I needed to help this customer.

Staying current on design blogs, forums, application FAQs and other Q&A websites is also very helpful. And keeping up with different industry resources and design periodicals like this one is another great tool to have at your fingertips.

Here's another good tool to have in your belt: preparation. This may sound pretty basic, but I feel that it is perhaps the most important tool of all for a PCB designer. When I was designing and starting a new project, I took the time to go through the entire design and familiarize myself thoroughly with it. I researched the parts that I was going to use, I looked at the floor-planning that the engineer was expecting, and I prepped the design database with as much up-front information that I possibly could.

I have seen many other designers just jump in and start throwing things on the screen while I was still going through all the data. Sometimes those designers would pull way ahead of my work and they looked very impressive. But as time went by, those other designers would then start to re-work their board because they had made a mistake with library parts, or their rushed placement did not allow enough room for critical routing, or any one of a number of different reasons. I'm not saying that I'm the "be all, end all" of how to design, but I do know that my rate of re-work was much lower than other designers because I made sure that I was prepared for the job, up front.

Part of being prepared is also being alert so you don't do something that you'll regret later. When I was a kid we had a very underpowered lawn mower, and grass would always get backed up inside it. I would have to shut the mower off and pull the packed grass out of the exit chute every 25 yards or so. This got so annoying that after a while I would just dig the grass out with my hand while the mower was still running. You can see this one coming can't you? Yep. One day I stuck my hand in too far and one of my fingers found the spinning blade. Fortunately the mower was so weak that all it did

was jam my finger and split my fingernail. But I had gotten careless in my haste. As carpenters say, "Measure twice and cut once." Perhaps we could modify that advice to make it analogous to the PCB design community and then stick that in the utility belt as well.

And here's my last thought for handy tools to have in your utility belt: "If your CAD system can do it, make sure that you use it." Too often I have seen designers omitting helpful features or doing something manually when their CAD system already has these automated routines available. These functions are put into the tools to help you, so you should use them. For example, on the layout system that I support, Intercept's Pantheon, we not only have regular DRCs available but also ERCs and MRCs (electrical rules checking and manufacturing rules checking). These checks give the designer the ability to verify their design in the same way that fabrication and manufacturing vendors do. With this ability the designer has the opportunity to find problems specific to the manufacturing process before the design leaves their department. This is a new and different way of doing things for a lot of designers and unfortunately many avoid it. But it's there for a reason: to help eliminate errors, reduce board spins, save cost, and ultimately create a better design.

We probably won't ever get called upon to save Gotham City from the Joker, and hopefully none of us will ever try to enhance a riding lawnmower with a jet engine as Tim "The Tool Man" Taylor did, but a utility belt fully stocked with tools to help us with PCB design is a great thing to have, and may ultimately make the difference when we are really stuck.

As Tim Taylor would say, "Aaaaaaaarooohhh!"

PCBDESIGN

Tim Haag is customer support and training manager for Intercept Technology.

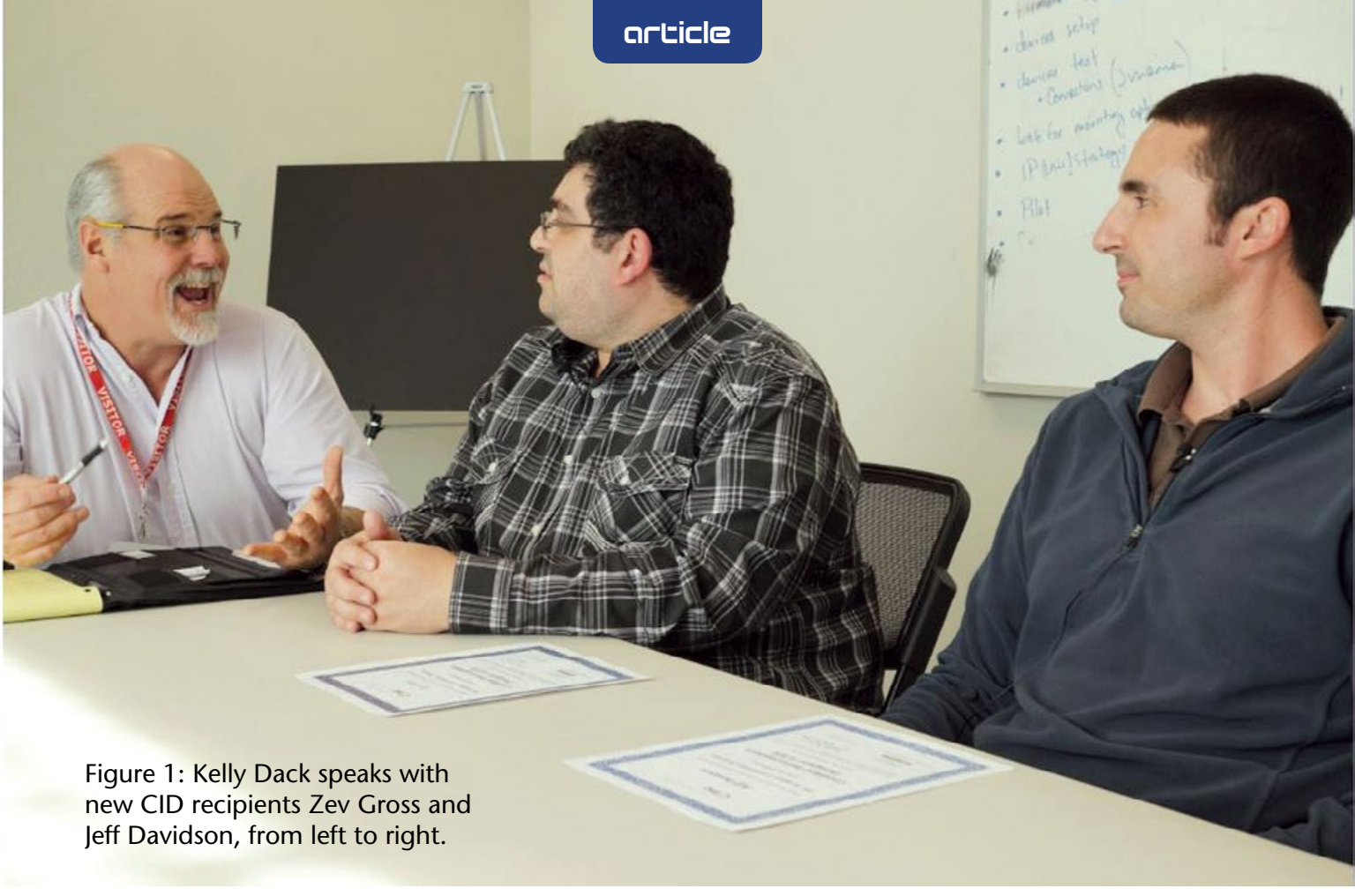

Figure 1: Kelly Dack speaks with new CID recipients Zev Gross and Jeff Davidson, from left to right.

Hunter's Two Newest CID Recipients Discuss Certification

I-Connect007 Guest Editor Kelly Dack spent time at Hunter Technology's Silicon Valley plant. He had the opportunity to sit down with two recent CID recipients, Jeff Davidson and Zev Gross, who completed Dack's CID training program. The two also discuss the benefits of achieving certification and their plans to take the CID+ advanced course.

Kelly Dack: *Thank you for the opportunity to visit Hunter Technology. And congratulations to you both for achieving IPC's Certified Interconnect Design certification. I enjoyed having you both in my class.*

Jeff Davidson: Thank you.

Zev Gross: Thank you, Kelly.

Dack: *Now, not many people get an opportunity to tell the world about this experience. What was it like going through the certification process?*

Davidson: Well, there was a lot of information in the book, but I thought it was pretty straightforward. And the materials are sent to us beforehand.

Dack: *Zev, what was it like for you? As one of our more vocal students in the class, you seemed to have a take on every concept that we discussed, and it blended right in with where we were going. As an instructor, it was helpful to have your commentary in the class.*

Gross: First of all, the feeling is great to have certification in our field, which is typically un-

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common. Thank you for teaching us. The commentary stems from the fact that I come from a lot of different environments, both here and abroad, which give me a take on many of the issues that we were learning about.

***Dack:** What was the purpose of obtaining your CID certification? Was it based on credibility, or the challenge, or what?*

Davidson: I think having that certificate is a sign of credibility, especially with IPC being the industry standard.

***Dack:** Here's the way it might be explained for some: We just walked through your plant, and I noticed that, at every step of the way in the PCB assembly process, things are checked and measured and verified. Isn't the CID program a way of measuring the capability or the learning and the knowledge of the designer?*

Davidson: Yes, absolutely. Our designs have got to be able to go through all those steps and they must pass all their measurements and verifications, so it's nice to make sure that we're doing it correctly, so that the people down the line can do it correctly.

***Dack:** There is also an advanced CID+ class. Do you both plan to take the advanced certification?*

Davidson: Absolutely, I do.

Gross: Yes, I do as well. We want to get more familiar and in-depth with our field and terminology, which are more standardized than what we typically do. It's nice to have it on paper. There are many benefits for us as designers.

***Dack:** In the CID+ program, many more concepts are built on from the basic course. You'll be going into the high-speed areas and much more, so look forward to that. Along with the class, it was part of the prerequisite to sign up and check out the IPC Designer Council, which seems to be revving up across the country. Have you done that?*

Gross: Yes, we both have signed up with the Silicon Valley chapter. We're looking forward to seeing both of our names on the CID Certified section.

***Dack:** And attending your first meeting, hopefully soon.*

Gross: Yes, definitely.

Figure 2: Kelly Dack speaking with Zev Gross.

***Dack:** Well, I'd like to again congratulate you both and thank you so much for having me to your plant. Your design area is top notch. In fact, I made a promise that I wouldn't keep you too long because you've got a customer waiting back there and he is fully expecting high-quality CID design right now, isn't he?*

Davidson: Exactly Thank you, Kelly.

Gross: Thanks, Kelly.

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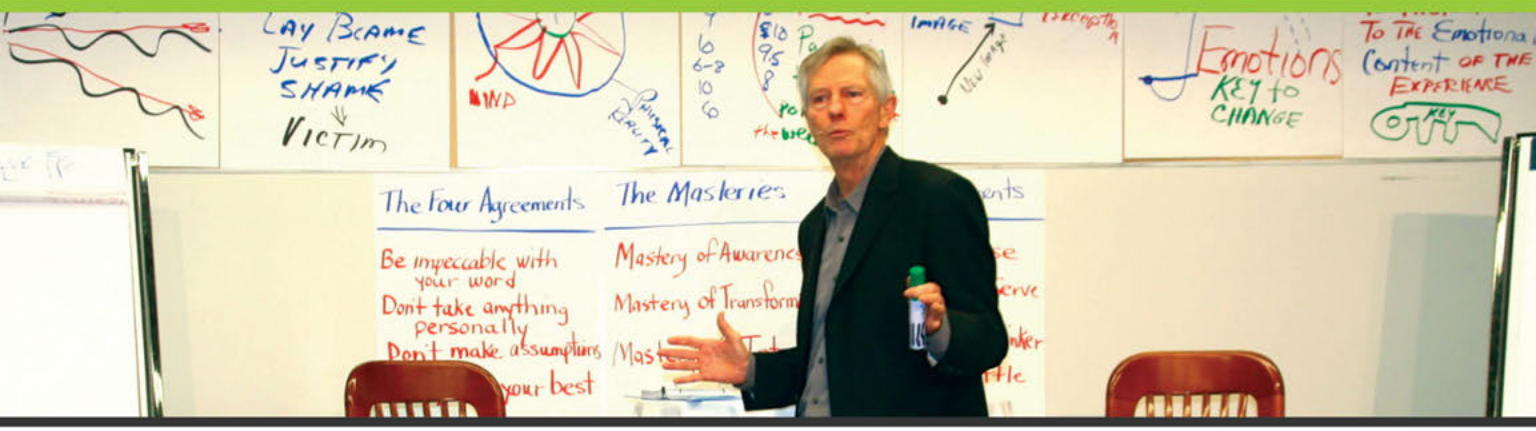

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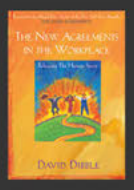

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News Highlights

Sanmina's Costa Mesa Facility Earns AS9100C

Sanmina's PCB facility in Costa Mesa, California, has received AS9100C certification, allowing the company to manufacture PCBs for aerospace and defense electronics equipment.

Shennan Circuit Gets Top Supplier Award

"Having a network of strong-performing suppliers that share our commitment to delivering exceptional quality and cost-effective solutions is essential to meeting our customers' needs," said Wayne Flory, vice president, material & supply for Rockwell Collins.

Ventec Increases Focus on Aerospace Market

Ventec Europe continues its investment in the establishment and maintenance of meticulous aerospace-standard cleanliness in the pre-preg handling areas of their state-of-the-art distribution center in Warwickshire, United Kingdom.

Electrochemicals Celebrates 50 Years of Service

Leo Linehan, VP & GM Electronic Chemicals states, "This is an exciting time in the electronics industry as we see significant technological advances, miniaturization, and the need for enhanced reliability. OM Group is committed to meeting these needs."

Automation Drives Military Ground Robot Market Growth

ReportsnReports.com adds Military Ground Robot Mobile Platform Systems to Engage Terrorists: Market Shares, Strategies, and Forecasts, Worldwide, 2015 to 2021 industry research report that says the new military is dependent on flexibility and early response.

Park Electrochemical Adds New Technical Sales Engineer

Park Electrochemical Corp. announced the appointment of Mike Kallbrier as a technical sales engineer of Park Electrochemical Corp. In this position, Mr. Kallbrier will be responsible for sales of Park's aerospace and electronics product lines in the Western territory of the United States. Mr. Kallbrier will report to Robert Nurmi, Park's VP of sales—Americas.

Isola Qualifies FTG to Use I-Speed Materials

Bradley C. Bourne, president and CEO of FTG, stated, "We are pleased to have Isola recognize FTG for our outstanding manufacturing capabilities using I-Speed materials. We look forward to continuing with the certification program in qualifying additional Isola materials."

Companies See Significant Benefit in Nadcap Accreditation

More than one in five companies pursues Nadcap accreditation to improve quality, according to a recent poll conducted by the Performance Review Institute (PRI). Of those that responded, 21% cited "improving quality" as a key driver behind their decision to obtain Nadcap accreditation, with 19% indicating that they pursued Nadcap accreditation in order to attract new business.

UAV Market Hurt by Cut in Defense Budgets

The global economic slowdown has reduced the defense budgets of most leading spenders in the world, including the US, France, Germany and the UK. Cuts to military expenditures have led to the cancellation and indefinite delays of various UAV projects and a detrimental impact on the growth of the UAV industry.

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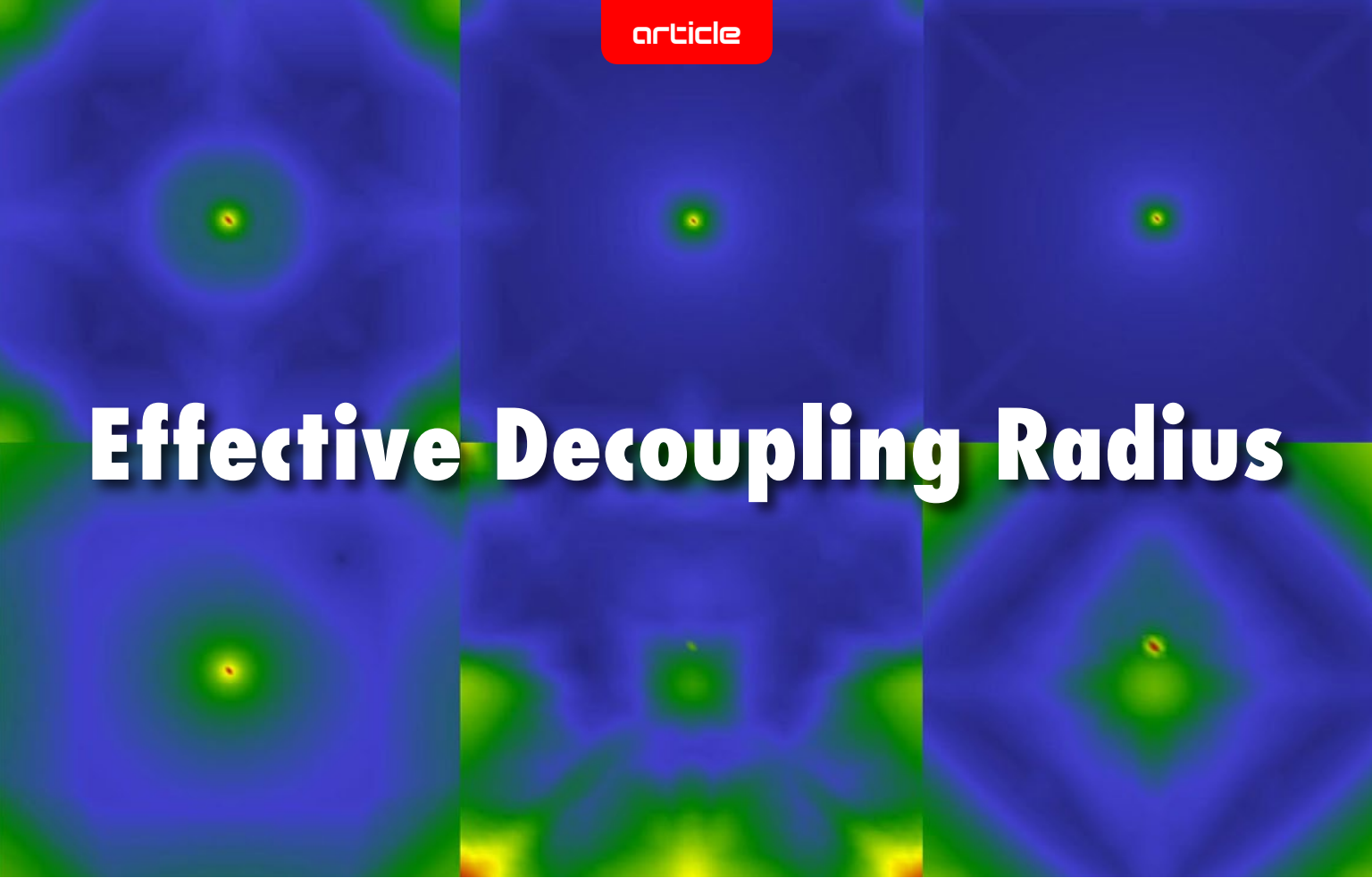

Effective Decoupling Radius

by Kirk Fabbri
KSPT ENGINEERING CONSULTING

Power distribution networks (PDN) are becoming an important topic. Many engineers are finding that properly designing the power supplies and providing adequate decoupling for devices is a challenge, especially since devices are switching faster and dimensions are shrinking. Engineers often focus on discrete decoupling capacitors placed local to switching devices in hopes of providing the required capacitance for these high current demands. One of the more overlooked items of the power distribution system is the PCB, and how it contributes to the power distribution system's ability to decouple the switching devices. The following experiment will outline a basic principle that should be in mind when designing a stack-up and PDN.

Basic PDN Model

A basic PDN includes the voltage regulator model (VRM), the discrete decoupling capacitors, the PCB, and any on-die capacitance formed on the IC or device. Each one of these components could be written about separately, but it is the PCB that will be focused on; specifically the effective decoupling radius.[2]

When a device is active, it will require current. The type of device (process size), load on the I/O drivers, and how the device is operated, all have an effect on the current required, among others. When the device demands current, it flows through the complex impedance of the PDN and causes a ripple voltage to appear. This transient current is drawn from a variety of sources including the local on-die decoupling capacitance, the PCB, the discrete capacitors, and finally the VRM.[1] The edge rate of this switching current is extremely important when trying to calculate how effective the PDN will be in suppressing the ripple voltage. The switching edge can be dissected into a variety of harmonic sine waves at decreasing amplitude described by a Fourier series equation. It is here that we discover the importance of the PCB, and its role in the PDN.

The simplest way to represent a PCB is a distributed RLC network. Capacitance is formed by the copper layers and the dielectric between them. Inductance is formed by the loop area between the layers, and the resistance is formed by

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EFFECTIVE DECOUPLING RADIUS *continues*

the cross sectional area and length of the copper planes. From equation 1 below, capacitance can be calculated where C = capacitance in pF, eo = permittivity of free space (0.225pF/inch), er = dielectric constant, A = area (in^2), and S = spacing between the planes (inches)[3]. Here we see that the best way to increase the capacitance is by decreasing the spacing between the planes or increasing the area of the metal layers.

According to Ott[2], the effective radius in which capacitance can be utilized is calculated by the equation below, where r = radius in inches, t = rise/fall time of switching edge (ns), and er = dielectric constant. By looking at this equation, we can conclude that the effective area (r) decreases when either the switching edge becomes faster (t decreases), or the dielectric constant of the medium increases.

$$C = \frac{eo * er * A}{S} \quad (1)$$

$$r = \frac{12 * t}{\sqrt{er}} \quad (2)$$

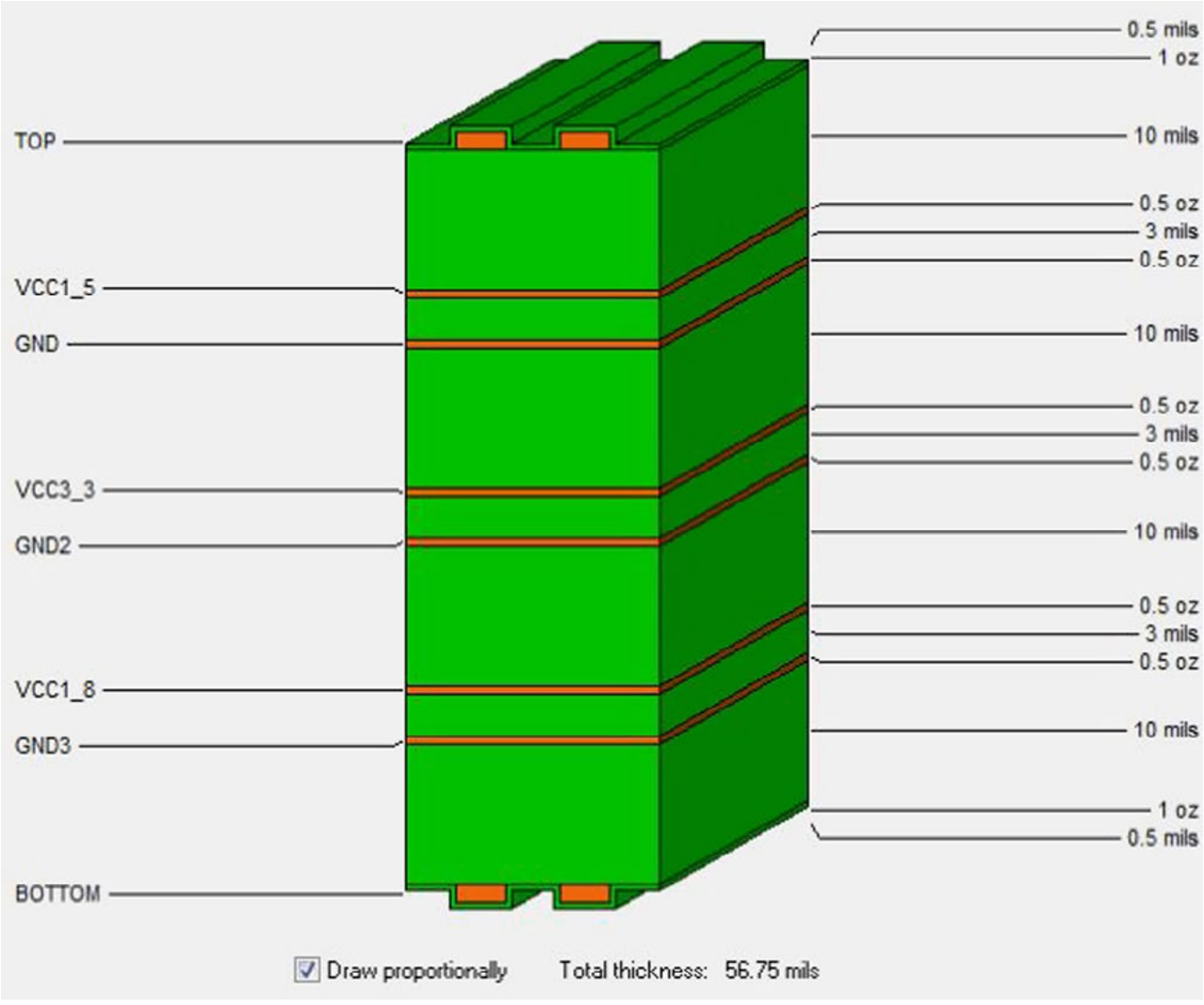

Figure 1: The baseline stack-up for Experiment 1. Power plane pairs are spaced 3 mils apart.

Experiment 1: PCB Area Larger than Required Effective Area.

This first experiment will outline a situation where the available power plane area is larger than the effective radius calculated in Equation 2. Shown in Figure 1 is the stack-up used for this experiment. It is an eight-layer board with a top/bottom layer, three ground planes, and three planes at different supply voltages (1.5, 1.8, and 3.3V). The dielectric thicknesses between the power/ground planes are 3 mils (0.75 mm), which is a fairly popular size.

Shown in Figure 2 is a simple PCB created in Mentor Graphics HyperLynx with an area of 16 in^2 (4 x 4 inches), where U1.1 represents the VRM and U2.1 represents the current sink. The current sink is setup to draw 250mA with rise/fall times equal to 250ps. In this baseline case, both the current sink and VRM are connected to layer 2 (VCC1_5), and referenced to all three GND layers. The small yellow circles represent stitching vias used to connect all GND layers together. Shown in equation 3 below is the calculation of the effective radius yielding an area of 6.60 in^2, which is considerably smaller than the total PCB area (16 in^2).

$$r = \frac{12 * 0.250ns}{\sqrt{4.3}} = 1.45\ in \quad (3)$$

Using this effective area, we can calculate the effective capacitance as 2.13nF, shown in equation 4 below. In this example, the capacitance is calculated based on a single VCC1_5 and GND plane pair (layers 2 and 3) neglecting the holes from the stitching vias.

Shown in Figure 3 are the results of this baseline simulation. The peak noise voltage is found to be 91.4 mV located at the current sink.

$$C = \frac{(\frac{0.225pF}{inch}) * 4.3 * 6.60}{0.003} = 2.13nF \quad (4)$$

Experiment 2: Further Increasing the PCB Area

Oftentimes, simply increasing the PCB area is thought to have a positive effect on the noise voltage since the capacitance is also being in-

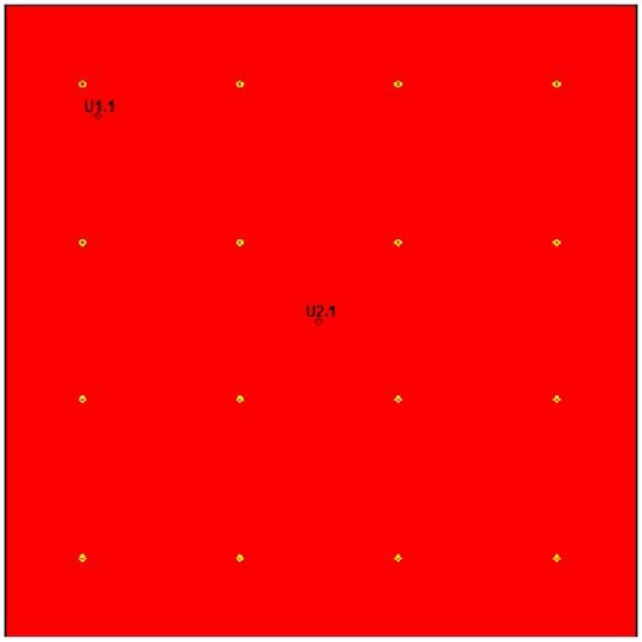

Figure 2: The example PCB with one current sink (U2.1) and one VRM (U1.1). The small yellow circles represent stitching vias used to connect the different ground layers together.

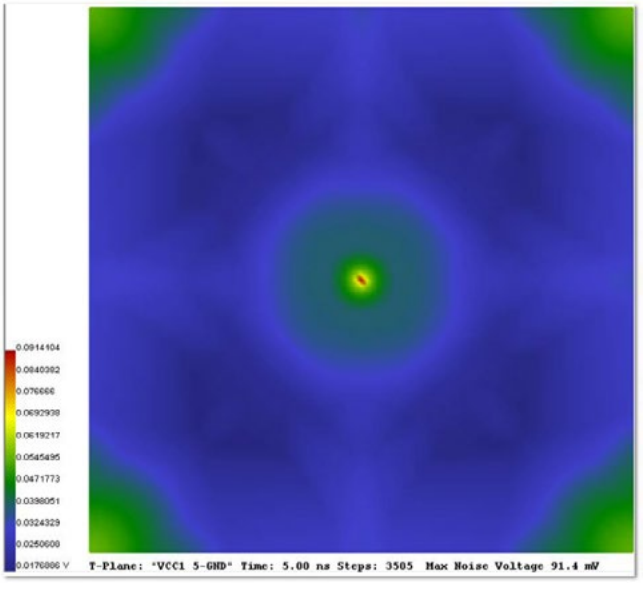

Figure 3: Showing the results of the baseline simulation connecting the VRM and current sink to layer 2 (VCC1_5). Peak noise voltage is 91.4 mV at the current sink.

creased. After running the simulation on this experiment, we will see that this isn't necessarily the case, as it depends on whether or not the plane area is already larger than the effective radius calculated in Equation 3 above.

The PCB size is now made 64 in² (8 in x 8 in) with all other factors remaining the same. The results of the simulation are shown in Figure 4 below with a noise voltage equal to 87.1mV. It's fairly easy to see that the additional capacitance of the plane isn't significantly improving the noise voltage, as its contributions are outside of the effective area based on the rise/fall times of the current sink.

Experiment 3: Increasing the Dielectric Constant, Changing the Layer Spacing

In Experiment 2, we found that increasing the power plane size outside of the effective area/radius had little to no effect on the noise voltage created at the current sink. What if we were to increase the capacitance of the power plane by either increasing the dielectric constant or by decreasing the spacing between layers? Either or both of these factors would certainly increase the capacitance of the plane pair as well.

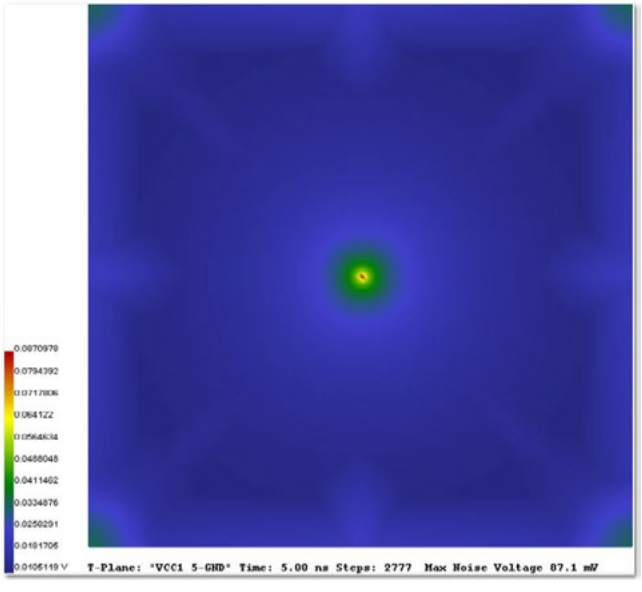

Figure 4: Showing the results of experiment 2 above. The area of the PCB (64 in²) is now much larger than the calculated effective area (6.60 in²), yet the noise voltage (87.1 mV) is almost unaffected from the previous simulation (91.4mV).

First, let's increase the dielectric constant of the material. What if we were to increase it by something much larger, say 20? After altering the stack-up to represent a dielectric constant of 20 on all layers (besides the solder mask on the top/bottom layers), the simulation was run and resulted in a peak noise voltage of 72.3mV. At first glance, simply looking at Equation 1 for capacitance indicates that we might expect to see a larger difference in noise voltage when using a higher dielectric constant. To answer this question, the new effective radius using a dielectric constant of 20 is calculated to be 0.67 in, as shown in Equation 5. This radius results in an effective area of only 1.41 in², which by comparison, is much smaller than 6.60 in² as it was in the original experiment.

$$r = \frac{12 * 0.250ns}{\sqrt{20}} = 0.67\ in \quad (5)$$

What we see happening here is very interesting. In this case we wanted to increase the total capacitance of the plane pairs in attempt to further suppress the noise voltage. By increasing the dielectric constant, we effectively shrink the effective radius, and thus the area that the current sink can effectively use. The effective capacitance from the original dielectric constant (4.3) is approximately 2.13nF, whereas the new capacitance formed by increasing the dielectric constant to 20 is calculated as 2.13nF also! Running the simulation on this setup yields a noise voltage of 72.3mV, which is improved slightly over 87.1mV. The results of the simulation are shown in Figure 5.

It is important to note that there are more complex interactions at work here than just the capacitance of the plane. Modal resonances, spreading inductance, etc., also play a part, which are accurately captured by the field solver.

Experiment 4: Decreasing the Spacing between the Planes

In this experiment, we will decrease the spacing between the planes to something very small—1 mil. Although these materials are available, they are very expensive and possibly

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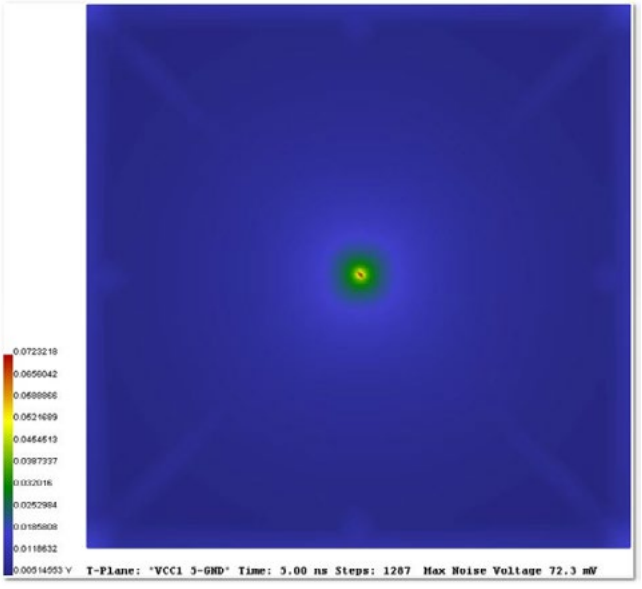

Figure 5: Results of the simulation for Experiment 3. The dielectric constant was increased to 20 for all layers. The noise voltage at the current sink has only dropped 14.8mV from the same setup with a normal dielectric constant of 4.3.

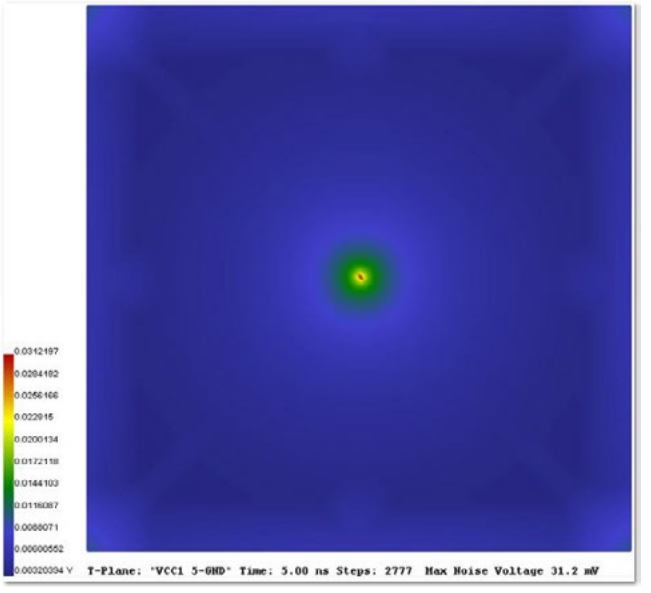

Figure 6: Results of the simulation for Experiment 4. The dielectric constant is 4.3, with the spacing between layers 2 and 3 = 1 mil. The peak noise voltage is found to be 31.2mV, substantially improved over the 87.1mV found in Experiment 2.

unavailable depending on the fabricator used. In this experiment, it is done to see if there are drastic effects on the results of the noise voltage. Additionally, the dielectric constants are set back to their original values of 4.3, and the board is made large (64 in^2). The capacitance of this setup is calculated as 6.39nF, and the results of the simulation are shown in Figure 6. Notice that the noise voltage is substantially improved over the previous cases, and even more so than the high dielectric case.

What if we set the board size back to 16 in^2 (4in x 4 in) as it was in experiment 1? After running this simulation, the noise voltage was found to be 32.8mV, consistent with what we thought might happen based on our previous experiments and intuition. The additional capacitance formed by increasing the board by 4x the original size has made almost no difference in the total noise voltage because it is outside of the calculated effective area.

Experiment 5: Increasing the Number of Power Planes

In the previous experiments, we have focused on what could be done when using a single power plane pair as the main source of PCB capacitance. We have shown that increasing the size of the PCB outside of the effective area has little effect on the noise voltage. Likewise, we have witnessed that increasing the dielectric constant also has little effect on the noise voltage as it offsets the added capacitance by shrinking the effective radius. What if we were to use two separate plane pair structures, both at a physical size that is similar to the size of the effective radius?

Running this experiment requires a change to the way the current sink and VRM are setup in the simulation. The stack-up is altered so that layers 6 and 7 are also connected to VCC1_5. Now we will have two cavities forming capacitance, both within the effective radius of the current sink. In a simplistic manor, the capacitance should double, but there is also inductance associated with not only each plane pair cavity, but also between the two cavities. Additionally, we must stitch the planes together with vias for both the GND layers and the newly created VCC1_5 plane on

layer 6. The dielectric constant is set back to 4.3 and the spacing is set to 3 mils between plane pairs. Figure 7 shows the results of the simulation having a peak noise voltage of only 39.1mV at the current sink.

What happens if we shrink the spacing between the power planes to 1 mil? From our previous experiments we can take an educated guess that the capacitance should increase and it should improve our noise voltage. Running this scenario concludes this and shows a peak noise voltage of only 15.4mV!

You may ask when a scenario like this is appropriate. Consider a memory system such as DDR2. Often the manufacturer will specify that byte lanes be routed on different layers for crosstalk, timing, trace impedance, and other constraints. In a system like this you will likely be forced to use multiple split planes for your PDN to accommodate other devices as well. In a system like DDR2, it makes sense for all of your signals to use either GND or a 1.8V power plane as a reference (return) plane since this is the nominal power loop where the current is drawn from. Using a reference plane that is not in the nominal current loop (say 3.3V) may not be a good choice. In this situation, the plane that is 3.3V could be split and connected to 1.8V in the area where the DDR2 nets are routed. This way the signals are referencing a power plane (or GND) that is in the nominal power loop and providing additional capacitance for the switching currents. One still needs to calculate the effective radius of the memory system by simulating/calculating the edge rates of the system. From here, the designer can grasp an idea of how large the plane area needs to be. Obviously, the placement/routing area of the memory system need to be considered as well when deciding where to place splits. Always extend the plane so that signals aren't routed over splits whenever possible, even if the plane area is larger than the calculated effective area dictates.

Experiment 6: Board Area is Smaller than the Effective Area

Our previous experiments only looked at the board when it was either similar or much larger than the effective area of the current sink. So what if the area of the PCB is smaller, or much smaller than the calculated effective area? What are the best solutions in this case?

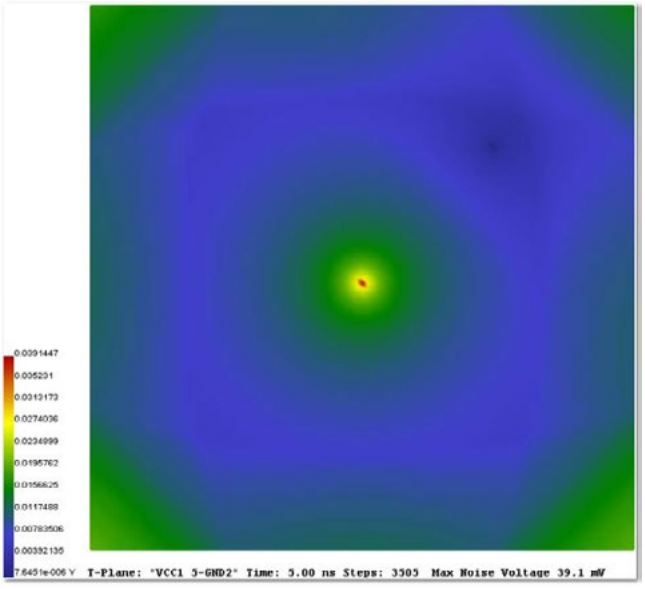

Figure 7: Showing the results of Experiment 5. Layer 6 is now connected to layer 2 by stitching vias to increase the effective capacitance connected to the current sink. Both layers 2 and 6 are sized so that they are similar to the calculated effective area. The peak noise voltage is only 39.1mV.

For this experiment, we will use the same current sink properties yielding an effective radius of 1.45 in and an area of 6.60 in^2. However, the board area will be considerably smaller—2 in^2 (1.41 x 1.41 in). The stack-up has been set back to 3 mil spacing, dielectric constant of 4.3, with the current sink and VRM connected to just layer 2 as previously. Figure 8 shows the results of the simulation. Here we see the peak noise voltage is worse at the edges of the board (129.4mV) versus at the current sink (106mV). The board geometry is also playing a role as there are modal resonances occurring differently than with the larger board.

We can conclude that both decreasing the dielectric spacing between the layers and using additional planes will decrease our noise voltage by increasing the capacitance of the system. What about increasing the dielectric constant to something higher?

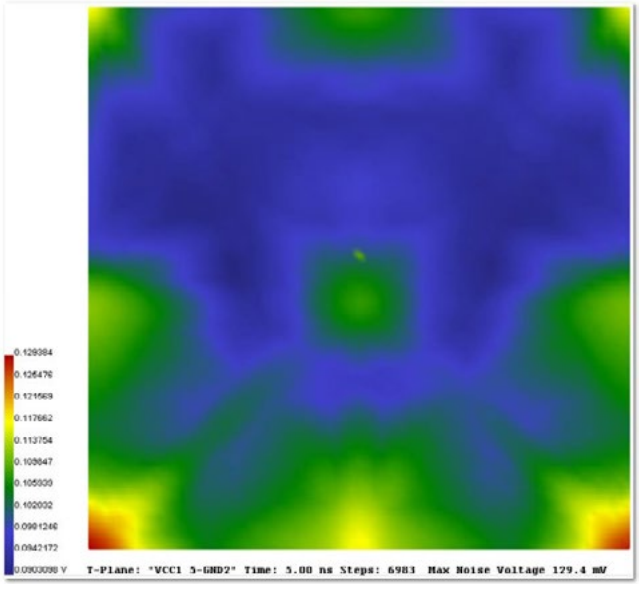

Figure 8: Results of Experiment 6. The total board area is considerably smaller than the effective area. The peak noise voltage is 129.4mV located at the edges whereas the voltage at the current sink is approximately 106mV.

Recalling the earlier experiment, increasing the dielectric constant negatively affected the available capacitance by shrinking the effective radius, and thus the area. This still very much holds true, but if the plane area is smaller than the effective area, then it isn't being fully utilized by the current sink. In this case, decreasing the effective area by increasing the dielectric constant will increase the available capacitance and should lower the noise voltage.

One has to calculate how much the dielectric constant can be increased, as to fully utilize the available plane area, but not so much as to shrink the effective area below the PCB plane area. In our case, the plane area is 2 in^2, which gives a capacitance of 645pF when the dielectric constant is 4.3 and the spacing is 3 mils. Since the area is 2 in^2, the radius (r) must equal 0.797 in. Solving Equation 2 for the dielectric constant using this radius yields ~ 14, which tells us we can increase the dielectric constant all the way up to 14, shrinking the effective area to match the current sink. By doing this we can fully utilize the plane area in a way that maximizes the capacitance and lowers the noise voltage.

Calculating the capacitance for both cases yields 645pF for the standard dielectric constant of 4.3 and 2.12nF for the high dielectric case. Running the simulation with the dielectric constant = 14 for all power plane layers is shown in Figure 9. Right away we notice that the noise voltage at the current sink hasn't changed much (delta of ~12mV), but the noise voltage at the plane edges has decreased by 66mV. In this case local decoupling of the current sink should also help suppress the noise voltage.

As a final thought, we could decrease the spacing and add additional plane pairs to increase the capacitance of the PCB. Simply changing the plane pair spacing to be 1 mil yields a noise voltage of only 22mV at the edges and 33.5mV at the current sink. Adding in an additional layer and leaving the spacing at 3 mils yields a noise voltage of 39.3mV at the current sink and 23mV at the edges of the PCB. The best scenario for this experiment is to change the power plane spacing to 1 mil as well as add an additional layer when using the high dielectric material. In this case the noise voltage simulates as only 15.5mV at the current sink and 8.5mV at the PCB edges.

Conclusions

Designing a stack-up and PDN can be a difficult task as there are many factors to consider for proper performance. Often times mechanical, thermal, and cost constraints impact the number of layers, the materials, and the amount of time that can be spent analyzing the design. It is also important to note that real designs have many complex current sinks, with many different dynamic characteristics. A traditional method of estimating these currents is to simulate the I/O of a device(s) and look at the driver I/O current spectrum to better understand the switching activity of these devices[1]. From this frequency spectrum, one can gain a better understanding of the load dynamics, and how to gauge the effective radius. With all simulations, it isn't an exact science. Sometimes, the most important thing you can find out is what scenarios yield the greatest impact given the amount of information available.

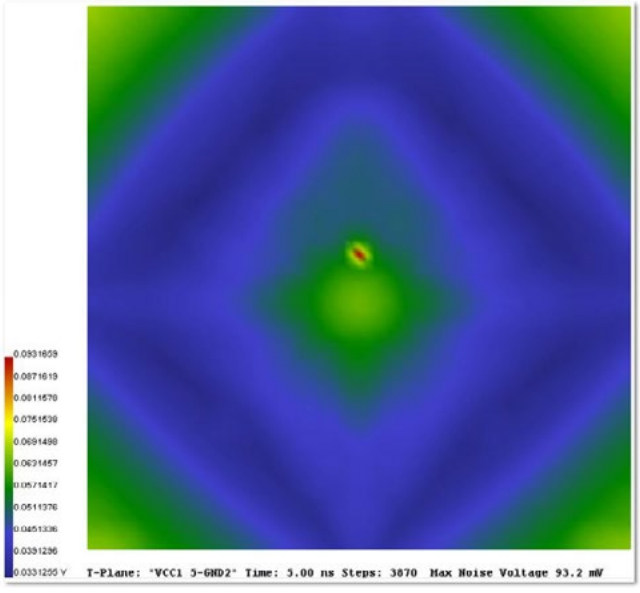

Figure 9: Showing the results of Experiment 6 when adjusting the dielectric constant higher. The peak noise voltage has decreased near the corners to 66mV, but only to 93.2mV at the current sink.

Important Points to Remember

- The dynamic characteristics of the current sink or load determine the effective area in which the capacitance of the PCB can be utilized.
- In the case where the PCB is much larger than the calculated effective area, high dielectric materials are of minimal impact in noise voltage suppression. Better performance is achieved by increasing capacitance either by minimizing power plane spacing, or by increasing the number of plane pairs attached to the current sink.
- In the case where the PCB is larger than the calculated effective area, further increases in plane area outside of the effective radius/area also have minimal impact on performance.
- In the case where the PCB is smaller than the calculated effective area; increasing the capacitance by using higher dielectric constant materials can improve noise voltage performance. However, similar, if not better results are achieved by decreasing the spacing or adding additional plane pairs.
- Decreasing the plane pair spacing not only increases the capacitance but also decreases the inductance of the structure.
- The PCB is only one part of a PDN. The VRM, discrete decoupling capacitors, chip package, and on-die capacitance are also very important in achieving the desired performance.

PCBDESIGN

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2. Electromagnetic Compatibility Engineering, by Henry W. Ott.
3. Signal Integrity: Simplified, by Eric Bogatin.

Kirk Fabbri is owner of KSPT Engineering Consulting LLC and Electrical Engineer for L-3 Communications—Avionics Systems. He can be reached at kirk.fabbri@L-3com.com.

Driverless Cars to Renovate Automotive Industry

The most recent Mercedes automatic car looks just like a car on the outside but like a lounge from the inside. The car, based on the concept F 015 "Luxury in Motion" showcased at the Consumer Electronics Show, is totally self-driving but has a brake and steering wheel if one wants to drive it manually.

Tesla, Audi, Google and a number of other companies are trying to create their own adaptations of driverless cars, satisfying the predictions that they will be a reality on the roads possibly by the end of this decade.

In fact, all the technology required for a self-driving car is already present. Existing features such as self-parking preview and adaptive cruise control show what a fully automatic car can do.

TOP TEN

Recent Highlights from PCBDesign007

1 PCB Designer and Instructor Kelly Dack Joins EPTAC

Kelly Dack, one of the electronic industry's most consummate printed circuit board designers, industry supporters and interviewer of the trendsetters in the market, has joined EPTAC Corporation to support the growth efforts of EPTAC's IPC Designer Group, led by Gary Ferrari.

2 Mentor Graphics Debuts Xpedition Package Integrator Flow

The new Package Integrator flow allows design teams to realize faster and more efficient physical path finding and seamless tool integration for rapid prototyping, right to the production flow. This solution ensures that ICs, packages and PCBs are optimized with each other to reduce package substrate and PCB costs.

3 Intercept Technology Launches New Website

Intercept customers can also make special use of a new, authorized access section devoted specifically for them. The new section includes the latest software releases, a continually updated Knowledge Base complete with all documentation across products and services, an Intercept User Forum and an easy to use customer request page.

4 Zuken Expands E3.series Reseller Network in N.A.

Zuken has expanded its E³.series reseller network in North America with the addition of CAM Logic. CAM Logic is a leading provider of PLM solutions and 3D engineering software and services.

5 Azitech to Host Seminar with Rick Hartley May 5-6

This two-day seminar in Copenhagen, Denmark, will feature Richard Hartley. The signal integrity guru will focus on issues PCB designers and engineers need to know about to prevent problems with noise, EMI, and signal integrity. Moreover, attendees will learn how to deal with crosstalk and grounding problems in high speed digital and mixed signal designs.

6 Zuken Offers PCB Reference Design for Intel IoT Devices

Intel and Zuken are engaged in a technical partnership working to address convenience improvements for designs in Zuken PCB design environments that use Intel platforms. This delivery of PCB reference designs forms just one part of these efforts.

7 Mentor Offering Training in Atlanta, Tampa in April

The agenda will include a description of the "electrical signoff" problem, and an overview of the HyperLynx tools that address the signoff requirements. Several short demos will show how easy-to-use and effective the HyperLynx virtual prototyping tools can be. The training will take place in Atlanta on April 14 and Tampa on April 16.

8 Pulsonix Continues Global Growth with the Appointment of 3D Tronic

This announcement continues Pulsonix EDA software's goal of global expansion. 3D Tronic boasts a wealth of experience in the EDA industry and this experience will act as a bi-directional synergy for both customers and the EDA tool alike.

9 DesignCon 2015 Names Best Paper Awards Winners

DesignCon has announced the winners of the Best Paper Awards from its 2015 program. The awards were divided into four categories: Modeling & Simulation, High-Speed Signal Design, Power Integrity & Signal Integrity, and Test & Measurement.

10 Mentor Graphics Launches New HyperLynx SI/PI

Mentor Graphics Corporation has released the newest version of the HyperLynx Signal Integrity/Power Integrity (SI/PI) tool for high-speed PCB designs. HyperLynx addresses high-speed systems design problems throughout the design flow, starting at the earliest architectural stages through post-layout verification.

events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out *The PCB Design Magazine's* event calendar.

South East Asia Technical Training Conference on Electronics Assembly Technologies 2015
April 14–16, 2015
Penang, Malaysia

SMTA Atlanta and Designers Roundtable
April 15, 2015
Duluth, Georgia, USA

NEPCON China 2015
April 21–23, 2015
Shanghai, China

Printed Electronics Europe 2015
April 28–29, 2015
Berlin, Germany

Graphene and 2D Materials Europe
April 28–29, 2015
Berlin, Germany

Internet of Things Applications Europe 2015
April 28–29, 2015
Berlin, Germany

Wearable Technology Europe
April 28–29, 2015
Berlin, Germany

SMT Processes Certification
April 28–30, 2015
Kokomo, Indiana, USA

IMPACT 2015: IPC ON CAPITOL HILL
(IPC Members-only)
April 29–30, 2015
Washington, DC, USA

Michigan Expo & Tech Forum
May 5, 2015
Livonia, Michigan, USA

Oregon Expo & Tech Forum
May 5, 2015
Beaverton, Oregon, USA

Puget Sound Expo & Tech Forum
May 7, 2015
Bellevue, Washington, USA

Wisconsin Expo & Tech Forum
May 12, 2015
Milwaukee, Wisconsin, USA

IPC Technical Education
May 13–14, 2015
Fort Worth, TX, USA

International Conference on Soldering & Reliability 2015
May 19–21, 2015
Markham, Ontario, Canada

Toronto SMTA Expo & Tech Forum
May 21, 2015
Markham, Ontario, Canada

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ADVERTISER INDEX

Candor Industries..... 39
Dibble Leaders..... 49
Downstream Technologies..... 21
Dymax..... 37
Eagle Electronics..... 7
EMA/EDA Design Automation..... 11
In-Circuit Design Pty Ltd..... 3
Intercept..... 47
IPC..... 53
Isola..... 5
Mentor..... 29
Miraco..... 43
Multilayer Technology..... 27
Prototron..... 19
Pulsonix..... 17
The PCB List..... 2, 57
Rogers..... 41
Sunstone Circuits..... 13
US Circuit..... 31
Ventec..... 51

Coming Soon to *The PCB Design Magazine:*

May:
Controlled Impedance

June:
IPC Standards Update

July:
Supply Chain Management