

THE **pcb**
DESIGN
MAGAZINE

July 2014

**Multi-Site Concurrent
Design: Tips and Best
Practices**

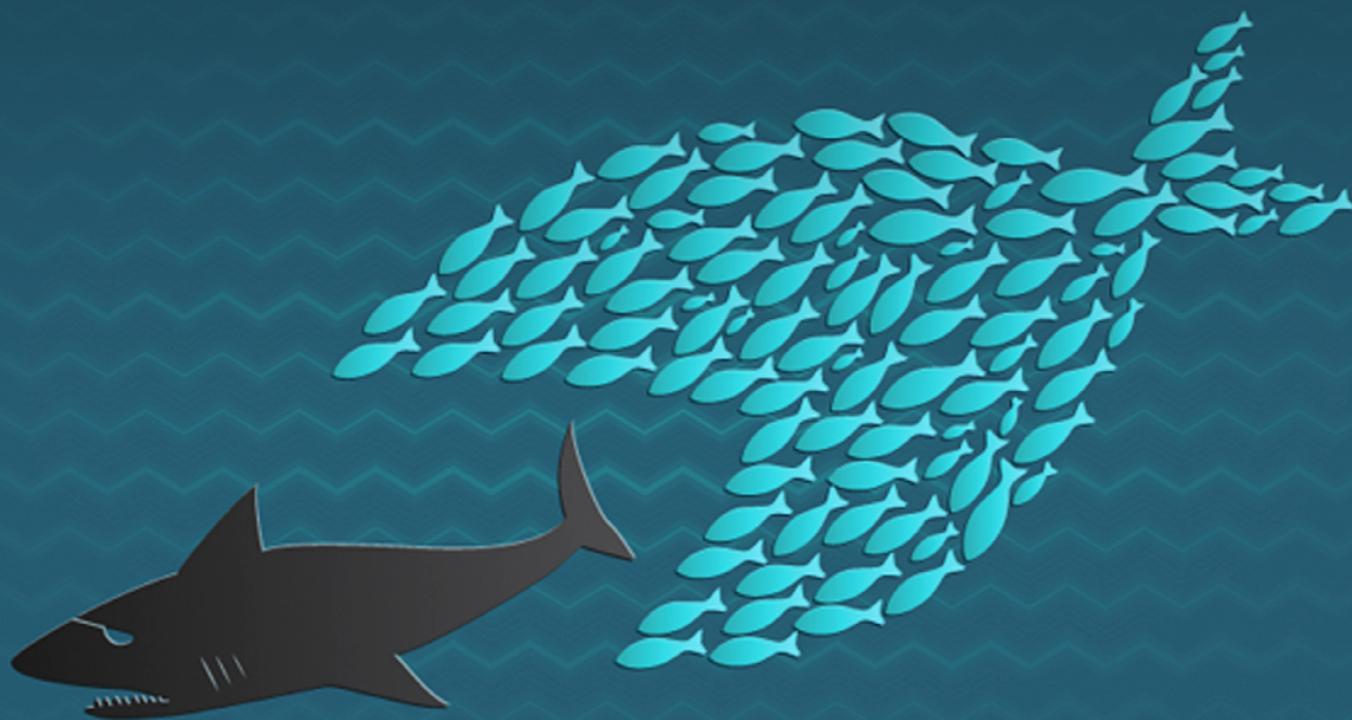
by Craig Armenti
p.22

Concurrent Design

by Barry Olney
p.34

AN  I-CONNECT  PUBLICATION

CONCURRENT DESIGN



Optimizing Collaboration for PCB Systems Design

Attack Big Problems with a Team

by David Wiens, page 12

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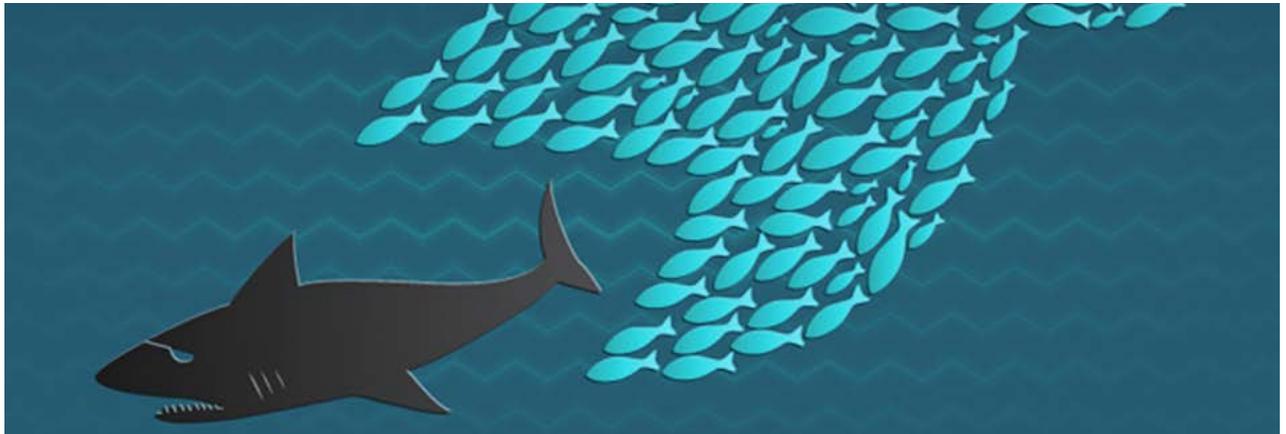
This Issue: CONCURRENT DESIGN

FEATURED CONTENT

Does it really take a village, or in this case, a design team? Each year, more PCB designers become part of concurrent design teams, groups that work “around the clock, around the globe.” This month, we deconstruct concurrent design with articles from expert contributors David Wiens, Craig Armenti, and Barry Olney.

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by David Wiens



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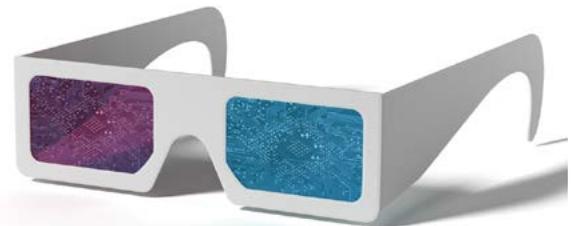
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FEATURE COLUMN

34 Concurrent Design

by Barry Olney





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CTE Z-axis (50 to 260°C)	2.90%	2.90%	2.80%	2.90%
T-260 & T-288	>60	>60	>60	>60
Halogen free	Yes	No	No	No
VLP-2 (2 micron Rz copper)	Standard	Standard	Available	Available
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Optimized Global constructions for Pb-Free Assembly	Yes	Yes	Yes	Yes
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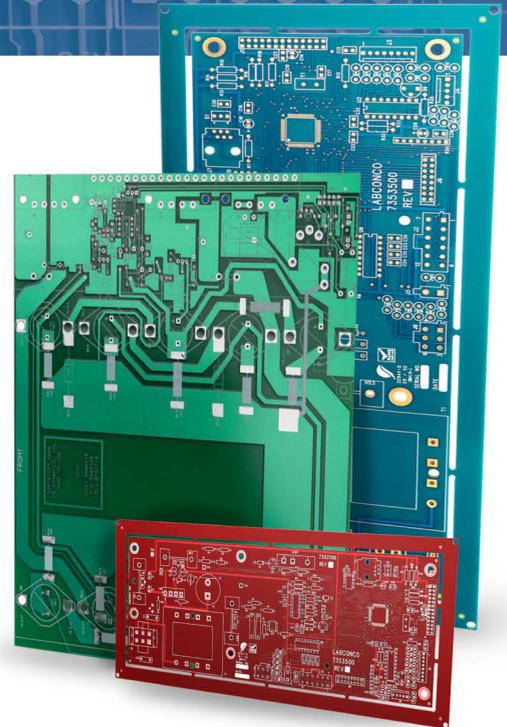


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Help Wanted: PCB Design Needs an Icon

by **Andy Shaughnessy**

I-CONNECT007

For years, veteran designers like Gary Ferrari, Bill Brooks, and the late Glenn Wells, just to mention a few, have been spreading the word to young people about PCB design as a viable career. Now, there are actual PCB design classes available at a handful of colleges, and PCB design is becoming more visible to the general public.

But it's still an uphill battle. Designers are retiring, and they just aren't being replaced. When was the last time you met a designer who was under 30?

Imagine what it's like to be a smart high school or college student—the kind of kid who would make a great PCB designer. You'd be interested in math and science, and you'd be considering a career in electronics. You'd be a little

bit off-grid, and able to harness that facet of your personality.

But you'd be getting deluged with information. You and your friends would most likely be interested in the “sexier” careers such as game developer or Web developer. Or you may have your sights set on being an electrical engineer. Not that there's anything wrong with that, of course.

After all, the EE is a known quantity; I imagine there will always be kids dreaming of being EEs. Why isn't it that way for PCB design?

If everyone knew how satisfying (and, often, profitable) a PCB design career can be, there would be waiting lists for every PCB design job. You know exactly what I mean: You may hate your boss, your company, and/or the EEs, but

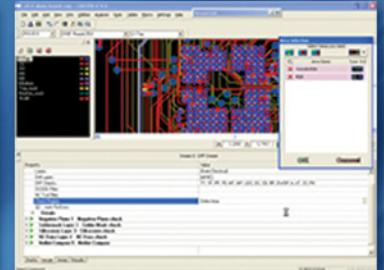
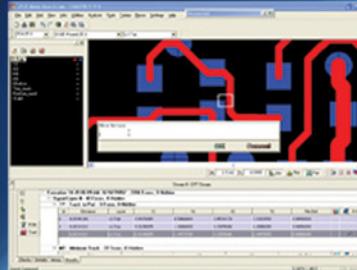


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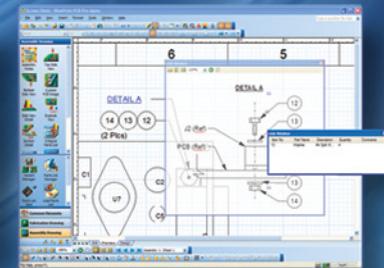
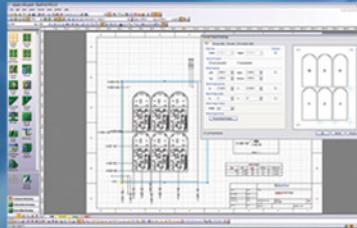
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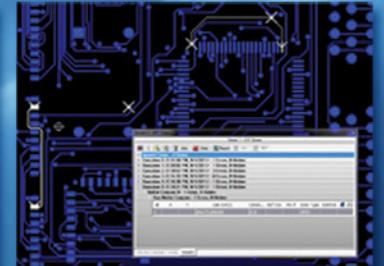
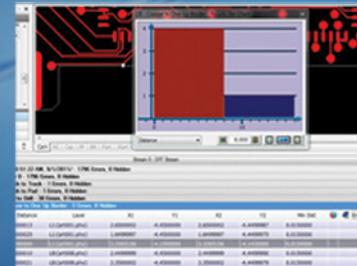
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HELP WANTED: PCB DESIGN NEEDS AN ICON *continues*

you love what you do. Not many people can say that.

We need to find a way into these kids' busy brains. What's our hook, our 10-second elevator spiel? PCB design suffers from an image problem. It has no image, and that's the problem.

PCB design needs an icon. Something that represents everything that design is about. Something we can show high school seniors and college students that would illustrate this career.

What idea encapsulates a designer's job? It doesn't have to be that complicated. We just need something to get kids thinking about PCB design.

Fabrication and assembly can be represented by the factory icon that we see in Skype and on the iPhone: a yellow building with a smokestack.

Assembly also has the robot. SMTA Atlanta has made the robot into a kind of icon. For the past couple of years, SMTA Atlanta has sponsored a robot competition to help get students interested in electronics and electronics assembly, and it seems to work. The students build remote-controlled robots and they compete for a prize. The robots have to pick up an object, move from point A to point B, etc. Then, while we're walking the aisles of the show, they're ramming their robots into each other and showing off for the adults. But it's clear that some of them want to be like us when they grow up.

They've built this robot, this cool thing that they can touch, something they can understand, and along the way they learn about high-tech manufacturing. It's not a stretch to see these kids becoming involved in robotics, capital equipment, or some other aspect of electronics assembly, especially when all these adult techies applaud for their favorite robots. The

robot is a good path into a student's cluttered mind. It's a futuristic icon that kids can hang their sideways baseball caps on.

But what is PCB design's icon? It's just tough to illustrate PCB design—ask anyone who has ever tried for days to come up with a cover for a PCB design magazine. Having been involved in all types of PCB mags, I have to say that design is by far the hardest segment to illustrate.

Fabrication and assembly are much simpler. You have a variety of ideas to work with: a close-up of a PCB or PCBA, a panel of PCBs, capital equipment, drills, lasers, squeegees, dispensing nozzles, a thermometer reading 260°C for a lead-free assembly...the list goes on. Or you can just write something clever in green or copper-colored lettering.

But design is such an abstract idea. There are a few obvious cover ideas: a giant key with a tagline of "Unlocking the Door to Signal Integrity." Then there's the twisting path heading into the horizon, labeled "The Long and Winding Road to HDI." After that, it's a struggle.

Design is the most important part of the whole equation, in my humble opinion, but it's hard to wrap your mind around it. PCB design needs an icon, and it needs one now.

What do you think it should be? What is our robot? What is our icon?

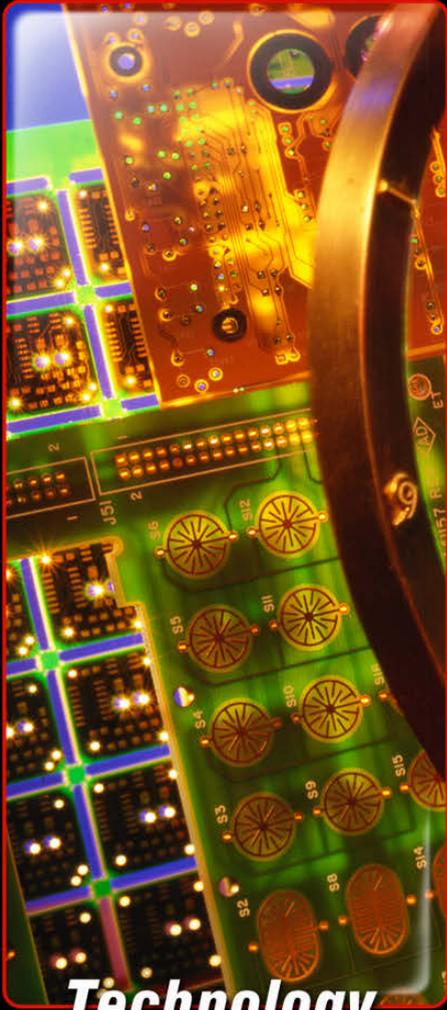
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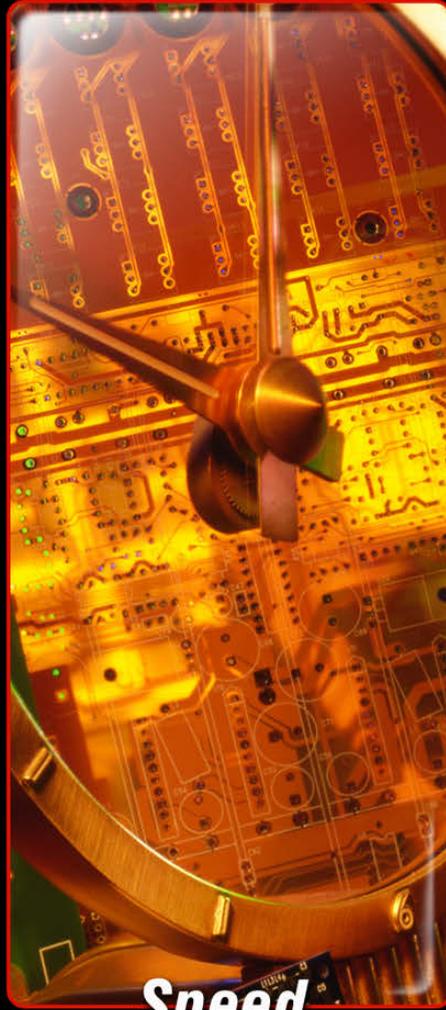


Andy Shaughnessy is managing editor of *The PCB Design Magazine*. He has been covering PCB design for 13 years. He can be reached by clicking [here](#).

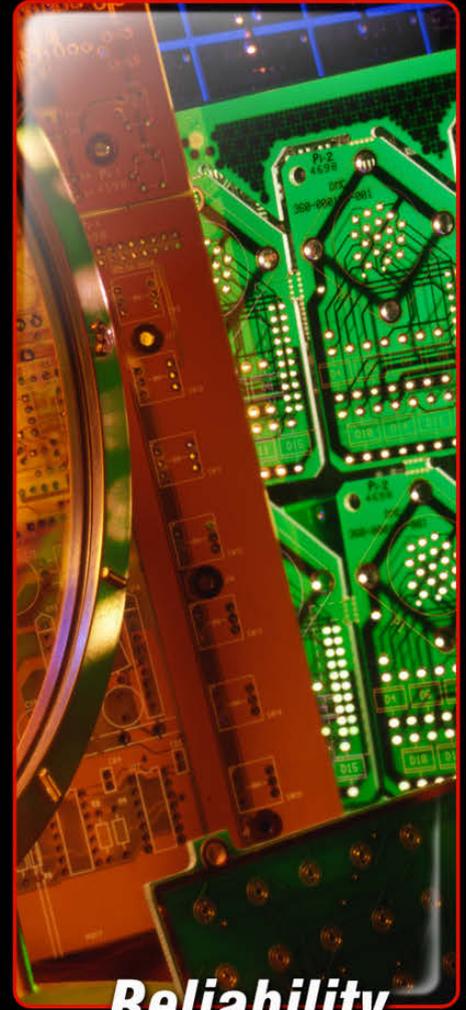
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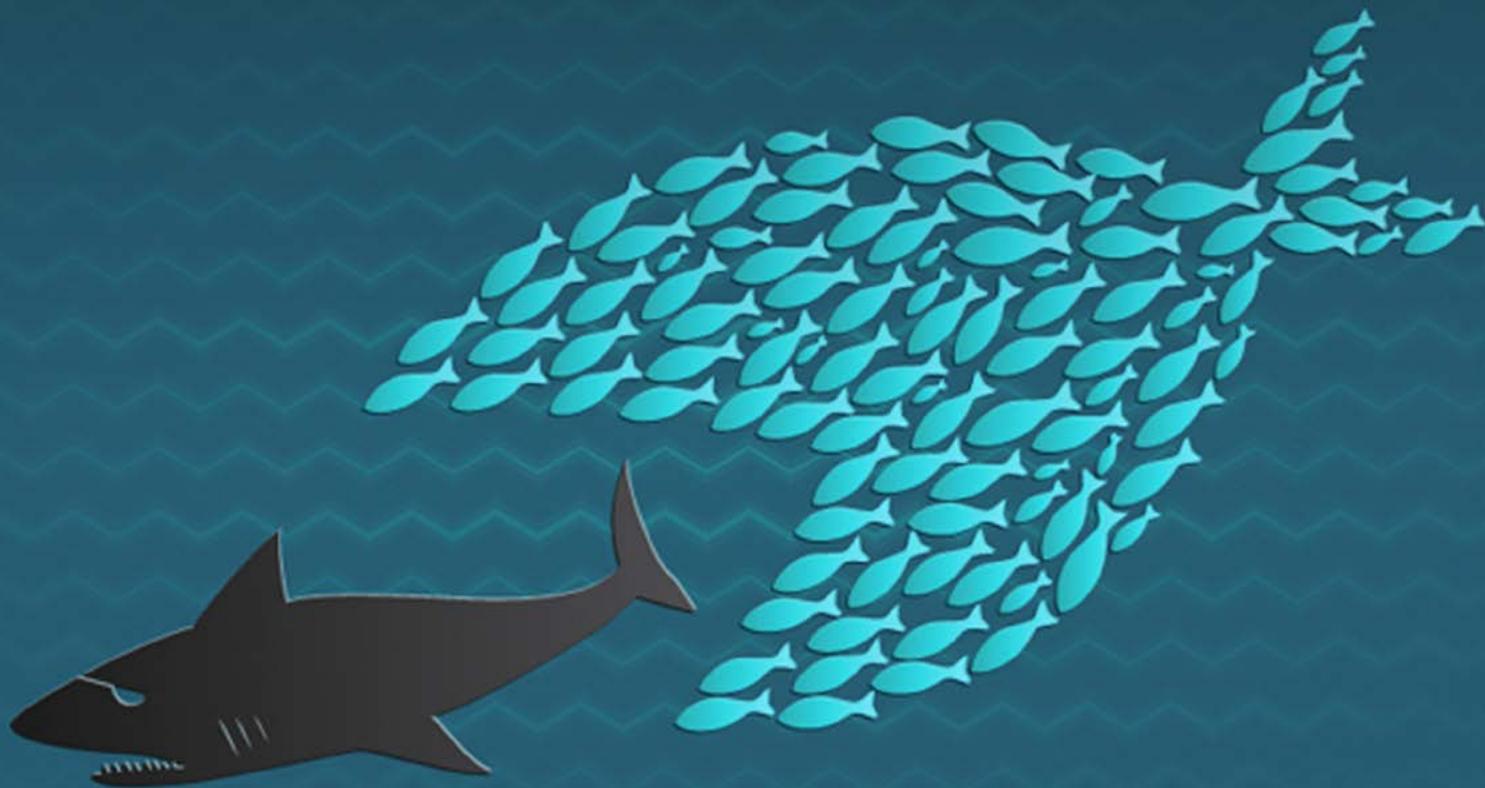


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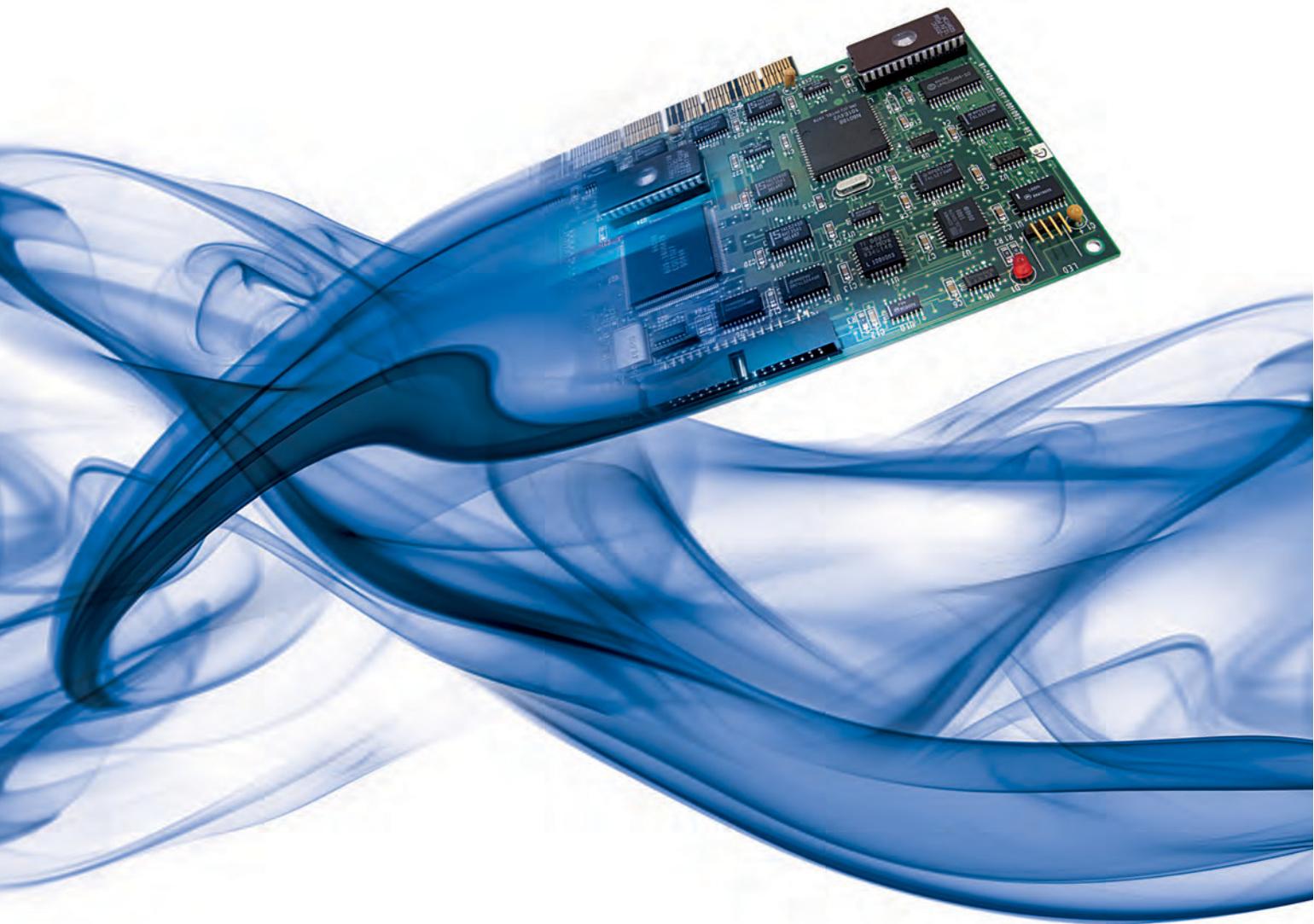
by **David Wiens**
MENTOR GRAPHICS CORP.

Design Efficiency in the Fast Lane

PCB systems design pressures can be broken down into the ubiquitous buckets of time, cost and quality. Efficient design is about balancing the three. Push too hard to shrink the design time, and watch your costs go up while quality diminishes. Spend too much time optimizing a design, and watch your market window wave goodbye. A recent survey by The Aberdeen Group ^[1] confirmed these critical pressures, and also identified some strategies to resolve them—two of the top four involved optimizing collaboration across the design team. Figures 1 and 2 show the responses graphically.

PCB design teams can range from the individual who does everything up to global enterprises with large, distributed teams. Large teams have a competitive advantage of resources and specialization, but they also bear the challenge of optimizing those resources to avoid the diminishing returns that can come with team inefficiency. The other dimension to the problem is design complexity, illustrated with Figure 3. An individual can design almost anything with the right tools; the challenge is to complete the design within a reasonable time, while optimizing quality and cost. Enterprises can tackle complexity with larger teams on a project, including specialists who can optimize design functions for quality.

Let's look at typical types of enterprise collaboration, and propose some best practices to optimize efficiency across the design team.



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OPTIMIZING COLLABORATION FOR PCB SYSTEMS DESIGN *continues*

Pressures on the PCB Process

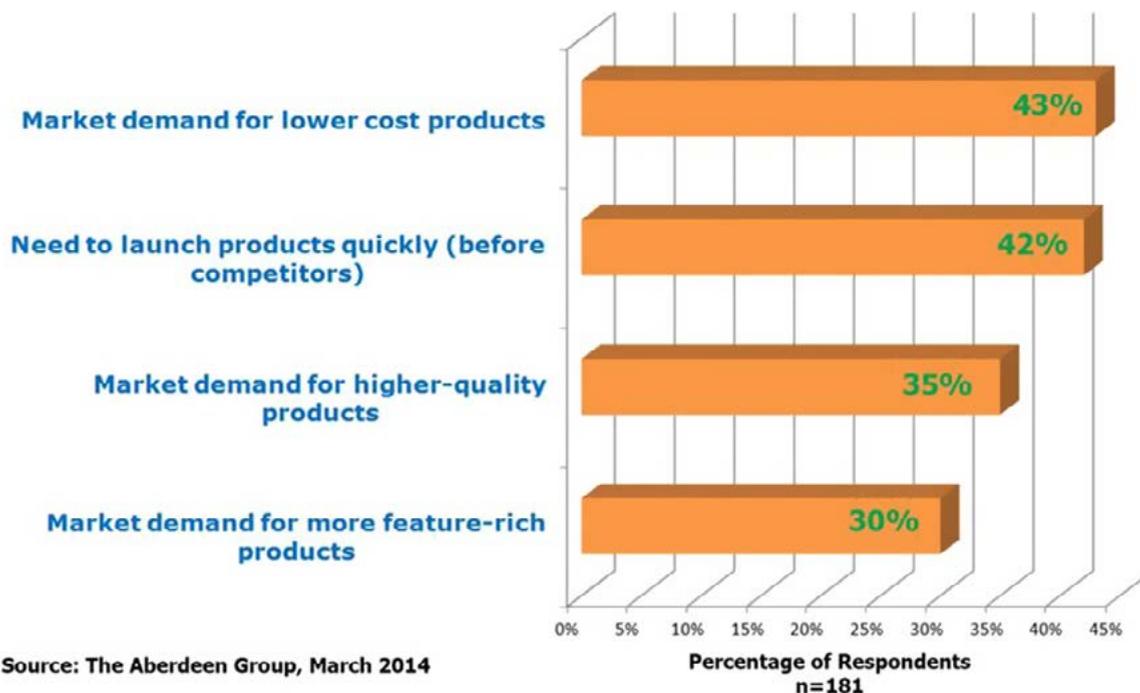


Figure 1: From the Aberdeen Group report, the top four responses to pressures on the PCB process.

Strategies to Reduce Pressures in the PCB Process

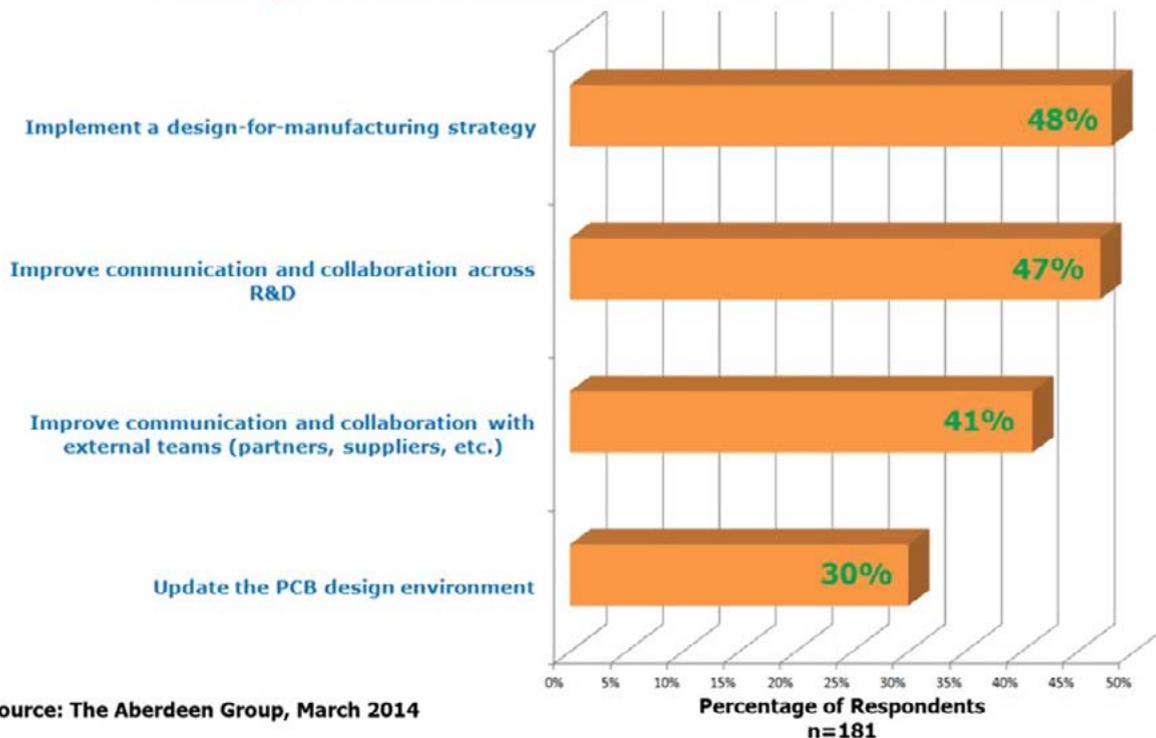


Figure 2: Respondents were also asked to list strategies that would help reduce pressure.

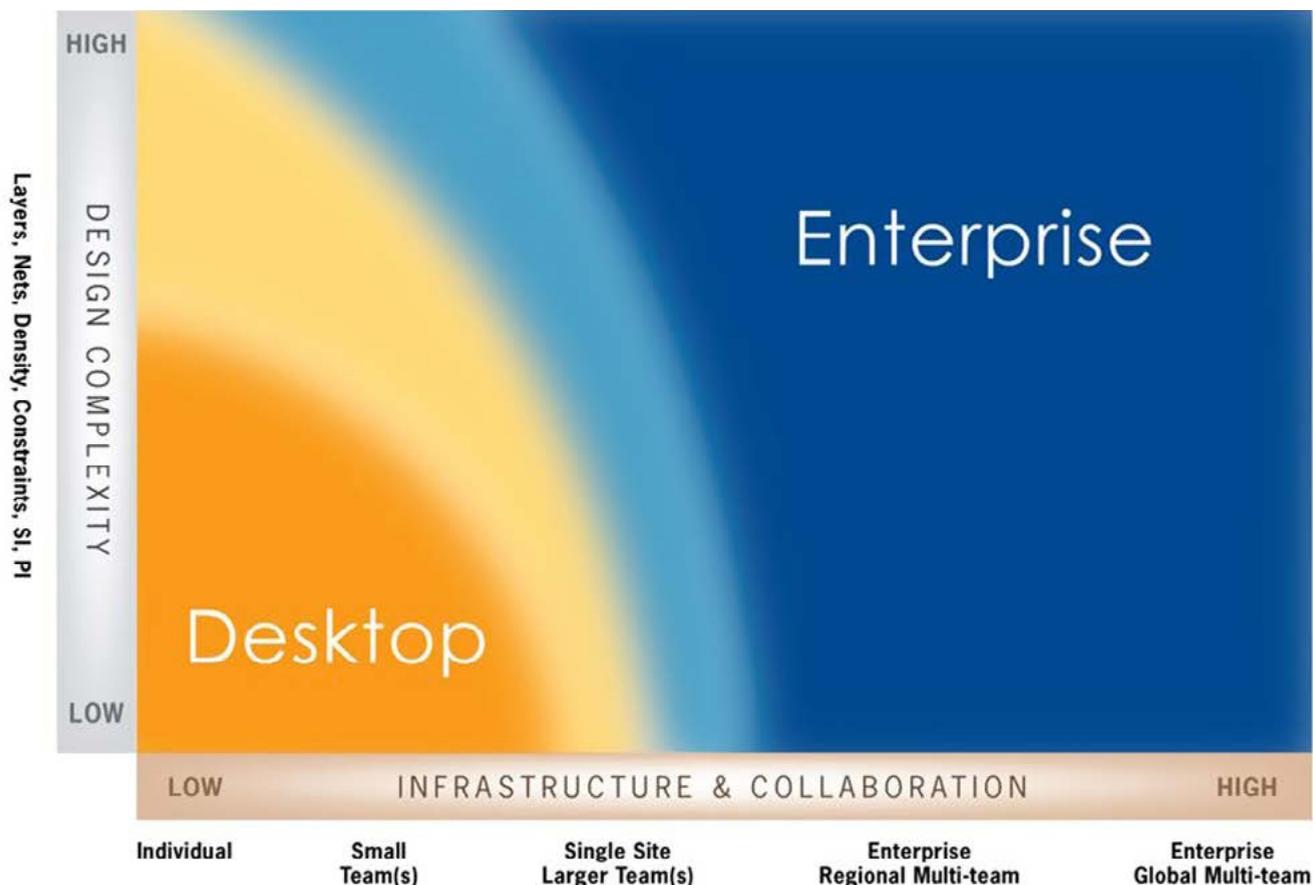


Figure 3: Organizational and design complexities scale. The challenge is to complete the design within a reasonable time, while optimizing quality and cost.

Collaboration is Everywhere

Regardless of your team size, there are always plenty of opportunities for collaboration; this business isn't a good place for hermits. Because collaboration involves transfer of data from one person to the next, and often from one tool to another, multitudes of "neutral" files have sprung up over the years as hand-off mechanisms. Some formats have survived the ages to become de facto or formal standards, but even formal standards are subject to interpretation at the sender or receiver, leaving them as imperfect media for collaboration but still the best option in many cases. Within vendor tool flows, the most efficient collaboration is achieved by sharing the same database, leveraging a client/server architecture so that there are no errors in translation, and absolute concurrency is achieved.

Due to inefficient collaboration environments, traditional design processes were very serial in progression—one stage would be completed before the next was started. ECOs were painful to execute, and thus discouraged. Improved flow integration and collaboration standards have enabled concurrent design processes that significantly reduce design cycles, and provide additional opportunities for design validation and optimization (virtual prototyping).

Collaboration opportunities can be broken down into those between engineering disciplines (e.g., ECAD/MCAD, FPGA/PCB, and design/manufacturing) referred to here as "inter-discipline collaboration, and those within an engineering discipline (e.g., multiple engineers working on a schematic, or multiple designers working on a layout) referred to as "intra-discipline collaboration."

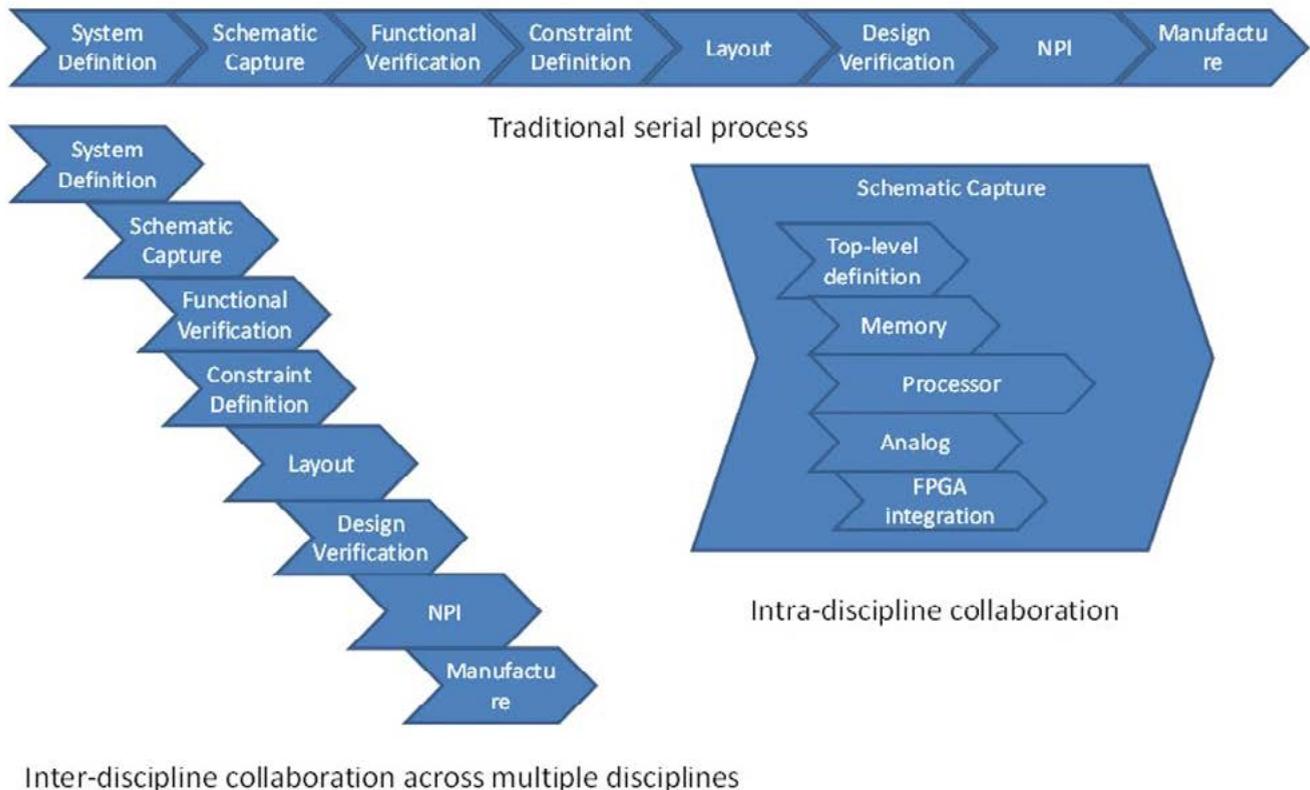
OPTIMIZING COLLABORATION FOR PCB SYSTEMS DESIGN *continues*

Figure 4: Collaboration can significantly compress the traditional serial design process.

Inter-Discipline Collaboration

The most common example occurs between design engineers and layout designers. Originally, it was a very serial process, with an engineer defining the logic on paper, then handing to the designer to draw the schematic and layout the board. Today, logic design, constraint definition and layout are expected to proceed concurrently, with initial board definition and placement occurring while the schematic is still under development. Of course, even if a schematic is proclaimed complete there are almost always going to be ECOs (something that the recent Aberdeen study identified as a major obstacle to efficient design)—being able to easily update the design is critical. An engineer is basically communicating intent to the layout designer (e.g., packaging, connectivity, constraints, and component floor plans/groups). In an efficient collaboration this is done without side documents or “voice-driven mouse.”

The other common collaboration is between

layout designer and manufacturing (typically with an NPI engineer acting as the middleman). This also used to be a very serial process, with manufacturing waiting until the layout was complete and with outputs generated before doing the first checks for manufacturability, creating a ton of design re-spins. Today, best practices involve leveraging the DFM rule deck from the target fabrication and assembly houses during placement and routing to optimize the layout before it’s finished (known as concurrent manufacturability validation). The hand-off to manufacturing has also been streamlined, with ODB++ being leveraged as the single source of data for manufacture (replacing the multitudes of separate files that used to be passed to manufacturing, requiring time-consuming, error-prone re-integration to produce intelligent data for manufacturing).

Every PCB must have a mechanical enclosure. Traditional collaborations were done with very conservative constraints (limiting PCB de-



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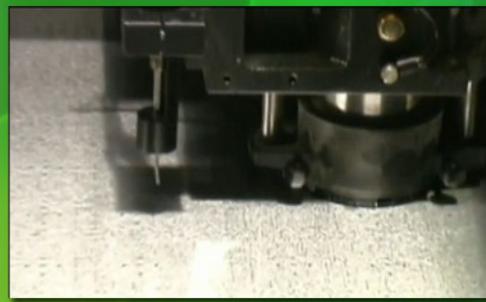
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OPTIMIZING COLLABORATION FOR PCB SYSTEMS DESIGN *continues*

sign options) and actual alignment wasn't determined until physical assembly. Today, PCB design systems include 3D visualization to enable optimization for the enclosure—and when collaboration is required to optimize the electro-mechanical product, dynamic communication with the mechanical engineer is provided via tools leveraging the ProSTEP IDX standard. Given basic outline constraints, design of the PCB can now proceed in parallel with refinement of the mechanical enclosure.

Integration of FPGAs on PCBs provides an opportunity for pin swapping to optimize the PCB for performance and cost—so efficient collaboration between FPGA and PCB engineers is critical. The cross-domain interchange has been vendor-specific, requiring flow-dependent processes and limiting optimization passes. Improved integration has enabled bi-directional collaboration and even multi-FPGA optimization based on PCB placement.

Most PCBs don't live by themselves; they're coupled with daughter cards or backplanes for cost-efficiency and flexibility. Definition of that multi-board PCB system has typically been isolated from the PCB design environment, requiring re-capture at the PCB stage (much like the original collaboration between PCB engineers and layout), increasing design time and potential for re-design errors, and also minimizing opportunities system optimization. Emerging environments support dynamic collaboration between system-level and PCB-level design, facilitating quick ECO updates and re-partitions for optimized system performance, size and cost.

Another system context is the design of IC through package to PCB. These three disciplines are often supported with disparate, disconnected toolsets. Tying the disciplines together (or even leveraging common tools) improves collaboration, resulting in optimal system performance, size and cost. Recent advances have automated definition of the connectivity between platforms, and also leveraged common design technologies to minimize the system design learning curve.

Mid-to-large enterprises achieve economies of scale by leveraging common design data (e.g., component libraries, simulation models,

and reuse blocks) across multiple projects. They typically manage this data, as well as control access to work-in-process designs, via conventional PLM systems. While functional, this process views PCB data as black boxes, with no visibility into the actual data, limiting design reviews and collaboration opportunities. Emerging standards such as the EDX format coupled with PCB-level design data management enable efficient collaboration with enterprise-level teams, and provide optimal access control and visibility for PCB design data.

Intra-Discipline Collaboration

We've covered the parallelization of inter-discipline tasks, but what about concurrency within a design task like schematic or layout design? Given that legacy schematic entry and layout tools were designed for a single user, it's no surprise that a multi-user process is cumbersome, though some enterprising teams haven't created workarounds. Engineers have long teamed up on a schematic design, enabled by either a hierarchical or flat multi-sheet structure that allows them to partition and distribute schematic blocks, and later stitch them back together. This "split and join" process requires manual communication regarding system updates (e.g., a new global signal name), diminishes team visibility into each other's work, and provides fun alignment challenges when the blocks are reintegrated. Now imagine doing that on a layout (it's often done by region or layer). How do you ensure that cross-region traces or vias will line up when the design is reintegrated? How do you partition the design when you've got cross-board (side-to-side or front-to-back) connectivity? How do you decide partition areas if not all parts are placed?

To enable efficient concurrent intra-discipline collaboration, the tools must be re-architected to support the team model. A client/server architecture enables multiple team members to concurrently access and edit a design, with dynamic updates so everyone is in sync. The communication between clients and server must also be optimized to deal with network latency issues if the team is distributed.

Applied to the schematic stage, multiple engineers could define logic in different sheets of

a common database (no need to partition the design first). This has the added benefit of resource flexibility—if there's no up-front partitioning pain, there's no problem adding team resources where necessary for short intervals to accelerate a project.

Optimization of designs for signal and power integrity is transitioning from isolated specialists (leveraging the inter-discipline collaboration model) to every design engineer. This means that the engineers must also be able to access simulation tools directly from the schematic, and transfer rules developed through analysis directly into the constraint system.

Most systems today allow definition of constraints within the schematic, a significant advancement from the days when spreadsheets were passed to the layout designer for inclusion. If you have multiple engineers working on the schematic, you also must allow concurrent constraint entry. Taking it a step further, since the layout team also needs to see the constraints,

they must be able to access and edit constraints along with the engineers.

The real fun with true concurrent design comes at the layout stage. Without a partitioning hurdle, designers could jump into a design at any time. True concurrency means no boundaries, and no task limitations (i.e., it should work for placement, routing, plane definition, manufacturing preparation, etc). A side benefit of this approach is mentoring—a junior designer could work alongside a senior designer to learn best practices (in reality they could be on opposite sides of the planet). Design reviews and/or validation could happen concurrently with design. Some teams segregate design by functional boundaries (analog, SerDes, DDRx, RF); you could call this inter-discipline collaboration, but I've included it in this section since they all use the same tool for layout. And as you'd expect, true concurrency should allow all of these specialists to work in parallel, as shown in Figure 5.

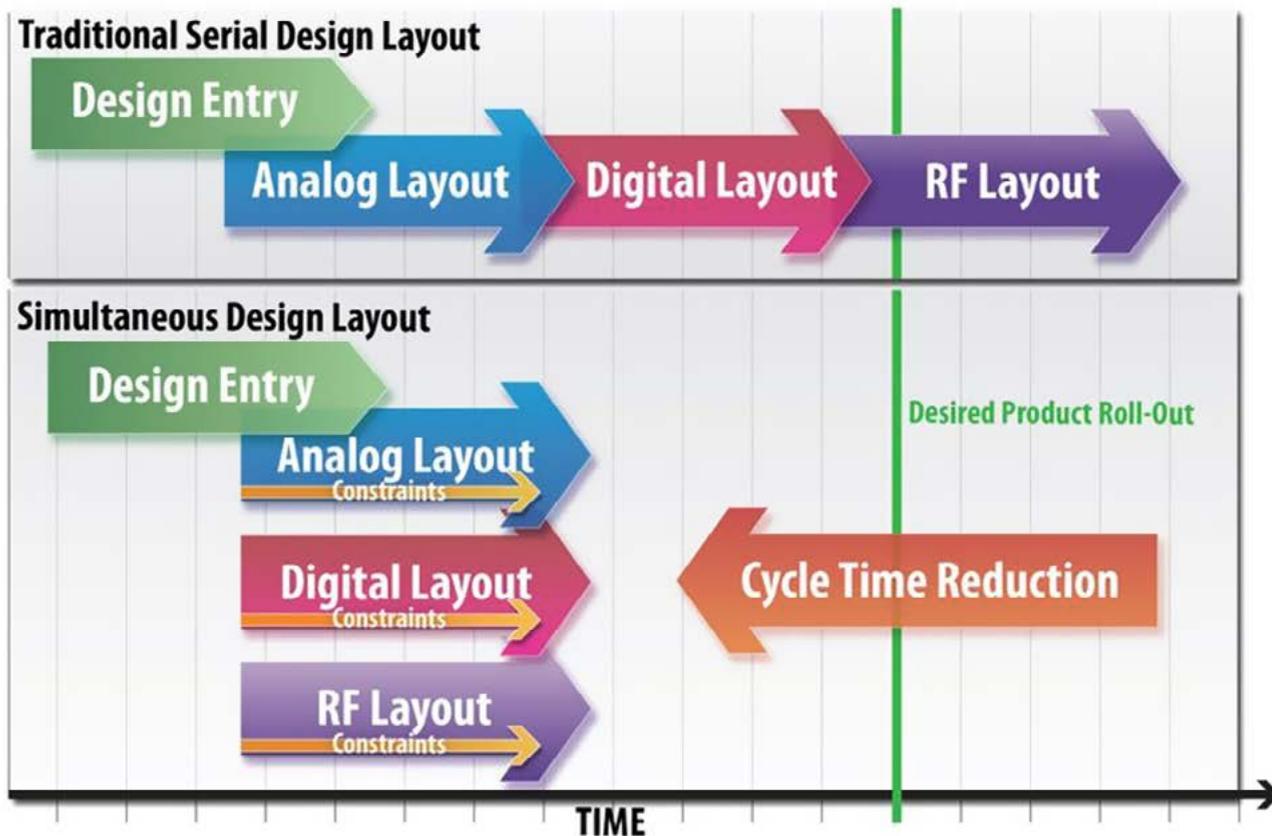


Figure 5: Concurrent layout can shorten the completion time significantly.

OPTIMIZING COLLABORATION FOR PCB SYSTEMS DESIGN *continues***Impediments to Collaboration**

As you might expect, entering a concurrent world can have some challenges beyond just a new tool learning curve. You must also have awareness of hardware and network configuration requirements and limitations (particularly with geographically dispersed teams) to ensure optimal client/server performance.

There are also new opportunities for conflict between team members in the intra-discipline model. What if two people want to edit the same schematic block, constraint, component or route? Conflict resolution mechanisms can be automated within software minimizing the need to stop work, send e-mail, or deploy the “sneakernet” to resolve the issue. But an effective workflow must also be defined, with team leads identified to drive the process and keep the team in sync. Disruptive updates, such as a logic or constraint ECO, should ideally be coordinated to minimize design cycle interrupts that impact all members working concurrently (constant forward/back annotations between a team of engineers collaborating with a team of layout designers will drive everyone crazy).

Another issue with intra-discipline collaboration (regardless of whether it's the traditional serial 24-hour shift model or a concurrent process) is re-engineering, also known as the not-invented-here syndrome. Everyone has their own style for laying out a schematic or layout—team members must resist the urge to redo the work of others, or the gains of collaboration will quickly be lost.

Enabling Efficient, Concurrent Collaboration

The primary benefit of efficient collaboration is an accelerated design cycle. We've seen customers achieve more than 70% reductions in design time just on layout, with efficiencies nearing 100%. In addition, if the core flow is accelerated, additional virtual prototyping tasks can be added to the process to validate for improved quality (e.g., signal/power integrity, thermal, and manufacturability). Alternative archi-

tectures and layouts can also be explored (e.g., different place, route and stack-up scenarios) to optimize the product for performance and cost.

Concurrent collaboration (without the partition/reassemble overhead) is also a great resource management tool, enabling the CAD manager to shift resources to the most critical projects

at any time, maximizing resource usage. Design specialists can be deployed in any geographic location concurrently with the rest of the design team. Dropping the partitioning step also improves data integrity by maintaining just one copy of the design data.

Moving from a serial to parallel collaborative process also reduces extra shifts and overtime—a significant design cost benefit. With the “round-the-clock/world” design model, there's a longer time between finding and fixing problems; specialists aren't fond of doing design reviews 24 hours a day. But a concurrent process resolves this (everyone's working in the same shift). There are limits to how many people can work concurrently on designs, so if you really want that overtime, it's still an option when design volume goes through the roof.

PCB systems design can't be done without some level of collaboration—everyone does it. There are a ton of design process and data format improvements that have emerged over the last five years to enable efficient collaboration. Take a look at your team collaboration, and ask yourself the question: Am I as efficient as my competitors? **PCBDESIGN**

“
We've seen customers achieve more than 70% reductions in design time just on layout, with efficiencies nearing 100%.
”

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1. PCB Design: A Guide to Optimizing Design Engineers, Kevin Prouty, The Aberdeen Group, March 2014.



David Wiens is a product marketing manager at Mentor Graphics.

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VT-4B3	3.0W/m.K.	✓	✓	✓	✓
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Multi-Site Concurrent Design: Tips and Best Practices



by Craig Armenti
ZUKEN

What does concurrent design mean to you? Chances are, if you ask six different engineers or designers you will get six different responses. Their responses will vary based on the types of industries they are in and their experience in this area. When I presented a paper on concurrent design at a conference in 1998, the highlight was having been able to achieve one schematic engineer and one PCB designer located at one site simultaneously working on one design. Since then, time-to-market demands, along with advances in networking technology and cloud computing, have pushed the process to require multiple schematic engineers and multiple PCB designers located at multiple sites, all accessing the same database concurrently: multi-site concurrent design.

How Did We Get Here?

When commercially-developed EDA software became readily available during the early 1980s, companies with multiple design centers

shared very little design data. The EDA vendors were tightly aligned with computer hardware vendors and there were no standards for installation or GUIs. Typically, each design center was responsible for configuring and managing their individual installation of the EDA tool suite—easy but limited. Each design center usually had a dedicated tools support person or team that would gladly customize the environment based on user requests. Configuration management was mostly ad hoc, with little traceability back to the original requirements for any environment customization.

Over time, as EDA software matured, as technology allowed for real-time collaboration, and as companies expanded, merged, or were acquired, each site's highly customized, locally optimized unique environment suddenly became a liability. In order for one design center to share data with another design center, the local environment and the local CAD library had to be self-contained (best case) or transferred in whole (worst case) in order for the design data to be viewable and editable at another site. Design teams quickly came to the realization that standardization of both the EDA environment

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MULTI-SITE CONCURRENT DESIGN: TIPS AND BEST PRACTICES *continues*

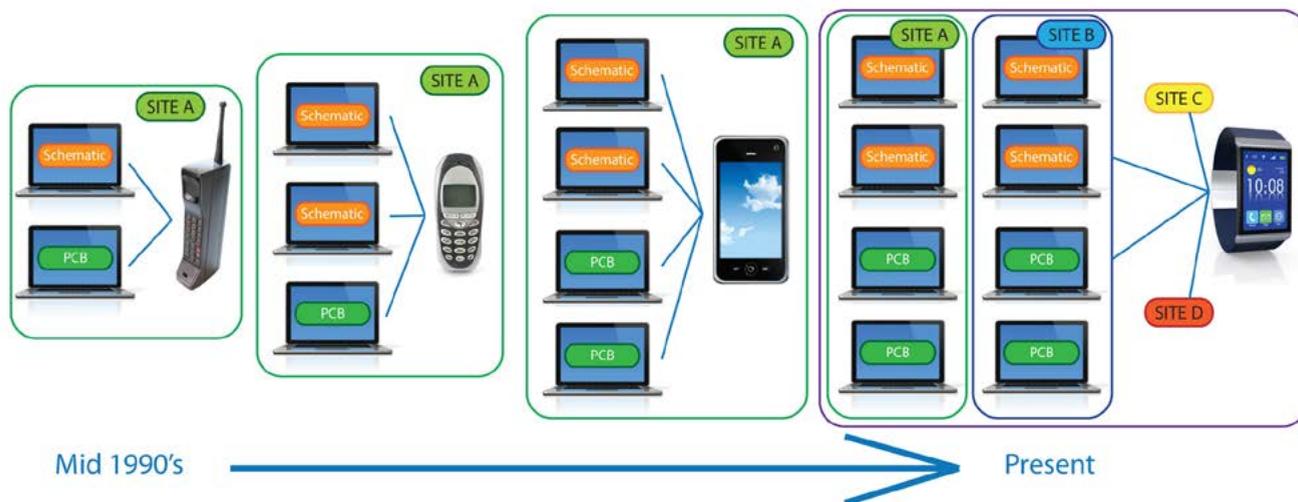


Figure 1: The evolution of concurrent design.

and the CAD library would be required in order to realistically share and reuse design data.

The Foundation: The EDA Environment

As the practice of maintaining design centers in different regions of the world has proliferated, the need to manage EDA tools globally and the opportunity for global multi-site concurrent design present themselves. If you are responsible for the configuration and management of an EDA environment, you already know this is a critical role. It's more than just an assemblage of tool executables. The underlying configuration files and the associated CAD library influence all system operations. The spiral of complexity rapidly increases when the installation spans multiple sites in the same region and becomes even more complex when the installation spans design centers around the globe. Proper configuration and management of a global EDA environment and CAD library is a prerequisite for global, multi-site concurrent design.

Global Multi-Site Product Development Requirements

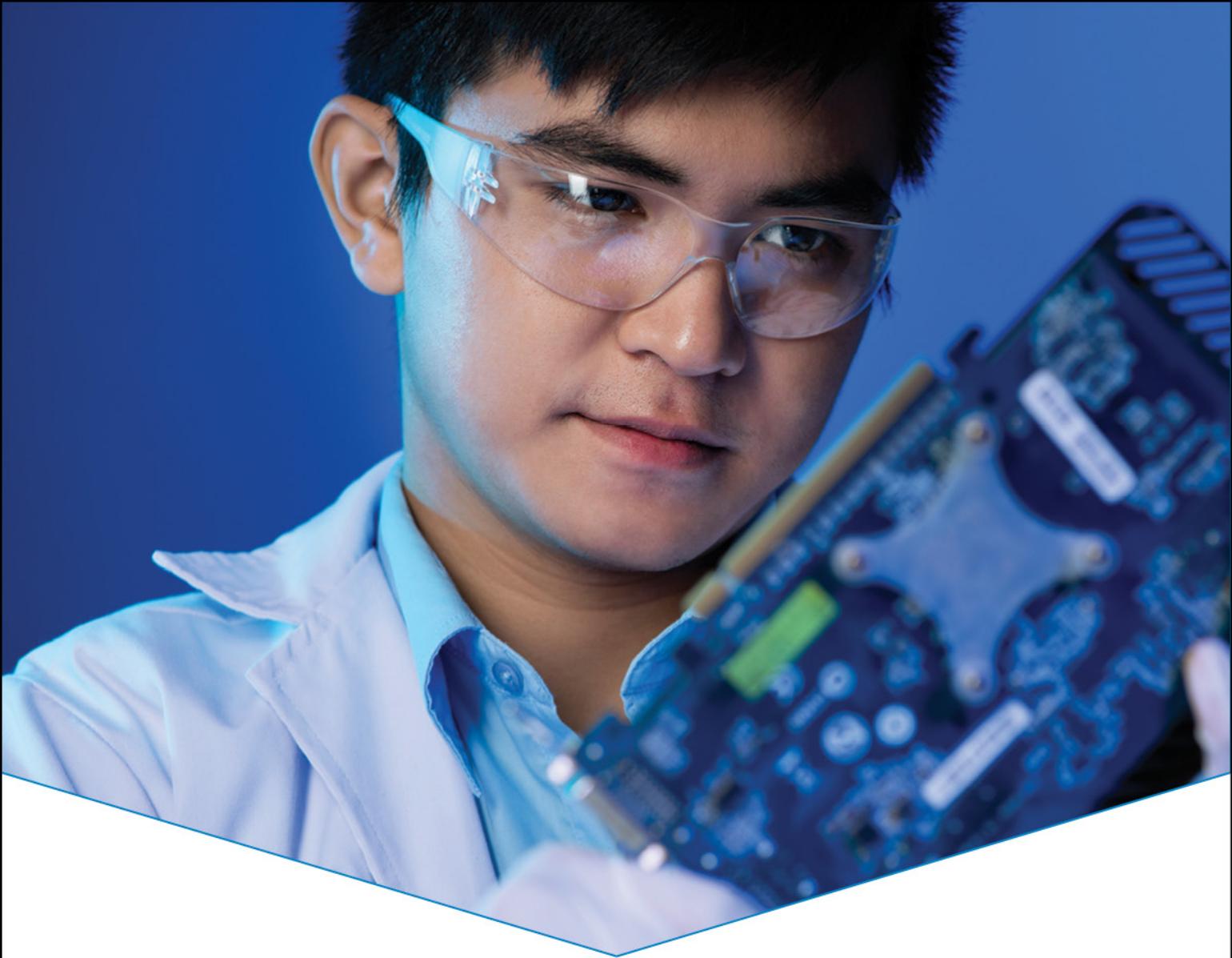
A company that has a need to support multi-site concurrent design will require an underlying engineering data management (EDM) system that can dynamically manage the environment, the CAD library, and the design data per the following requirements:

1. Environment Management

- All design sites utilize a common, centrally managed, continually synchronized enterprise-level EDA environment. Minor site-specific variations are acceptable, as long as the variations do not compromise the fundamental requirement to seamlessly share design data.
- All environment data is under strict revision control with write access allocated only to those with responsibility for maintaining the environment.
- Environment data is updated as required, tested in a sandbox environment, approved for release, and then synchronized to each site's production environment.
- Only environment data customized to support the corporate requirements is managed at the enterprise level. All other environment data is accessed from the local install. The end result: you are only managing and replicating the minimum set of customized data to support your corporate requirements. You move from managing hundreds of environment files, to managing files that now potentially number only in the tens.

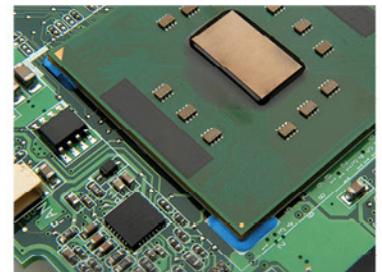
2. Library Management

- All design sites utilize a common, centrally managed, continually synchronized CAD library.



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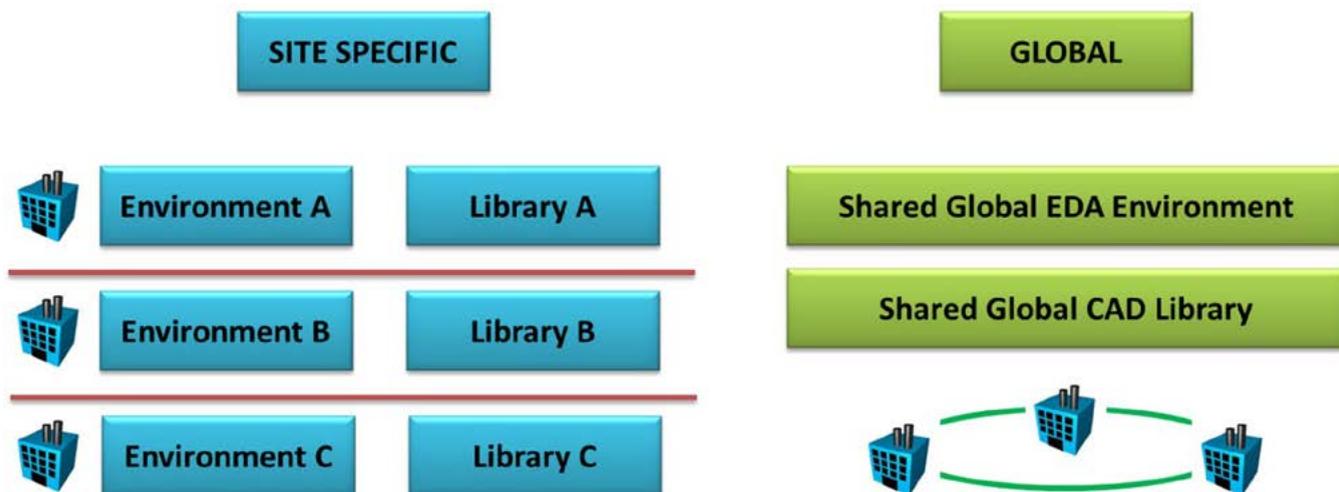
MULTI-SITE CONCURRENT DESIGN: TIPS AND BEST PRACTICES *continues*

Figure 2: Site-specific vs. global approach.

- In its simplest form, write access to the library data is allocated only to those with responsibility for maintaining the library's logical, parametric, and geometric information. In its more sophisticated form the library can also be configured to interface with information from a centralized Component Information System (CIS). At this level the parametric data in a Material Requirements Planning (MRP) system, an Enterprise Resource Planning (ERP) system, or a content provider, is available for viewing during the component decision-making process.

- Library data is updated as required, tested in a sandbox environment, approved for release, and then synchronized to each site's production environment.

3. Data Management

- All design data exists in a central vault, accessible from any design center at any time, enabling distributed design teams to work closely together.

- Design data is under continuous revision control, with data locked for non-editing team members during work-in-progress and to all team members during release to manufacturing.

- Access to design data is permission-based—only those with a need to view and/or edit data have access to the data.

- Check-in and check-out of either entire designs or portions of designs is fully supported

by both the EDM system and the EDA software suite.

- A library of known good design data (circuit blocks and PCB blocks) is available and under strict revision control.

Leveraging Your Global Configuration

Now that you are managing your EDA environment, CAD library, and design data to properly support your global engineering team, let's leverage all three to enable effective multi-site concurrent design. As time to market for many high tech products continues to be a paramount driver, various methods and techniques to reduce design cycle time are continually being developed and evaluated. For leading-edge products with short lifespans, the first to market has the luxury of time, while the clock is ticking for the followers. In many cases the leader can produce multiple generations of a product before the follower brings their first "me too" product to market. A properly managed and configured global design environment can provide a competitive advantage that permits design cycle time compression without the need to add resources or to compromise quality.

Manage and Share Work Locally and Globally

Design teams with resources distributed around the globe are a fact of life for many corporations today. The ability to work on a design

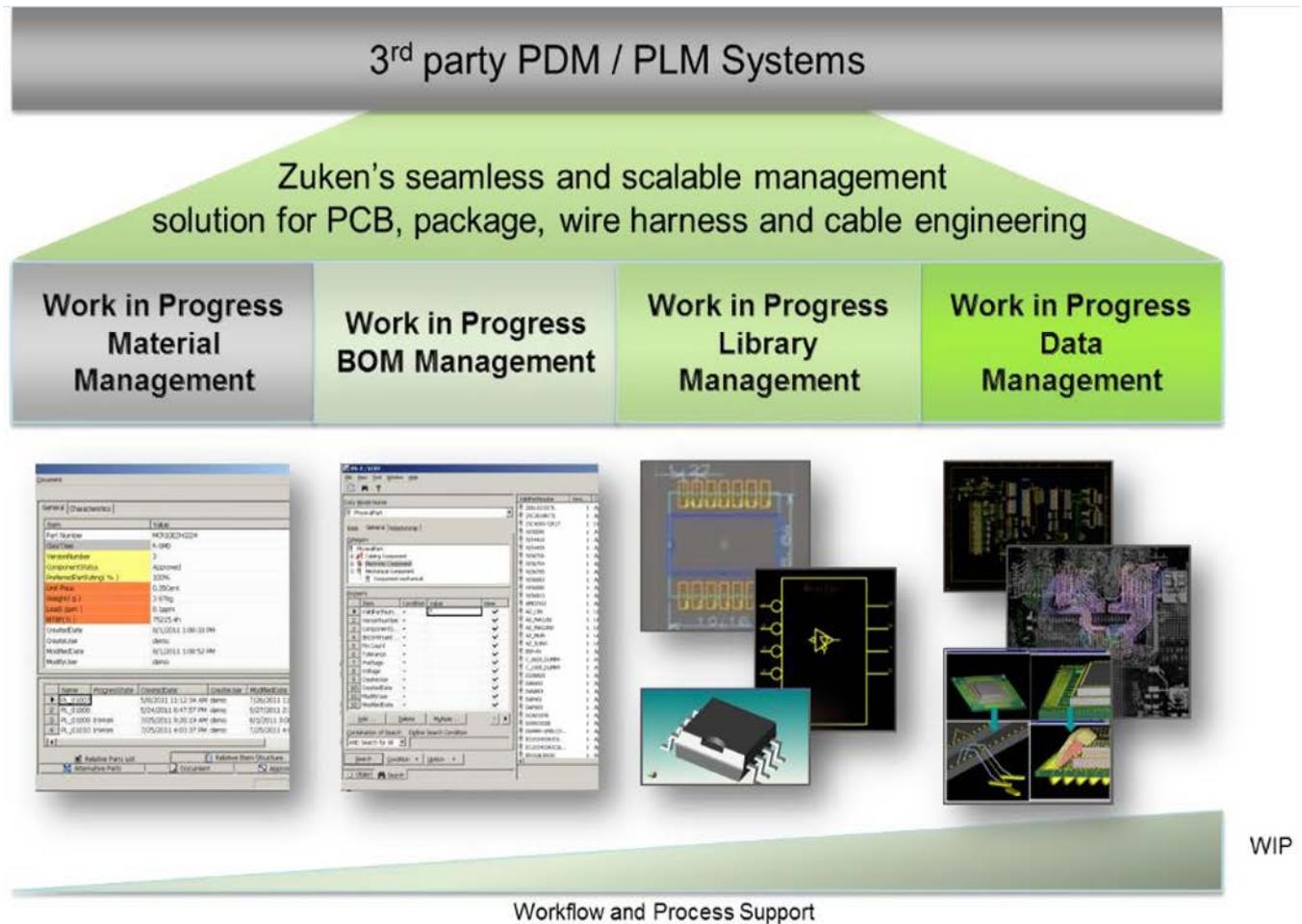


Figure 3: Zuken's engineering data management solution.

continually, following the sun across multiple sites around the globe, may well be critical to your time-to-market success. Functional experts in different regions can be leveraged to continually move the design forward 24 hours a day. Think of your global configuration and supporting EDM system as a "virtual design center" that can seamlessly manage both the individual design objects along with their relationships at any point in time at any of your global design centers, ensuring rigorous configuration control throughout the design cycle.

Partition the Design for Success

Multi-site concurrent design employing a follow-the-sun methodology is more than just moving the entire design container from one design center to another and then back again

throughout a 24-hour period. Any product development team member at any site must have access to the design data at any time. In order to facilitate this philosophy, the design team should first use its EDA tool to partition the design by functional area. For example, if a design contains memory, processor, WiFi, RF, and power functional areas, the design container should be configured so that both the schematic and the PCB are partitioned along those same functional areas. Most EDA tools support schematic partitioning using hierarchical blocks, but that's the easy part, your tool also needs to support:

- **Partitioning the PCB**

There are several ways for a design team to partition a PCB. One option is dividing the board along predetermined functional bound-

MULTI-SITE CONCURRENT DESIGN: TIPS AND BEST PRACTICES *continues*

aries with each designer routing to common virtual points. Another option is to simultaneously design without fixed boundaries. Design teams that are new to concurrent design, or with dense, highly-constrained designs, will find the former easier and more straightforward to implement than the latter. Furthermore, in the divided approach the PCB split often emulates the schematic partitions, not only facilitating the work in progress concurrent design, but also promoting subsequent vaulting of PCB blocks for reuse.

- **Management of schematic and PCB partitions both individually and as a whole**

The EDM system needs to do more than just manage check-in and check-out, it needs to have a true understanding of the ECAD data. For example, if one schematic partition is checked out from your EDM system for edits, the other partitions should still be visible as

read only in the schematic editor. The same applies to the PCB.

- **Centrally managed parametric data**

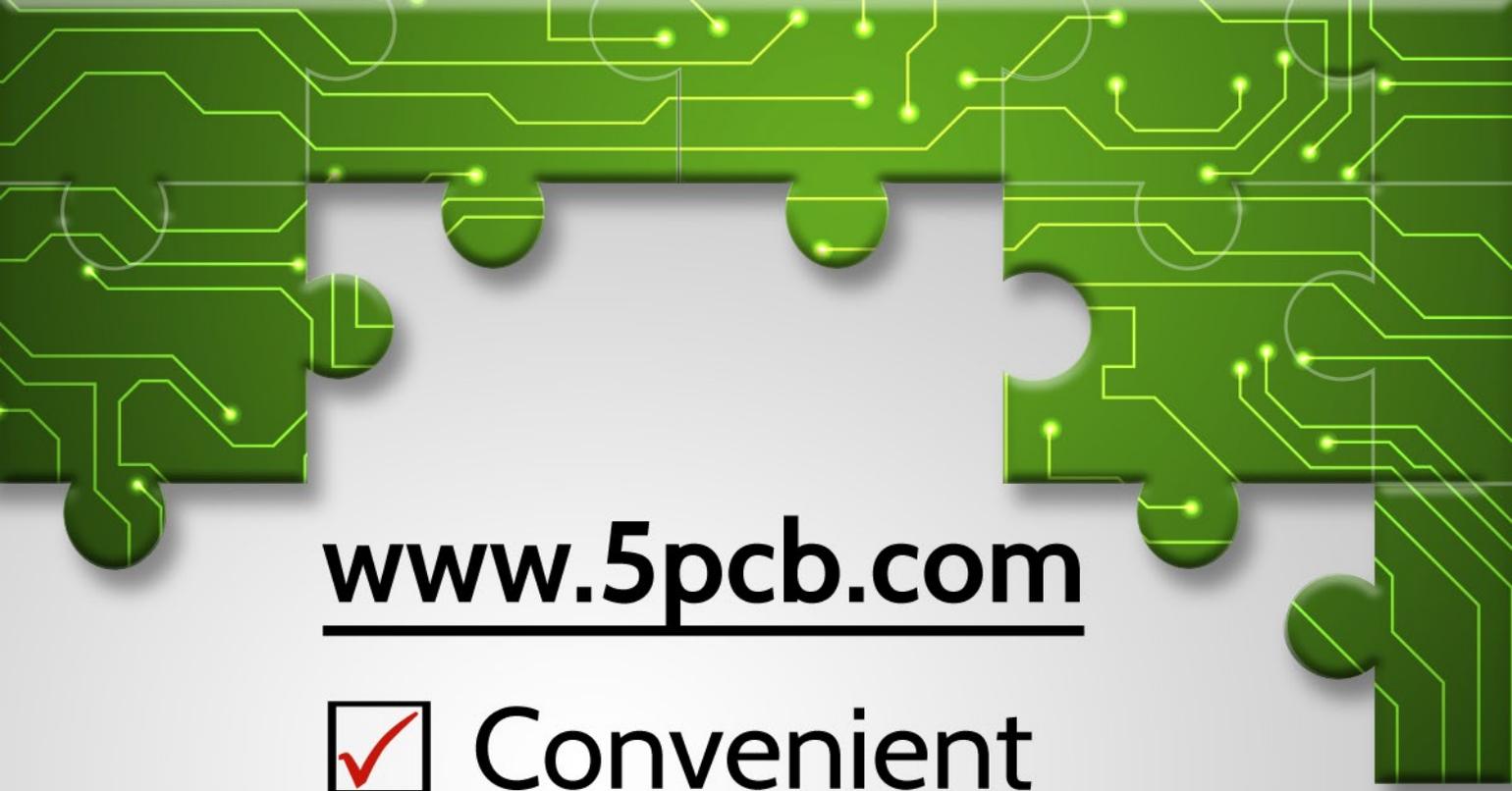
The component engineering tools should “suggest” the most appropriate component to a design engineer for a given partition based on corporate defined criteria such as price, availability, number of suppliers, pending obsolescence and reliability. This capability simultaneously improves quality while also properly managing component inventory.

- **Proper management of design rules and constraints**

Just because the design is partitioned doesn't mean the design rules and constraints become unusable. The EDA tool should support central constraint management for both electrical and physical rules that understands how to apply the constraints within the context of the partitioned schematic or PCB.



Figure 4: The “follow-the-sun” design methodology.



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MULTI-SITE CONCURRENT DESIGN: TIPS AND BEST PRACTICES *continues*

Figure 5: Do you want to be a leader or a follower?

Conclusion

In this article we have reviewed best practices and processes that can be applied to assist and, in fact, embolden EDA tool managers, engineers, and PCB designers to move forward

with multi-site concurrent design. By investing the time to create a proper foundation with a standardized global EDA environment, then adding an EDM system that truly understands how to manage your ECAD data, you will be well on your way to sharing, reusing, and concurrently designing across all of your product centers.

In the end, you will benefit from a new level of collaboration between globally-distributed design centers, while also realizing tangential effects like promoting the documentation and sharing of engineering best practices and common processes for the benefit of all design teams in all regions. At the end of the day, you and your design team need to decide: do you want to be a leader or a follower? **PCBDESIGN**



Craig Armenti is senior technical marketing manager for PCB products at Zuken.

“Tiled” 36-core Chip Unveiled

For years, Li-Shiuan Peh, the Singapore Research Professor of Electrical Engineering and Computer Science at MIT, has argued that the massively multicore chips of the future will need to resemble little Internets, where each core has an associated router, and data travels between cores in packets of fixed size.

This week, at the International Symposium on Computer Architecture, Peh’s group unveiled a 36-core chip that features just such a “network-on-chip.”

The chip’s 36 cores are given different, hierarchical priorities. Say, for instance, that during one interval, both core 1 and core 10 issue requests, but core 1 has a higher priority. Core 32’s

router may receive core 10’s request well before it receives core 1’s. But it will hold it until it’s passed along 1’s.

Cache coherence in multicore chips “is a big problem, and it’s one that gets larger all the time,” says Todd Austin, a professor of electrical engineering and computer science at the University of Michigan. “Their contribution is an interesting one: They’re saying, ‘Let’s get rid of a lot of the complexity that’s in existing networks. That will

create more avenues for communication, and our clever communication protocol will sort out all the details.’ It’s a much simpler approach and a faster approach. It’s a really clever idea.”



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News Highlights



North American PCB Industry Growth Still Slow

“With year-to-date growth rates improving but still negative, and a book-to-bill ratio just barely in positive territory for the second month, the North American PCB industry appears to be moving very slowly toward a modest recovery this year,” said Sharon Starr, IPC’s director of market research. “The negative month-to-month growth rates in April reflect normal seasonal patterns.”

IPC PCQRR Database Allows PCB Fabricator Comparison

The IPC Printed Board Process Capability, Quality, and Relative Reliability (PCQRR) Database was developed by IPC and Conductor Analysis Technologies Inc. in 2001 for designers, purchasers, assemblers, and manufacturers of PCBs. It gives board buyers a way to compare board fabricators, and fabricators a way to compare their processes to the industry at large.

Invotec Strengthens Euro Team with New Appointments

Invotec Group is delighted to announce the appointment of Thomas Witt and Monika Braun as sales agent and sales assistant for Germany. Witt joins the company with extensive experience as a sales account manager, primarily within the high-reliability PCB sector, whilst Braun has a strong customer service background in the PCB industry with a particular focus on quick turnaround orders.

Candor Highlights Cutting-edge PCB Manufacturing

Candor President Yogen Patel remarks, “We’re extremely excited over the success we’ve had achieving these high-end, technical builds. With the speed at which the industry changes these days, Candor wants to be ahead of the pack, at the forefront of technology.

FPCB Report: Mektron Suffers First Loss

The world’s largest FPCB company, Mektron, suffered its first loss since its establishment, due to three main reasons: HDD and ODD markets contracted; the company began to intervene in the price war; and the company’s 45% output came from China where RMB appreciation and rising labor costs eroded profits.

Multiline Restructures Business; Sharpens Focus

Multiline Technology has restructured its business to improve consistency and dependability while delivering custom equipment and spare parts. In the last few years, the company’s business has changed to comprise predominately multiple camera, very tight tolerance, and large format post etch punches.

NCAB Expands U.S. Presence, Acquires M-Wave

One of the world’s largest suppliers of PCBs, NCAB Group, has acquired 100% of M-Wave International LLC’s PCB Division. Bob Duke, former president of M-Wave’s PCB Division, commented, “Being selected by NCAB to be a part of their U.S. team is a great compliment. As the PCB supply market continues to evolve, I felt this was an excellent time for M-Wave to expand its resources.”

Matrix Opens New “Value-added” California Warehouse

Branch Manager Jim Alves reports that the new warehouse is now in full operation. With the ongoing success of Panasonic High-Speed laminates, Jinzhou Carbide Tools, and Agfa Specialty products, the company is committed to expanding its services and presence in this region.

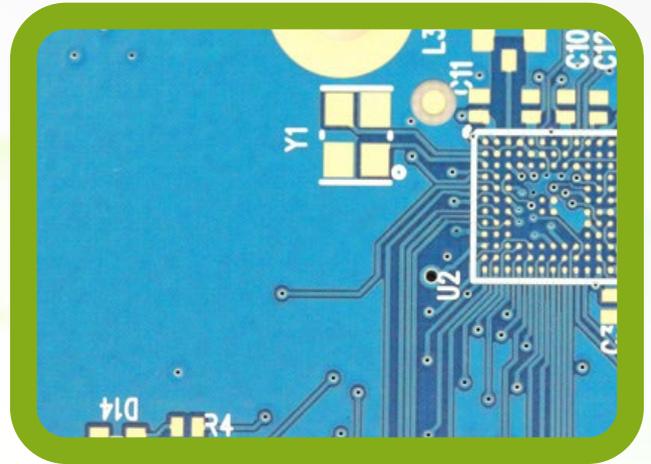
Technology Convergence Critical for PCB Fabrication

The PCB industry is showing signs of life, which indicates that the pendulum is swinging in a more positive direction economically, but we’re not quite ready to uncork the champagne. A June 2013 report by Research & Markets forecast that the global PCB fabrication industry alone will reach about \$94 billion in 2017, with a compounded annual growth rate (CAGR) of 8.1% during this period.

Multilayer Technology Nets 2014 Best of Irving Award

Various sources of information were gathered and analyzed to choose the winners in each category. The 2014 Irving Award Program focuses on quality, not quantity. Winners are determined based on the information gathered both internally by the Irving Award Program and data provided by third parties.

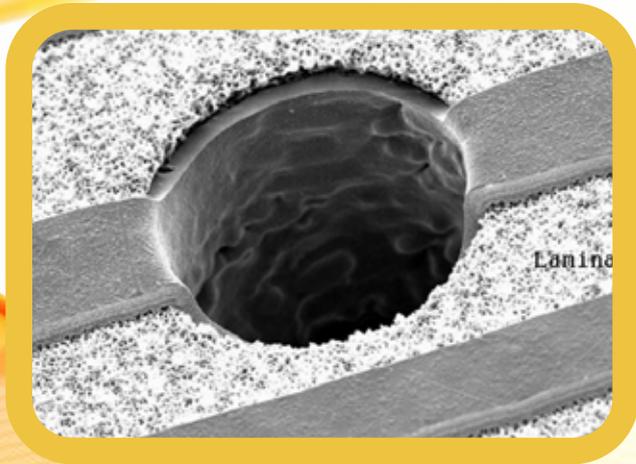
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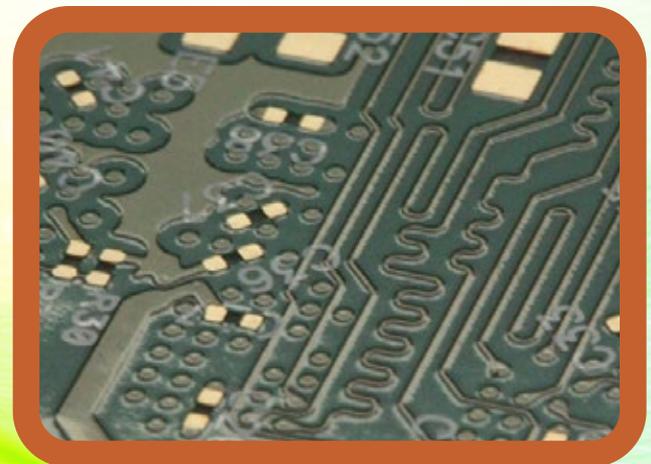


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Concurrent Design



by **Barry Olney**

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With the traditional PCB design process, the designer executes each stage of the design in sequence. But, as designs become more complex and time-to-market schedules become more demanding, we must take advantage of pre-layout simulation, and simultaneous process design in order to beat the competition. The pressure is on engineering managers to achieve more with their existing resources, although the design tasks have become more complex with increased levels of functional integration.

Concurrent design is the practice of developing products in which the different stages run simultaneously rather than consecutively. It decreases product development time and also the time-to-market, leading to improved pro-

ductivity and reduced costs. Concurrent design is a relatively new process strategy and although the initial implementation can be challenging, the competitive advantage means it is beneficial in the long term. It eliminates the need to have multiple design iterations, by creating an environment for designing a product right-first-time.

Typically, a high-speed computer based product takes two to three iterations to develop a working prototype. However, these days the product life cycle is very short and therefore time-to-market is of the essence. One board iteration can be very costly, not only in engineering time, but also in the cost of delaying the product's market launch. This missed opportu-

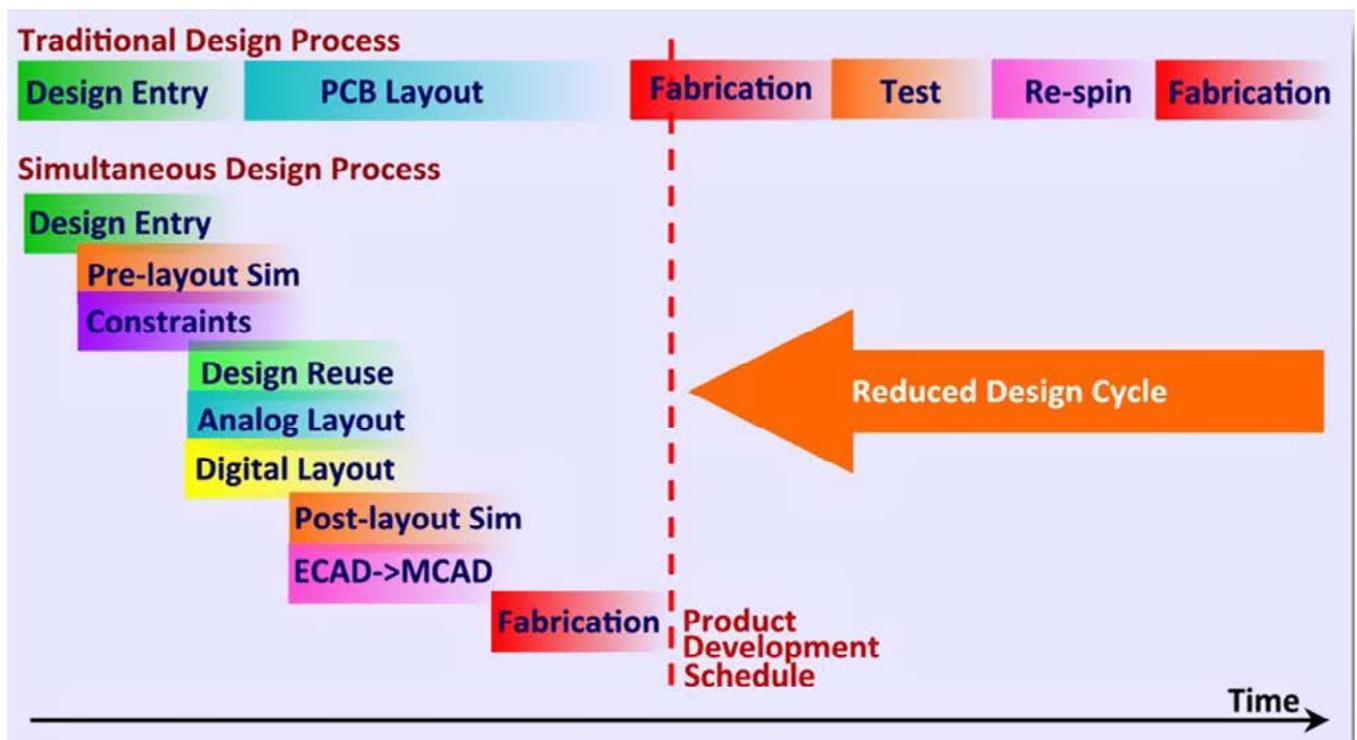
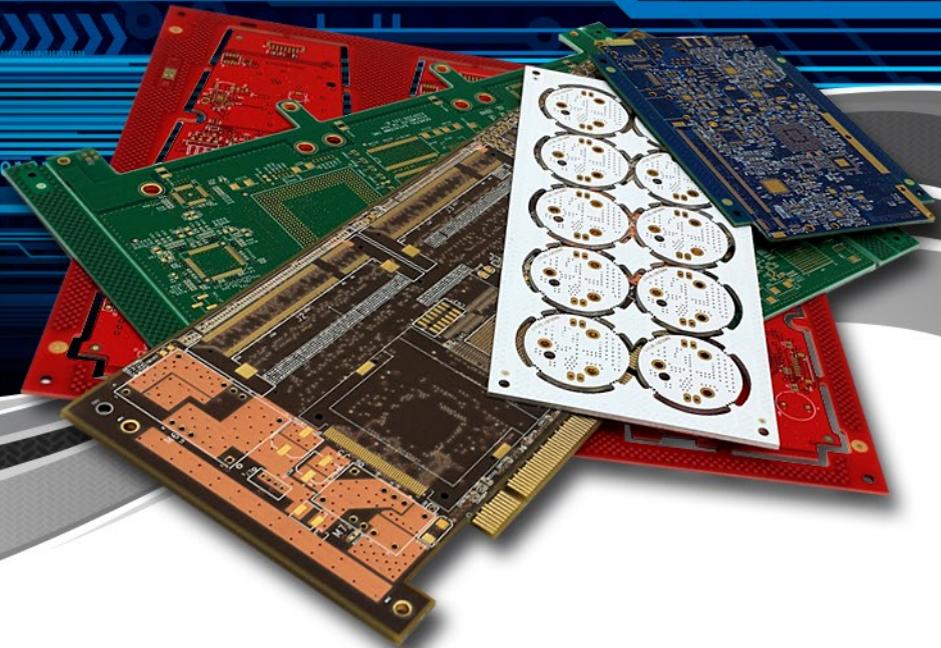


Figure 1: Traditional design process compared to the simultaneous design process.

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CONCURRENT DESIGN *continues*

nity could cost hundreds of thousands of dollars. All of the above impact on company profit by increasing prototype costs and the time-to-market. Computer-based products have a very small market window these days (e.g., one year). If the product is delayed by six months (e.g., two re-spins) then the company has lost half its projected return.

Figure 1 illustrates the traditional design process compared to the simultaneous parallel design process. Pre-layout simulation can be done during design capture to establish the required design constraints. Functional sections of previously developed “golden” boards can be reused giving high confidence in performance and multiple designers can be employed on the same layout. Post-layout simulation and mechanical integration can be done towards the end on the layout to ensure compliance to specification prior to fabrication. This process can dramatically reduce development time.

The significant business benefits of concurrent engineering make it a compelling strategy. Introducing concurrent engineering results in:

- Competitive advantage—reduction in time-to-market means that the business gains an edge over their competitors.
- Enhanced productivity—earlier identification of design problems means potential issues can be corrected sooner, rather than at a later stage in the development process.
- Reduced development time—development of high-performance products, in less time and at a reduced cost.

Process improvement is a systematic approach to ensure a development team optimizes its underlying processes to achieve more efficient results. Process improvement is an aspect of organizational development in which a series of actions are taken to identify, analyze and improve existing design processes to meet new goals and objectives, such as increasing profits and performance, reducing costs and accelerating schedules. These actions often follow a specific methodology or strategy to increase the likelihood of successful results. There are many ways to improve efficiency in the PCB design process:

1. Simulation: stackup planning, PDN analysis and signal integrity
2. Design reuse
3. Collaborative PCB design
4. Virtual prototyping: ECAD/MCAD collaboration

1. Simulation

Pre-layout analysis allows a designer to identify and eliminate signal integrity, crosstalk and EMI issues early in the design process. This is the most cost-effective way to design a board with fewer iterations, rather than starting with the “find-and-fix” based post-layout simulation.

There are multiple facets to pre-layout analysis including:

- Stackup planning for controlled impedance, SI, crosstalk, and cost control.
- Dielectric material selection for manufacturing yield, and high-frequency operation.
- PDN optimization for product reliability and cost reduction.
- I/O buffer and drive strength selection.
- Topology optimization.
- Termination strategy.
- Floor planning for critical components.
- Deriving layout routing constraints, including trace width, spacing and length matching.
- Signal Integrity analysis to meet the design specifications, with respect to noise margins, timing, skew, crosstalk, and signal distortion.

Although the trace impedance is specified on the fabrication drawing, stackup planning is often left until Gerbers are produced and the deliverables are sent to the fab shop. However, generally, the virtual dielectric material selection and trace width and clearance provided do not match the desired controlled impedance. So, the CAM engineer returns the calculations that may require trace width and clearance changes. This is not what we need at the end of the design cycle. This flawed process can be attributed to the fact the PCB designers do not have access to field solvers during layout and either have to wait until an SI engineer analyses

the design, or—as commonly occurs—wait for the fab shop's report.

ICD has responded to this challenge by recently developing a bi-directional interface from the ICD Stackup Planner to Altium Designer 14. This new interface allows the designer to exact the rigid/flex stackup from the Altium Layer Stack Manager into the Stackup Planner. High-speed materials (up to 40GHz) can be merged from the Dielectrics Materials Library, of over 8,800 materials, and the impedance of multiple differential pairs can be simulated on the same substrate. Once finalized, the designer simply exports the data, including PTH and blind and buried microvia spans, trace width and clearances and differential pair rules back into Altium Designer. This allows the designer to route to impedance. A fabrication drawing of the stackup specifying all HDI requirements is also exported to Excel. (Thus ends my shameless plug. But it does work well.)

Similarly, PDN analysis is often overlooked completely. I can't stress enough how important low AC impedance is for high-speed designs that demand high-current drain at low

core voltages. If the impedance is high at either the fundamental frequency or any of the odd harmonics, then higher levels of electromagnetic radiation can be expected. This has a direct impact on product reliability and the ability to pass EMC.

For years, application notes have recommended the use of three decoupling capacitors per power pin. This generally consisted of a 100nF, 10nF and a 47pF capacitor. The idea behind this was that different values provided current at different frequencies, but unfortunately not the right frequencies, as all boards are different. As can be seen in Figure 3, multiple capacitors per decade are required to keep the effective impedance, of the PDN, below the target up to the required bandwidth. If too few capacitors are used, spread widely across the frequency domain, then there is a good chance that anti-resonance peaks in the PDN will exacerbate the problem.

Also, in this case, I have incorporated the use of 3M Embedded Capacitance Material (ECM) which is the only practical way to pull the PDN low around the GHz region. This ma-

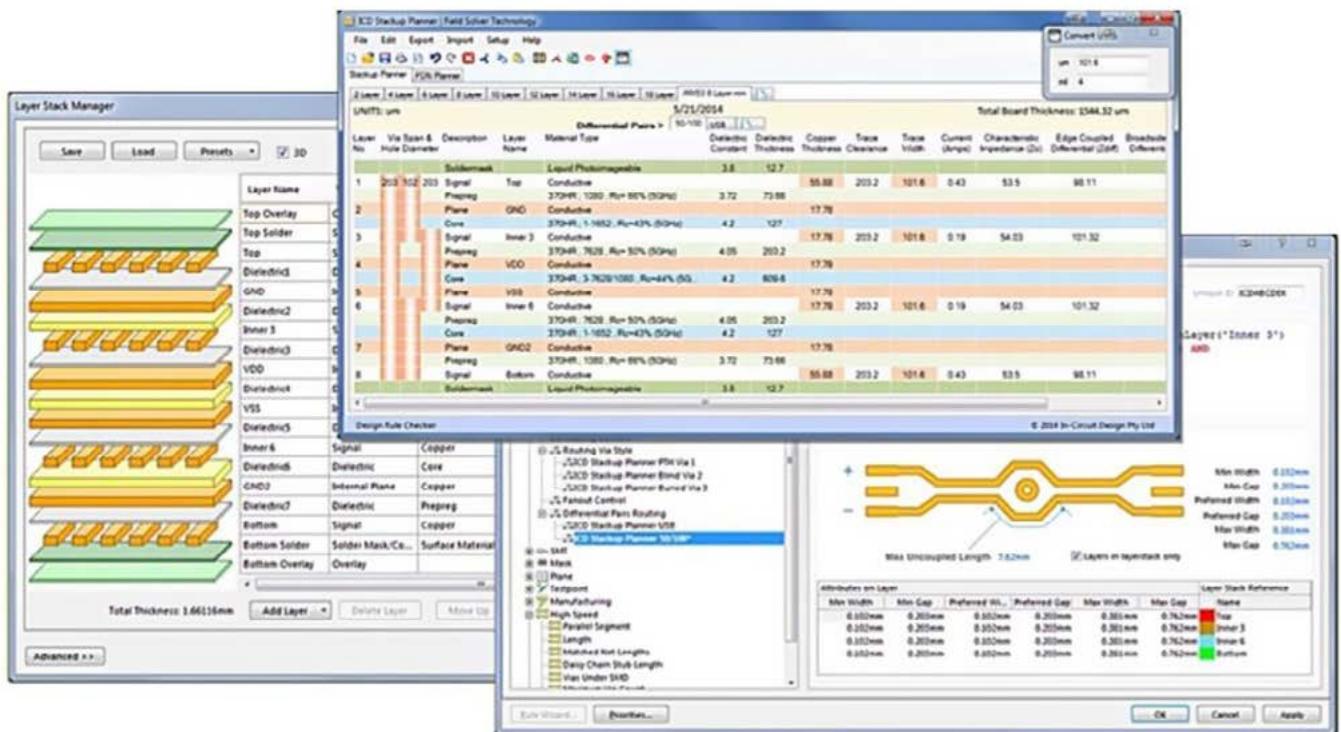


Figure 2: Integration of the ICD Stackup Planner and Altium Designer 14.

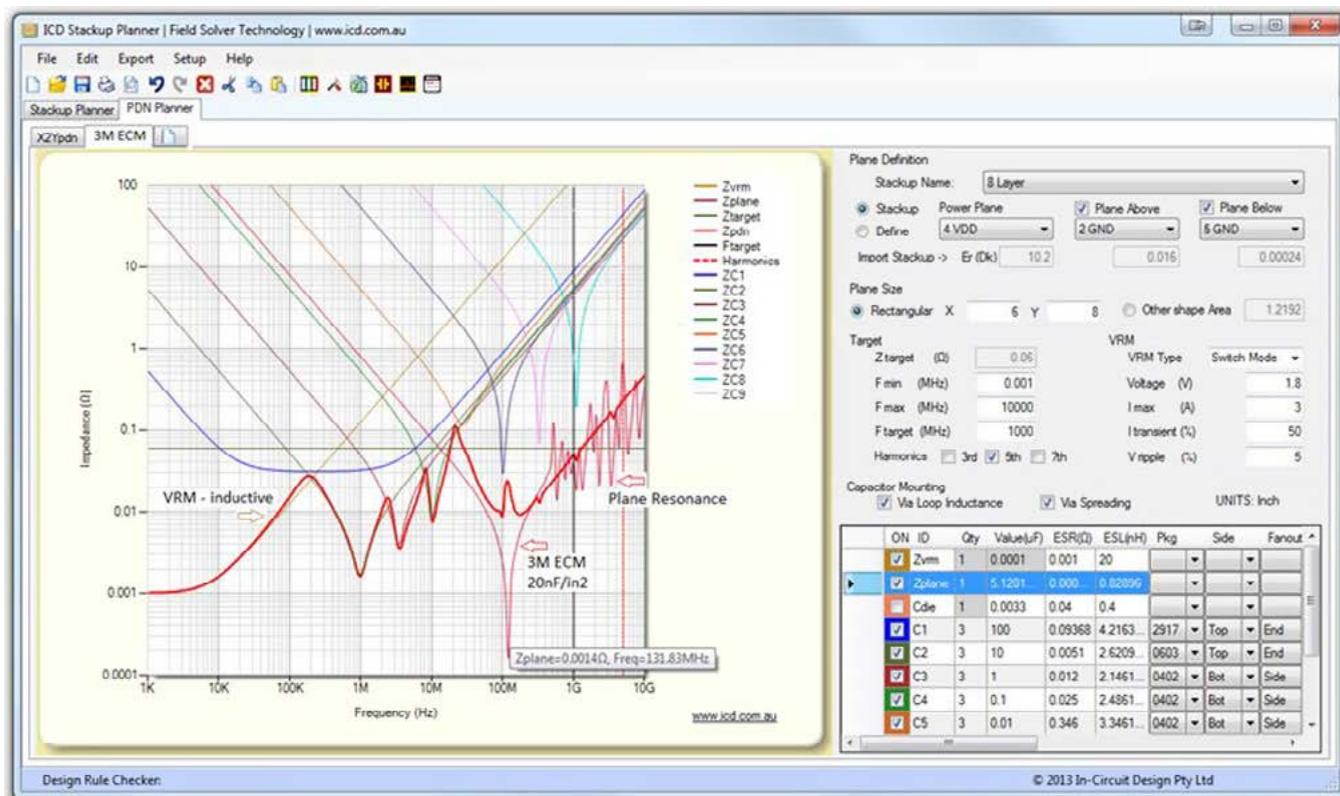
CONCURRENT DESIGN *continues*

Figure 3: PDN Analysis using multiple capacitors per decade and 3M ECM planar material.

material provides 20nF/in² which is an excellent way of amassing additional planar capacitance. The tight integration between the ICD Stackup Planner and PDN Planner allows the automatic transfer of the effects of different dielectric materials to the PDN for analysis.

2. Design Reuse

If the same switching regulator or processor and memory chips, for instance, are used on consecutive designs, creating a library of matching “reuse blocks or snippets” for schematic and PCB makes the best use of existing design elements for future designs. Simply add a sub-circuit block to the schematic, transfer to the PCB database, and load a predefined layout block including component placement, tracks, copper and text. Whether it is used for multiple channel designs, critical digital circuitry, RF circuit blocks, or just to replicate a commonly used layout pattern, design reuse will save time and ensure repeatability of design: a proven, tested, working solution to just drop into place.

3. Collaborative PCB Design

For many years designers have attempted team design, to avoid the seemingly unavoidable routing bottleneck, using multiple PCB designers to route different sections of the board at the same time.

Schematics and layouts can be divided into function blocks for example: power supply, analog, digital, memory and SERDES. Or, multiple designers can work on the same section simultaneously in different parts of the world. I have done this many times, providing an over-night design service for US based companies. Co-design implies that a group of designers can work on a design at the same time and all their design inputs are accepted. But obviously, this is full of traps and there has to be some form of priority when merging databases.

In recent years, some EDA companies have developed tools to enable designers to collaborate, compare and merge designs and these capabilities include:

- The ability for multiple designers to access and merge a PCB database.
- A mechanism to accurately identify and compare databases.
- The capacity to display the differences and allow the lead designer to informatively select the best outcome of any conflicts.

Also, live collaboration is now possible. Each designer defines a work region and this is displayed clearly on each designer's database view, enabling the avoidance of conflicts. Other tools allow designers to work with the one database in real time with no need to partition and re-assemble the design. The tool manages edits from all users and continually sends updates to the entire team. Team collaboration can result in extreme reductions in design time with a typical 13 week complex design being reduced to five weeks and in some cases, providing a 60% increase in productivity.

4. Virtual Prototyping: ECAD/MCAD Collaboration

Like simulation, the integration of mechanical aspects of the design process is generally not considered until late in the design process. This leaves the design open to change once the mechanical issues have been identified—hence delay.

With stylish housings, how do designers fit the tightly packed, complex shaped electronics into the box? Traditionally, designers assumed there was no problem and simply handed over the CAD drawing to be manufactured. But after years of denial, it has been concluded that this approach did not work too well.

The challenges that many companies face when they use both 2D and 3D solutions is that these tools are fundamentally disconnected. A design that is created in 2D, in order to be reused in 3D, has to either be imported or recreated into the 3D tool. This disconnection

causes inefficiencies in the design process. Also, any changes that are made in the 2D environment are not automatically reflected in 3D. This means that the user either has to go through the re-import process or create the change twice.

However, this issue has been overcome by some tools that bridge the gap between electronics and mechanical design so that you can be assured that your product fits together every time. This is accomplished by using 3D DRC interference checking at the PCB design level and dynamically linking the 2D back into the 3D design space. This is a great solution to the problem—a native 3D environment.

In conclusion, concurrent design offers significant benefits to product development teams providing a competitive advantage by reducing time-to-market, and cost while providing high-performance, reliable products on time. Delivering a product on schedule provides higher returns due to a longer presence in the market. This all of course leads to higher profits.

Points to Remember

- The traditional PCB design process is to execute each stage of the design in sequence.

- Concurrent design is the practice of developing products, in which the different stages run simultaneously.

- Typically, a high-speed computer based product takes two to three iterations to develop a working prototype. This impacts company profit by increasing prototype costs and the time-to-market.

- Concurrent engineering gives a competitive advantage, enhances productivity and decreases development time.

- Process improvement is a series of actions taken to identify, analyze and improve existing design processes.

“
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 ”

CONCURRENT DESIGN *continues*

- ICD's bi-directional Altium Designer interface allows early detection of stackup and PDN issues.

- The efficiency of the PCB design process can be improved by simulation, design reuse, co-design and virtual prototyping.

- Pre-layout analysis allows a designer to identify and eliminate issues early in the design process.

- Design reuse will save time and ensure repeatability of design: a proven, tested, working solution to just drop into place.

- Team collaboration can result in extreme reductions in design time with a typical 13 week complex design being reduced to five weeks.

- Virtual prototyping ensures that your product fits together every time by using 3D DRC interference checking at the PCB design level. **PCBDESIGN**

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[and the PCB Design Process](#), and [Power Distribution Network Planning](#)

2. Altium Documentation: Collaborative PCB Design

3. Wikipedia: Business Process Improvement Randall Myers, Mentor Graphics: Concurrent Design One Team One Virtual Location

4. Concurrent Engineering: [What is Concurrent Engineering](#)

5. The ICD Stackup Planner and PDN Planner are distributed globally by [Altium](#)



Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, [click here](#).

video interview**Sunstone on New Initiatives, Website and More**

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Matt Stevenson, the new marketing manager for Sunstone Circuits, discusses some of his plans for the prototype manufacturer, including fine-tuning the website. He also explains the company's focus on Lean manufacturing, and gives an outlook on the industry.



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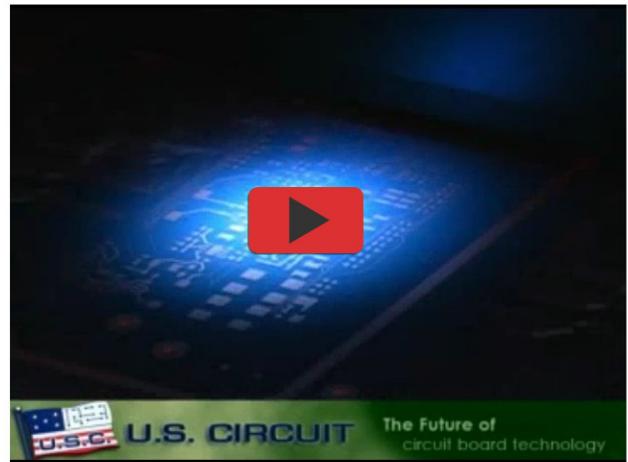




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Considering Creepage and Clearance

by **Amit Bahl**
SIERRA CIRCUITS

Several years ago, my company published a guide to the design and manufacture of PCBs that would carry very high voltage, potentials up to 40,000V. Much of the advice in that brief regards a narrow project category, and I have an idea that a review of the basic layout precautions for any board that would carry what is considered hazardous voltage—greater than $30V_{RMS}$, or 60V dc—would have a much wider audience. Reiterating such rules now and again could save a lot of headaches and perhaps liability down the road.

If the system or product for which your board is destined must meet IEC or UL standards, the minimum distance permitted between conductors that are subject to hazardous voltage will include a wide margin for safety, which depends

on the peak working voltage, laminate material, operating environment (moisture, particulates, altitude), circuit location relative to human access or proximity, and whether the traces involved are on an internal or outer layer. The spacing required on outer layers also depends on whether traces are coated or bare.

Determining what spacing to use is simple, if your system or product requires compliance to international safety standards. Find the standard relevant to the product category and adhere to the tabulated values with respect to the details of your application as noted. For example, IEC-60950-1 (2nd edition) is the document to consult for most IT products to be sold internationally that are powered from ac mains, or batteries, and applies both to the primary



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CONSIDERING CREEPAGE AND CLEARANCE *continues*

side and the dc secondary circuits within those products. Starting with section 2.10.3, midway through the document, the standard defines what clearances are required so that over-voltages, including transients and peak voltages that may be generated within the equipment, cannot cause faults. A series of tables, 2J through 2M, explains how to calculate clearances with respect to the details of your application. Next, section 2.10.4 explains how to determine the spacing required for creepage.

Clearance vs. Creepage

What's the difference between clearance and creepage? Clearance is the shortest distance between two conductors measured through air. Creepage is the shortest distance between two conductors, measured along the surface of the insulation separating them. Consider the ways an electrical fault between conductors can occur if the clearance or the creepage spacing is too small. If the clearance is too small, a transient over-voltage event can result in arcing between the conductors, especially if there is dust in the air or humidity. This is a virtually instantaneous fault that does not recur until another such over-voltage event. Faults resulting from insufficient spacing for creepage can take much longer to occur. Over time, usually stemming from dust buildup and moisture, a path (in other words, a track) for current to leak from one conductor to another can develop and cause a gradual breakdown of the surface of the insulating material between them. The mechanism for this is not a voltage spike—

though that could contribute—but the continual presence of high voltage combined with an insulating material whose comparative tracking index (CTI) is too low.

CTI is a measure of a material as an electrical insulator and is expressed as the voltage at which the surface of a material breaks down under a standardized test. The manufacturers of PCB laminates publish CTI figures for their products. For convenience, the breakdown voltages are lumped into six categories: The highest rating is 0 for withstanding values of 600V and greater and the lowest is 5, for less than 100V. For example, conventional FR-4 has a CTI of from 175–249 volts, which places it in rating category 3.

The paramount objective of all electrical safety standards is of course to prevent any danger of shock. If no one will ever be near a circuit while it is powered, the clearance and creepage allowances among its conductors that are subject to hazardous voltage can be the minimum that ensure the circuit will function and not deteriorate. IEC-60950-1 specifies five increasing levels of mandatory insulation related to the physical location of a circuit relative to human contact, the voltage, and the operating environment. Naturally, the best tactic to avoid the danger of shock or circuit degradation is to space traces as far apart as possible but very often that distance will not meet creepage requirements. What can be done in those cases?

If turning to a material with a better CTI is not feasible, routing a slot in the space between

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Consider the ways an electrical fault between conductors can occur if the clearance or the creepage spacing is too small. If the clearance is too small, a transient over-voltage event can result in arcing between the conductors, especially if there is dust in the air or humidity. This is a virtually instantaneous fault that does not recur until another such over-voltage event. Faults resulting from insufficient spacing for creepage can take much longer to occur.
 ”

two traces can increase the creepage distance. Leakage from one trace to the other along the laminate surface would have to travel around the air gap. Alternatively, a vertical barrier of insulating material could be placed in the space, which would increase both the creepage and clearance distances.

Keep in mind the spacing on assembled boards when you consider creepage and clearance requirements for layout. The distance between an uninsulated edge of a charged component and the edge of an adjacent component could be too small to meet a clearance requirement, even though the creepage distance between their traces is sufficient. Moreover, there may be some operations needed during assembly to meet clearance requirements, for example, applying potting compound to isolate the leads on the package of a power semiconductor from a nearby component.

If your project does not require compliance with a particular safety standard, you can rely on the latest version of IPC-2221, the gener-

ic standard for PCB design, for clearance and creepage guidance. In any case, consultation with your PCB fabricator and assembler regarding suitable materials and design alternatives will help you achieve a safe product that meets your performance objectives at the lowest possible cost.

Our quick trip through the basics of laying out boards that involve hazardous voltage amounts to just a first step, simply an opportunity to point to out some helpful and hopefully familiar guideposts as you start your journey. Consider this presentation my personal opinion only and certainly not legal advice. **PCBDESIGN**



Amit Bahl directs sales and marketing at Sierra Circuits, a PCB manufacturer in Sunnyvale, California. He can be reached by [clicking here](#).

video interview

Printed Circuit Handbook, 7th Ed., Coming Soon

by *Real Time with...*
IPC APEX EXPO



Clyde F. Coombs Jr., editor of the venerable Printed Circuit Handbook, discusses the upcoming 7th edition, and what readers can expect. He explains how the book's content has evolved over the years, and why some readers are not "board guys" in the classic sense.



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Accelerating the SI Learning Curve: Bogatin's SI Academy

by Bert Simonovich
LAMSIM ENTERPRISES

Last year, Dr. Eric Bogatin, the “Signal Integrity Evangelist,” announced the end of his famous signal integrity classes. At the time I remember thinking to myself, “What’s next for Eric?”

If you know Eric, like I do, you realize that the end of one phase of his career usually means the start of the next one. And now we know what that is. You see, Eric has been busy the last six months preparing to launch his new [Teledyne LeCroy Signal Integrity Academy](#) Web portal.

Eric is currently a signal integrity evangelist with Teledyne LeCroy, and on the faculty at the University of Colorado at Boulder, where he recently moved to from Kansas.

He has a BS degree in physics from MIT, and MS and PhD degrees in physics from the Uni-

versity of Arizona in Tucson. He has held senior engineering and management positions at Bell Labs, Raychem, Sun Microsystems, Ansoft, and Interconnect Devices. Prior to joining Teledyne Lecroy, he ran a successful company providing signal integrity training, Bogatin Enterprises, along with his wife Susan.

I met and got to know Eric in 2008, when we collaborated on our first DesignCon paper for 2009, [Practical Analysis of Backplane Vias](#). We were privileged to win a Best Paper award that year. Since that time we have worked on several projects together, and have become good friends. The last project we worked on was for a DesignCon2013 paper titled, [Dramatic Noise Reduction using Guard Traces with Optimized Shorting Vias](#), which also won a Best Paper award.

Over the years, I have studied much of Eric’s work through his papers, articles, webinars, blogs and content from his previous website. I always made it a point to catch all of his presentations at any conferences I attended. I have his first edition book, [Signal Integrity Simplified](#) as well. It has been one of my go-to books when starting any of my research projects or trying to grasp concepts.

Like the other go-to signal integrity books in my library, it is well marked and used, though this one seems more so than others. Having the

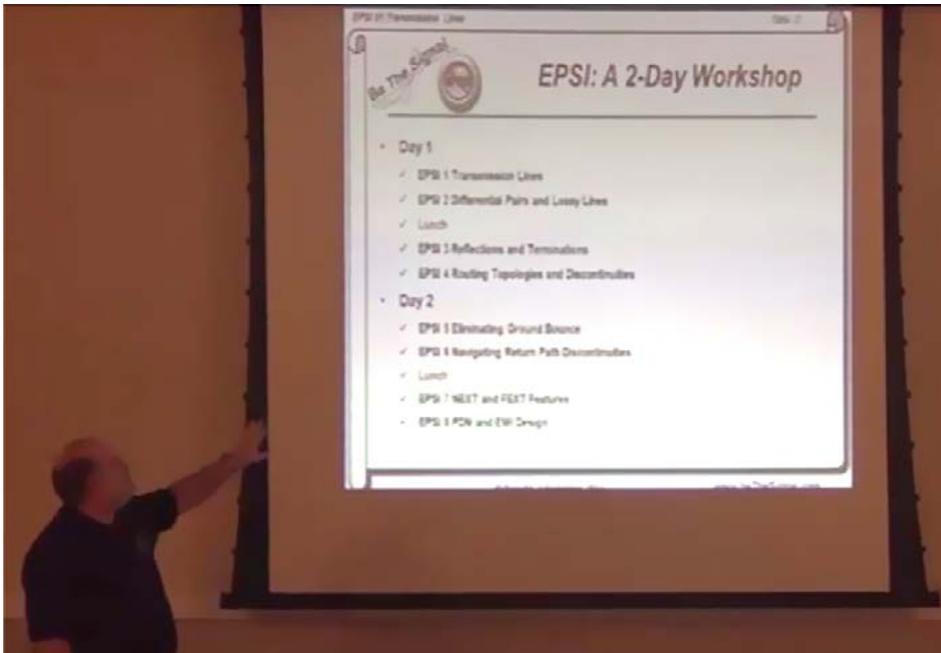


Figure 1: Eric Bogatin preaching to the signal integrity choir.



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ACCELERATING THE SI LEARNING CURVE: BOGATIN'S SI ACADEMY *continues*

privilege of working with Eric has also enriched my learning experience.

Over the years, I always wished I could have attended some of his classes, but due to travel cost and time away from the office, it could never be justified. Now, with the beauty of the Internet, the classes can come to me. I can choose to watch what I want, when I want, as many times as I want, and on whatever device I want. My iPad is a perfect choice! For a yearly subscription fee for individuals or corporations, anyone who desires has the opportunity of watching any class or lesson, anytime.

The content is in the form of short, concise video lessons lasting from 5–15 minutes. Slides are available for download and I suggest downloading the respective slides prior to watching the presentation so you can make notes as you go along. The initial three courses, Essential Principles of SI; Advanced Gigabit Channel Design; and S-Parameters for SI, are based on his most popular public classes. Once subscribed, you are offered an “all you can eat buffet” of

these lessons. There are more courses and lessons planned in the future.

If you have always wanted to accelerate your signal integrity learning curve, then the Tele-dyne LeCroy Signal Integrity Academy may be the right place for you to start. **PCBDESIGN**



Bert Simonovich spent 32 years at Bell Northern Research/ Nortel Networks as an electronic engineering technologist. During his tenure, he helped pioneer many advanced technologies into products, and later went on to specialize in high-speed signal integrity and backplane design. After leaving Nortel in 2009, he founded Lamsim Enterprises Inc., where he provides innovative signal integrity and backplane solutions as a consultant. You may contact Bert through Lamsimenterprises.com.

video interview

IPC Printed Electronics Standards Update

by *Real Time with...*
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Taiyo's Josh Goldberg explains some of the ongoing work behind IPC's printed electronics standards. IPC has launched a number of committees devoted to printed electronics, allowing North American technologists to work with organizations in other countries.



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Mil/Aero007 News Highlights



Dragon Circuits Adds Up-cycled PCBs to Drone Division

Since Dragon started their UAV/drone branch earlier this year, the first step to up-cycle scrap material for drones was an obvious one. Vice President Rajan Babaria comments, "Many circuit boards are layered and quite durable. It was clear this would make them a great candidate to be used as a drone frame."

IPC Offers One-day Conflict Minerals Conference

Continuing its long-standing conflict minerals educational outreach efforts, IPC is offering a one-day conference, "Conflict Minerals: Staying Current in a Changing Landscape," July 10, 2014, in Santa Clara, California to provide manufacturers up-to-the-minute information on the changing landscape of conflict minerals.

Invotec's Flex Rigid PCBs Earn ESA Approval

Having secured its first approval from the European Space Agency (ESA) earlier this year, Invotec Group is delighted to announce that it has now gained approval for sequential flex rigid boards.

i3 Electronics to Supply PCBs for Satellite Use

The company announced that an industry-leading aerospace and telecommunications firm has awarded the company a substantial contract for the supply of its high-complexity, high-reliability PCBs for a satellite application.

Gardien Services USA Debuts A8/G60 Test Combo

Gardien Services USA is happy to announce the addition of its new Acceler8/G60 Flying Probe combination to its ever expanding Quality Assurance offerings available in Plymouth, Minnesota.

FTG Secures LTA for PCBs for Wing Platforms Use

Firan Technology Group Corporation has been awarded a new three year long term agreement (LTA) from one of the leading global OEMs sup-

porting the aerospace market. The agreement incorporates a variety of high-technology PCBs for use on key fixed-wing platforms including the Boeing 787, Airbus A350, A400M, and the Bombardier C-Series.

Ventec Europe Announces AS9100 Rev C Accreditation

The company is proud to announce that the quality management system at its Leamington Spa, UK, headquarters is now fully accredited to AS9100 Revision C, in accordance with the Aerospace Supplier Quality System Certification Scheme EN9101:2011, EN9104-001:2013.

Possible Expansion of Anti-counterfeiting Efforts

Applied DNA Sciences' SigNature DNA marking program is currently in use by several defense industry suppliers for application on electronics deemed to be at high risk for counterfeiting. A House committee has begun consideration of the DoD's fiscal year 2015 budget request, taking particular interest in efforts to combat the intrusion of counterfeit parts into the military supply chain.

SIA Lauds DoD Rule Reducing Counterfeit Semicon

The Semiconductor Industry Association (SIA), representing U.S. leadership in semiconductor manufacturing and design, has applauded a newly finalized DoD rule that reduces the risk of counterfeit semiconductor products being used by our military by implementing needed safeguards in the procurement of semiconductors and other electronic parts.

Aerospace & Military APU Market to Hit CAGR of 3.92%

APU use the same fuel as the aircraft's engines and generally account for about 2% of the total fuel consumption on a given mission. The global aerospace and military APU market is estimated to be \$1,527.89 million in 2014 and is projected to register a CAGR of 3.92% to reach \$1,851.69 million by 2019.



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FAILURE

Choosing the Right PCBA Repair Shop

by Ron Fukui

PSI REPAIR SERVICES

No matter what brand or board type you're working with, it's impossible to escape the reality that PCBs are inherently failure prone. Planning for when, rather than if your circuit boards will malfunction is an approach that reduces costs and relieves future headaches.

Shipping out your faulty PCBA for service can be stressful when you're on a tight production schedule and board failure has already led to downtime, but it pays to have practiced technicians discover the root cause of a circuit board's failure and analyze the extent of its damage.

In addition to physical damage to the circuit card, like cracks and corrosion, discrete and power components can deteriorate for a wide range of reasons, including extreme heat, over/

under voltage surges and sags, and age; contaminants like grime and dust are also frequent sources of trace damage. Contacting a repair provider is the best way to ensure that your circuit board assembly functions properly once it's reinstalled, and—more importantly—that your industrial electronics won't fail again a few weeks down the road.

Even though factories save millions every year by repairing and/or reworking circuit boards, the guesswork associated with choosing a repair shop and anxiety about the quality of the craftsmanship they offer convinces many plant managers to purchase brand new replacement boards instead. This is a costly decision in the short and long term: In addition to spending an arm and a leg for new boards, OEMs don't provide preventive and corrective repair recommendations and actions to help your electronics equipment (not just the circuit

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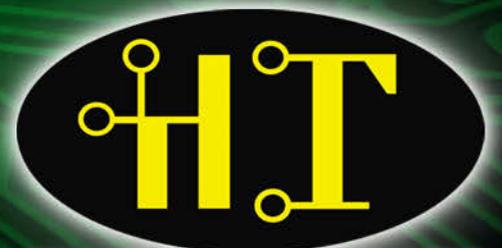
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CHOOSING THE RIGHT PCBA REPAIR SHOP *continues*

board part that needs to be replaced) exceed its performance expectations.

What criteria should guide your selection of a service provider if you've decided to repair or rework your circuit board? We recommend focusing on "Three Es"—expertise, equipment, and economies of scale.

I. Expertise

Circuit board repair remains a labor-intensive process at its core, demanding highly skilled handiwork and technical knowledge.

One of the benefits of working with service-centric repair companies, as opposed to OEMs, is that their profitability depends on the capabilities and customer service of their engineers and technicians. Their ability (or inability) to deliver high-quality and reliable repairs before deadline—especially when large or complex projects are on the line—powers (or stunts) their growth.

Subsequently, longevity is an important factor to consider when choosing a repair company; there's a reason why some repair providers have been operating and growing for several decades and others stagnate after a few years in business.

Certifications are another obvious factor to bear in mind: If a company's technicians aren't qualified in ESD and IPC repair and rework standards, you shouldn't trust them to handle advanced microprocessors and digital signal processor circuits.

Similar to this, while not advertised publicly, ongoing specialized training for technicians is a sign of a competent independent service provider (ISP) committed to competing on a global stage. Technicians should be able to operate the latest diagnostic technology and also develop world-class programs for handling and testing parts.

In addition to having the ability to quickly diagnose a failing circuit board component, execute its repair, test its performance, and provide an aggressive warranty, repair companies should also be eager to offer value-added technical services. These might include:

removing and replacing stressed parts, improving inefficient design with stronger, more reliable technology, remanufacturing unsalvageable or obsolete components, manufacturing custom-designed products and implementing end-of-life (EOL) strategies, among others.

II. Equipment

Everything else being equal, up-to-date diagnostic and testing instruments can make the difference between a 1-day turnaround and a 3-day turnaround on an urgent project. For this reason alone, successful PCBA repair companies invest millions to equip their facilities with the most state-of-the-art equipment available.

Specifically, ISPs need a mixture of equipment in order to address the digital, analog, and power sections of circuit cards. A properly outfitted PCB repair facility will incorporate the following equipment into their production process:

1. In-Circuit testers perform a powered, in-circuit logical test of digital and many analog ICs, as well as signature analysis of the chips. These tests check for the Boolean functions from digital chips, and also provide a signature analysis of dynamic operation. Unknown chips can be identified by its Boolean output. The Diagnosys PinPoint System also contains libraries of digital chip pinouts to assist the technician in troubleshooting, and can determine wiring patterns of the circuits.

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CHOOSING THE RIGHT PCBA REPAIR SHOP *continues*

2. Data I/O programmers read, verify and store data in programmable logic devices, such as PROMs, microprocessors and memory devices. A master database of all programmable devices is stored for current and future repairs.

3. Using Hot air IC installation & removal systems, surface mount ICs can be subjected to temperature-controlled hot air to reflow solder. A vacuum pickup tool is used to remove or install the chip with the help of a magnifying CCD camera.

4. Signature analysis is the primary diagnostic tool for PCB repair activity. It works by applying a current-limited AC signal across two points of a semiconductor junction. The current flow causes a vertical deflection of the CRT trace, while the applied voltage causes a horizontal deflection. Together, they form a unique V/I signature that represents the overall health of the junction under test. Analyzing the deflection signature tells us whether the component is good, bad or marginal. Many units also have the internal ability to fire gate-triggered devices while viewing the V/I curves.

5. Oscilloscopes of various bandwidth, both analog and digital, are used to analyze voltage waveforms under power.

6. Function generators are used to simulate square, sinusoidal or triangle wave input and trigger signals.

7. Digital volt meters (DVMs) can measure voltages from 3.5 digits down to 6.5 digit precision at the selected measurement range.

8. Sencore cap & inductance meters are used to analyze capacitors for capacitance, equivalent series resistance (ESR), dielectric leakage and frequency response. Inductance meters are used for measuring similar attributes in coils.

9. Power supply load boxes are dynamic load banks for testing power supplies' capacities, hold-up time, and spike sensitivity.

10. Calibrators are reference systems traceable back to NIST standards for final adjustment of temperature, flow and pressure related products.

11. Mings are hand-held testers for identifying and checking various integrated circuits.

12. System or simulation testers provide a means to test assemblies from the connectors to determine entire functionality.

Furthermore, all equipment should be identified as either used for diagnostic work or for final repair (calibrated). All calibrated equipment should be on a scheduled gage program.

III. Economies of Scale

The best repair, rework, and overhaul options at the lowest price points are only sustainable if an ISP is highly scalable.

For example, larger repair shops can offer more agility by leveraging their inventory of new and refurbished circuit board assembly parts. This is especially important as it relates to emergency/rush repair services when customers are experiencing production downtime.

In addition to cost-effectively replacing defective circuit boards components with new and/or more reliable parts, plant managers, owners and operators want a full-service partner that can improve their equipment performance and operating efficiency as a whole.

Most repair shops, however, do not have the manpower, experience, and technology necessary to provide value-added PCB redesign and manufacturing services, for example—these are simply cost-prohibitive for small and medium-sized repair facilities.

Bottom Line

When your circuit board repair project is complete, the remanufactured, like-new condition board(s) should always meet the same industry specifications for performance as new PCBs. If you found a quality shop, you should expect that the parts will easily exceed the expected lifetime of the original board.

And when it's all said and done, choosing the right PCBA repair provider can save you up to 70% compared to the cost of buying replacement PCBs from the OEM. **PCBDESIGN**



Ronald D. Fukui is the director of engineering and technology for the Repair Services Division of PSI Repair Services. He is a former president and majority owner of FAST Inc., a company that provides repair services to the industrial equipment market.

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TOP TEN

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News

News Highlights from PCBDesign007 this Month

① **Mentor's Xpedition Path Finder Offers New Capabilities**

Mentor Graphics has announced its Xpedition Path Finder product suite, providing designers with the ability to assemble and optimize complex electronic systems, and thereby enabling improved design, increased chip performance, and cost efficiency.

② **Zuken Unveils Latest E3.series; Trims Manufacturing Costs**

Zuken announces manufacturing cost reductions through enhanced electrical design. The latest version of E3.series – Zuken's industry-leading electrical and fluid CAD software – contains integration with B&R Automation Studio, data export for drilling and milling machines, XVL output for Lattice viewer, and enhanced support for Komax.

③ **DesignCon 2015 Issues Call for Papers**

The DesignCon 2015 Call for Technical Papers, Panels and Tutorials is now open. DesignCon gives chip, board and systems design engineering community the unique opportunity to gather for four days of learning the latest design techniques, methodologies and tools around SI and PI, high-speed serial design, PCB design tools, test and measurement, and more.

④ **Ucamco's Integr8tor v8.3 Now Available**

Integr8tor works around the clock, automatically downloading and analysing incoming client design data, delivering accurate quote-ready data to the sales department, and in-depth design breakdowns together with design-rule, DFM and capability checks to the engineering and production departments.

5 Agilent Debuts ADS DDR4 Compliance Test Bench

Agilent Technologies Inc. has introduced Advanced Design System DDR4 Compliance Test Bench, which enables a complete workflow for DDR4 engineers, from simulation of a candidate design through measurement of the finished prototype. The solution is ideal for semiconductor companies developing DDR controller IP; those developing DRAM chips and DIMMs; and OEMs integrating the controller and DIMM into a system using PCB technology.

6 Streamlining PCB Design and Mfg Process for DIY Engineers

"FabStream offers the casual DIY user free comprehensive, yet easy-to-use PCB design tools readily available and integrated with manufacturing," said Rick Almeida, founder of DownStream Technologies. "We wanted FabStream to support those individuals who are less experienced in PCB design and manufacturing by eliminating design pitfalls that can lead to problems getting a board produced."

7 Altium, In-Circuit Design Partner for Altium Designer Extensions

Altium Limited, in cooperation with In-Circuit Design Pty Ltd. (ICD), has launched new extensions for Altium Designer for advanced stackup planning and power distribution network analysis to bring comprehensive high-speed design capabilities to the mainstream market.

8 Embedded Component Meeting: Process Variations

With the theme "PCB Design and Fabrication Process Variations for Embedding Passive and Active Components," Vern Solberg's presentation will focus on the six basic embedded component structure designs described in IPC-7092. He will make his presentation at the upcoming Embedded Component Meeting in Biltmore Santa Clara on September 10.

9 Intercept Expands to India with Tecnode Solutions

Intercept Technology Inc. announces its newest authorized reseller, Tecnode Solutions (P) Ltd. Tecnode's primary goal is to expand its RF and microwave solutions portfolio by selling Intercept's PCB, RF, and hybrid design software applications throughout India.

10 Letter: Longing for Light Table, but Happy With CAD Tools

"Zuken has amazing simulation software, and the cheaper packages are certainly catching up," says reader Steve Knobel. "Generally, with faster computers and ever-improving CAD software, life for PCB designers is good. There are days when I still long for the drawing board and light table, but the feeling doesn't last very long."

**PCBDesign007.com for the latest circuit design news—
anywhere, anytime.**



EVENTS

For the IPC Calendar of Events, [click here](#).

For the SMTA Calendar of Events, [click here](#).

For a complete listing, check out
The PCB Design Magazine's [event calendar](#).



[SEMICON West TechXPOT: Driving Automotive Innovation](#)

July 8–10, 2014

San Francisco, California, USA

[Ohio Expo & Tech Forum](#)

July 17, 2014

Cleveland, Ohio, USA

[SusTech 2014](#)

July 24–26, 2014

Portland, Oregon, USA

[Advancements in Thermal Management 2014](#)

August 6–7, 2014

Denver, Colorado, USA

[Philadelphia Expo & Tech Forum](#)

August 12, 2014

Cherry Hill, New Jersey, USA



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INNOVATIVE TECHNOLOGY: **BRYSON MATTIES**

COVER ART: **PROVIDED BY MENTOR GRAPHICS**



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July 2014, Volume 3, Number 7 • The PCB Design Magazine® is published monthly, by BR Publishing, Inc.

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**Coming Soon to
The PCB Design
Magazine:**

**August:
Materials**

**September:
Data Transfer:
The State of
Standards**

**October:
Signal Integrity**