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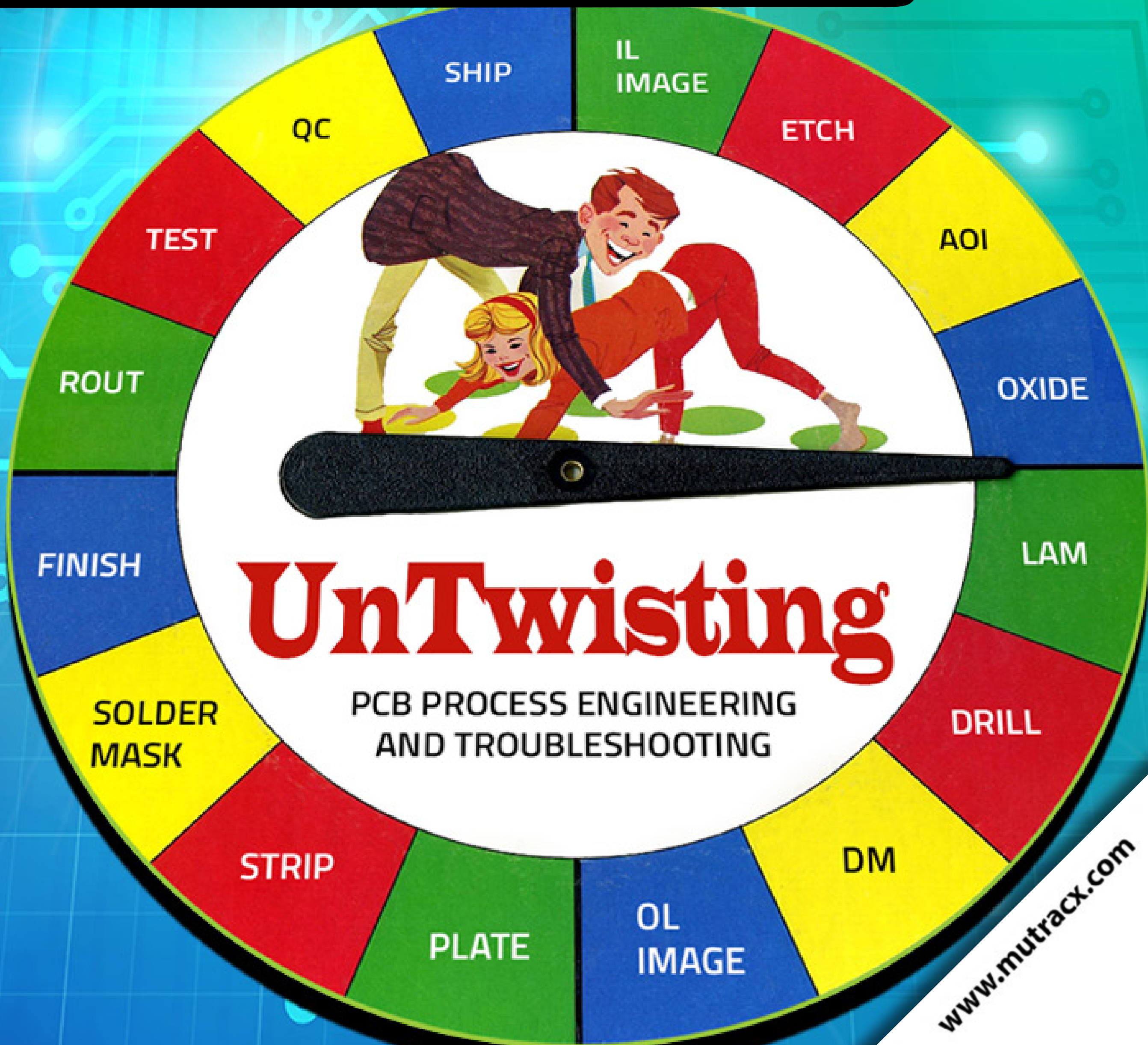
the pcb magazine

April 2016



UnTwisting

PCB PROCESS ENGINEERING AND TROUBLESHOOTING

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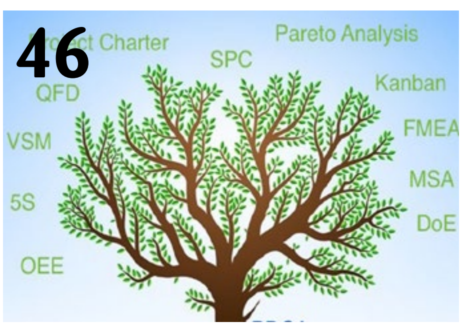

Process Engineering & Troubleshooting

Process engineers (and PE types) are the worker bees of the industry. In addition to writing standards and specifications or presenting the technical papers at industry events, they stay busy behind the scenes—running tests, gathering data, coming up with new ideas, developing new products, and so forth. Our experts this month bring first-hand knowledge of the phenomenon known as process engineering.

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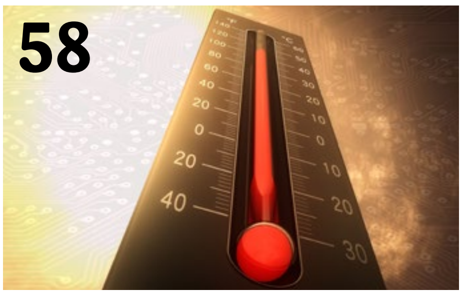

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A Salute to Process Engineers

by Patty Goldman
I-CONNECT007

It seems very appropriate, coming on the heels of IPC APEX EXPO 2016, that the focus of our April issue is process engineering. I believe process engineers (and process engineer types) are the worker bees of IPC (and obviously of the companies they work for). If they don't actually write the standards and specifications or present the technical papers, they most certainly are doing the work behind the scenes—running tests, gathering data, coming up with new ideas, developing new products, making existing products work better, and so forth.

The interesting thing about process engineering in our industry is that you don't have to be a degreed engineer. You just have to be willing to take on the problem solving and troubleshooting that is involved in making things work—in this case, the PCB shop and its product. No easy task, believe me (I've been there) but the intrigue and the never-ending variety of problems, often brought on by the increasing complexity of PCBs, is probably what lured all of us in in the first place and keeps the job interesting and challenging—and makes it tough to leave. How many people do you know who have left the industry and found themselves drawn back in?

Getting back to the recent IPC conference and show, it was and is quite an event, as those in attendance can tell you. Between myriad subcommittee meetings, keynotes, a couple dozen technical paper sessions and the exhibition, one finds too much to do and way too little time to do it—and this year we had a lot of ground to cover. We certainly got plenty of walking in at the Las Vegas Convention Center; some people reached their 10,000 steps by noon!

In the meantime, though, there were more exhibitors than ever (though the PCB corner seemed smaller than ever) and there were many very interesting technical sessions where attendance was SRO. We hope to bring you some of those presentations in future issues of *The PCB Magazine*. The conference had special meaning to me, as I was inducted into IPC's Hall of Fame at the Tuesday luncheon, a huge honor and one

I am still trying to believe really happened. I am now an IPC Ambassador!

But let's talk more about this issue. I've started us off with Joe Fjelstad of Verdant Electronics who likens PCB process engineers to a "Delta Force." He gives us a great feel for what it is that a process engineer does and needs to do. His column should inspire and encourage all those in the figurative trenches, plus he points out some newly available resources.

This is followed by RBP Chemical's Mike Carano, back in action after a hiatus, with a fine article on troubleshooting. Mike is certainly an expert on this subject; he chairs the IPC Process Effects subcommittee and they have recently issued the latest rev of the troubleshooting guide, IPC-9121 "Troubleshooting for Printed Board Fabrication Processes," the first since 1997. Definitely a must have volume for every PCB manufacturer's bookcase.

Departing slightly from his usual testing subjects, Gardien's Todd Kolmodin gives us a wonderful, step-by-step guide to building and maintaining a robust process, stressing the importance of each step along the way.

Next, our newest columnist, Renato Peres of Circuibras in Brazil goes into some detail on DMAIC methodology used in Six Sigma. He includes the kind of practical, down-to-earth advice that process engineers want and need, having been there himself.

Another technique used in continuous improvement efforts is a Kaizen event, as Dave Becker of All Flex Flexible Circuits explains in his column. Perhaps not to be used lightly or for a quick fix, but a very useful tool for your process improvement toolbox.

As you can see, a good amount of process engineering involves process improvement and process streamlining, which is the essence of Lean and, as Steve Williams of the Right Approach shows us, not that complicated; in fact most of it is good old common sense.

We have a great technical article for you this month from Eva McDermott, et. al., of Amphenol Printed Circuit Board Technology, on the long-term thermal reliability of PCB materials. Just the sort of valuable, detailed study that engineers do (and yes, she is one).

Next month we will be focusing on strategies to reduce handling errors—and we're not just talking automation. See you then! **PCB**

Patricia Goldman is a 30+ year veteran of the PCB industry, with experience in a variety of areas, including R&D of imaging technologies, wet process engineering, and sales and marketing of PWB chemistry. Active with IPC since 1981, Goldman has chaired numerous committees and served as TAEC chairman, and is also the co-author of numerous technical papers. To contact Goldman, click here.

Process Engineering: PCB Manufacturing's "Delta Force"

by Joe Fjelstad

The role of the process engineer is arguably one of the most important jobs in the printed circuit industry. The process engineer is on the front line of manufacturing and responsible for making sure product yields and profitability meet expectations. The job typically entails and intertwines many different and even disparate disciplines, including: electrochemistry, mechanical engineering, NC machining, robotics and automation, metallurgy, laser technology, polymer processing and photolithography. It even reaches back into the printed circuit design process. Because of this variety, it is also arguably at once, one of the most challenging and interesting jobs in the PCB industry.

In practice in most major manufacturing facilities, process engineers often specialize in just one of the areas identified here. In smaller facilities, the process engineer often must move between and attend to matters in more than one discipline, most commonly process steps which immediately precede or follow the area where the engineer has special training and expertise. However, in many cases, factors which may influence product quality and yield may be several steps earlier or later in the process. This is extremely important when one is looking into, or in the midst of implementing a new process on the manufacturing floor. Change comes slowly in PCB manufacturing and old habits are hard to break, so keeping a finger on the pulse of the process is critical.

It is a simple fact of life that in PCB manufacturing, process characterization, monitoring and maintenance are critical to success, and so also is collecting and evaluating data on process health. The tools and specific methods and measurements required will vary significantly from process to process, but without control, the quality of the results of the process will be left to a roll of the dice. One of the most important skills a process engineer should master

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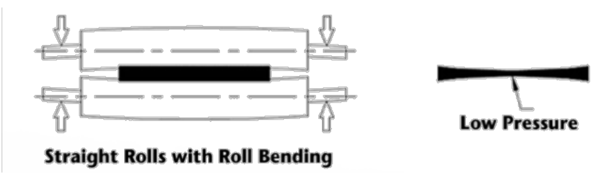

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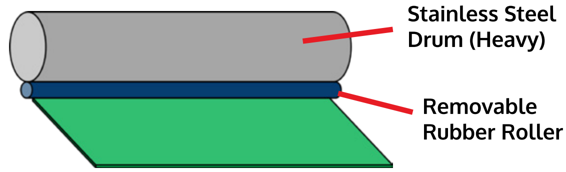

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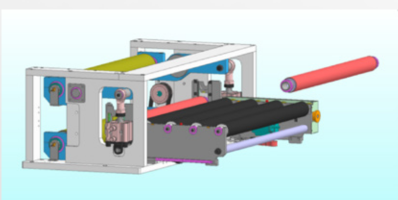

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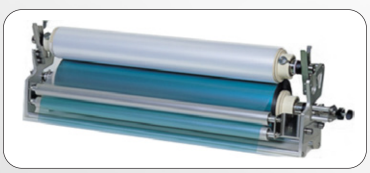

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is learning how to properly design experiments to identify the optimal operating parameters for the target process. Selecting which variables to monitor and optimize is critical. One must first do the right things and then do things right. Pick the wrong ones and the data collected will likely be meaningless. And this begs the question: How does one choose variables to monitor in an experiment?

We are fortunately living in a time when there are oceans of experience in most of the processes used in circuit manufacturing, so tapping into that experience is important. There is no benefit in repeating experiments that have been run countless times before. In this regard, it is very important that the process engineer be at least as much a reader as an experimentalist. Running experiments is useful and can be engrossing but if the answers are known by others, it is better to tap into their knowledge base.

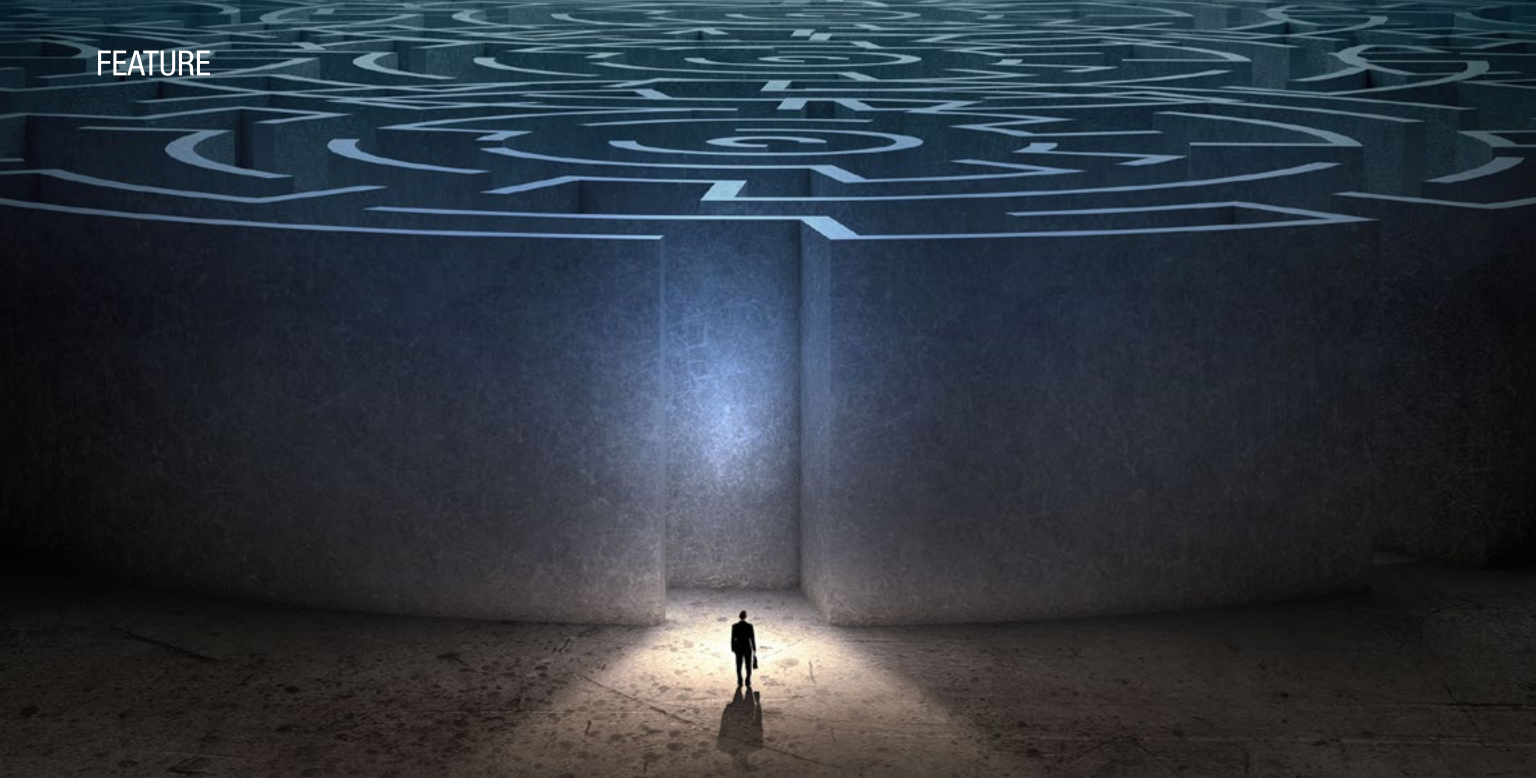
There is the old story of the successful individual who was queried as to the most important factor in their success. The two-word answer was "good experience." When pushed to explain how one gets the necessary good experience another two-word answer was given: "Bad experience." This apocryphal story was no doubt concocted by someone who understood the importance of learning from experiences and of the importance of failure. If we, in our infancy, were afraid of falling on our behinds as we departed infancy and attempted to walk, we would still be crawling about on our hands and knees. To this end there is the reminder from another sage, the early 20th century polymath and philosopher, G.K. Chesterton, who wrote: "Anything worth doing is worth doing badly." What is missing and must be inferred as an addendum to his message are the words, "…at first". There is nothing wrong with mistakes; mistakes are how we learn. However, if one has the resources available to them to avoid mistakes, then it is folly not to avail one's self of that information.

For the astute PCB process engineer, resources abound. There is a treasure trove of legacy information to be found in trade magazines, in academic journals, blogs, columns, supplier websites and industry specific texts. While on that thought, it is worth noting that *The Printed Circuits Handbook,* now in its 50th year, has just been released in a 7th Edition, edited by PCB industry icons and gurus Clyde Coombs and Happy Holden. The tome has been both a bible and a source of intelligence for preparing battle plans for process engineers since its first edition and has been translated into several different languages. It arguably should be found on the reference bookshelf of any competent PCB vendor and more importantly it should be read…

There are, of course, numerous other repositories of process knowledge available. One easily overlooked are the individuals who represent the process or equipment developers. These individuals are the honey bees of the industry who help cross pollinate those within the industry with new ideas, transferring knowledge and experience between manufacturers to the betterment of all.

In summary, process engineers serve a vital function on the front line of printed circuit manufacturing. They are often, if you will, the "Delta Force" that subdues and controls that which is one of the mortal enemies of manufacturing…process variation. The intelligent process engineers should avail themselves of all of the tools they need to complete their mission. To that end and in reference and support of that last thought, it is highly recommended that the reader of this piece read the series of columns being prepared by Happy Holden for I-Connect007, titled "25 Essential Skills for Engineers." Holden's near half-century of experience and accumulated knowledge as PCB process engineer and manager are too important to let pass by unread. **PCB**

Verdant Electronics Founder and President **Joseph (Joe) Fjelstad** is a four-decade veteran of the electronics industry and an international authority and innovator in the field of electronic interconnection and packaging technologies. Fjelstad has more than 250 U.S. and international patents issued or pending and is the author of Flexible Circuit Technology. He is a frequent contributor to I-Connect007 publications.



A Process Engineer's Guide to Effectively Troubleshooting PWB Defects

by Michael Carano
RBP CHEMICAL TECHNOLOGY

The printed wiring board fabrication process is an intricate maze of interrelated steps, both chemical and mechanical. A thorough understanding of each of the process steps is critical in minimizing or eliminating non-conforming defects—the ones that cost the fabricator money and can lead to lost customers. It is also critical to note that these profit-killing defects may have their origins elsewhere in the process.

That is the difficult thing about troubleshooting—the defect is often blamed on the process (such as electrodeposition of copper) because that is where the problem is first discovered. However, this is often false, as the origin of the defect may have had its humble beginnings in a previous process step.

To be successful at troubleshooting a problem, common sense usually applies. Basically one must first:

- Identify the problem or problems (be as specific as possible)
- Determine possible causes (looks for links to those other less obvious processes)
- Identify methods and procedures to test to see which causes apply
- Test the assumptions
- Implement corrective action

While this sounds like an oversimplification, this approach is required to properly identify and attack the problem at hand. A structured routine is really what is required.

In upcoming columns we will attempt to provide some insight as to the cause or causes of non-conforming defects and the potential solutions. We will discuss process parameters and the importance of control of the processes.

Let's discuss the step-by-step methodology for troubleshooting.

Identify the Problem or Problems

First and foremost, you must have a clear sense of what you are looking at. In troubleshooting, I firmly believe in the team approach to solving the problem. However, the team must agree on what the defect is: is it hole wall pull-away (HWPA) or resin recession; is this an interconnect defect (ICD) or simply a line of demarcation? These are just a few examples. But the wrong call will lead you down the incorrect

path as you attempt to tech out of the problem.

In Figure 1, examine the cross-section closely. Carefully determine if what one is seeing is a shrinking or recessing of the resin, or is the plated copper blistering or pulling away? Some would jump to the conclusion that the defect is HWPA. This would then trigger an exercise to brainstorm on a number of processes including desmear and electroless copper (including a deeper dive into drilling, electroless copper catalyzation and copper plating rates). However embarking on this path would be disastrous. Clearly the issue shown in not HWPA. The resin has recessed, leading to the proper conclusion that this is resin recession.

According to IPC-600 H, section 3.1.9, resin recession is acceptable for all classes of PCB boards after thermal stress.

Now, in the case of the defect shown in Figure 2, the plated copper clearly has lost adhesion to the hole wall.

When a condition such as HWPA is discovered, there are several potential causes of the defect:

1. Overactive electroless copper process: Essentially, the deposit is being laid down much too fast, leading to a stressed condition. The inherent stress in the deposit causes the copper to pull away from the substrate. Check the deposition rate on the electroless copper rate panels-was an increase noted possibly due to over temperature condition in the electroless copper solution? Is the chemistry out of balance? Check the formaldehyde, caustic and copper concentration. Is the process being controlled within the operating window of these additives? A higher than normal caustic concentration will lead to a higher deposition rate. Examine the grain structure of the electroless copper deposit. Compare to previous results when HWPA did not exist.

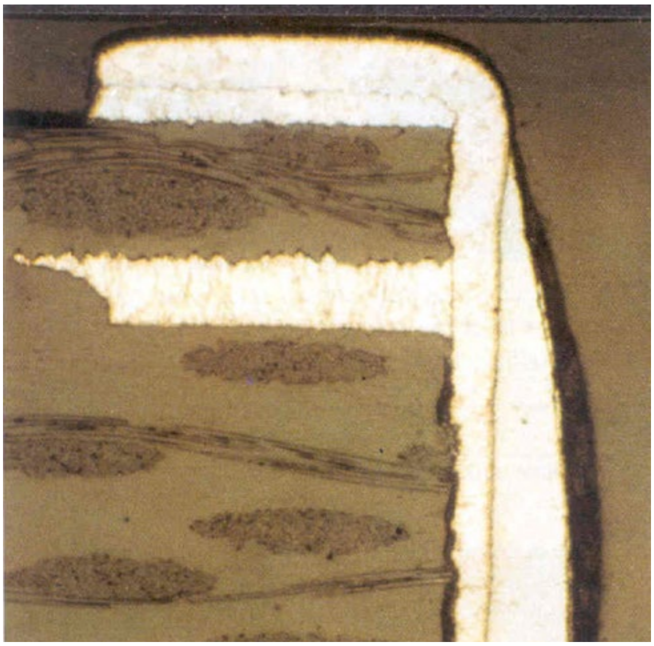


Figure 1: Defect clearly shows resin recession, not HWPA.

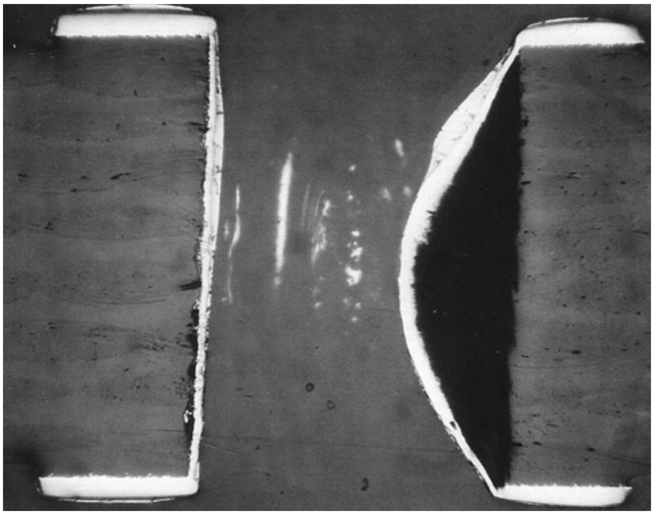


Figure 2: Severe case of HWPA.

2. Desmear operation leaving a less than desirable surface topography on the resin: Typically, this is an issue related to the permanganate process. Higher Tg resins are more resistant to desmear chemistry and thus the surface topography and extent of resin removal are less than optimum. Weight loss measurements utilizing a small coupon made of the same resin system and processed through the desmear process under the current conditions will yield some evidence. An SEM taken of the PTH will give a good picture of the topography on the resin after desmearing. Do not rely on weight loss data alone. A sufficiently micro-roughened resin surface provides a surface area to promote catalyst adsorption as

well as to provide anchoring sites for subsequent copper metalization. It is conceivable that the solvent swell (the first process step in the alkaline permanganate process) is not sufficiently weakening the polymer-polymer bonds in the resin. This will result in reduced resin removal and insufficient topography. First and foremost, the defect or issue must be properly identified in order to design a plan of attack. And again, I cannot stress enough the importance of up and downstream processing.

> First and foremost, the defect or issue must be properly identified in order to design a plan of attack.

Looking into methods to troubleshoot deeper, determine whether or not proper operating procedures were followed. Did the process change in some way from the standard? Compare the defective product to a non-defective one. Was the process operating within the specified parameters? Don't take anyone's word for it. Check this out thoroughly! On way too many occasions, significant loss has been incurred because the process or processes were run out of spec. ***Famous last words: We checked everything an hour ago and all is good!***

Simple analysis or control procedures would have prevented such an occurrence. If the analysis shows that the chemistry, dwell times, operating temperatures, etc., are not in control, then bring the operation to a halt until the corrections are made. Then run some tests to see of these corrections solve the problem. If this does not correct the problem, then the team must sit down to determine other possible causes for the defect.

Possible Causes

The rule of thumb here is to keep the troubleshooting project as manageable as possible. Begin to brainstorm on the linkages in the up and downstream processes and potential effects of process variation in these process steps. Gather all pertinent information including statistical process control (SPC) charts, temperature logs, analysis records (including record of calibration and analytical standards) and the like. Then develop a cause-and-effect diagram. Fish-bone diagrams serve this purpose well. At the risk of having hundreds of factors to investigate, only the most likely causes should be investigated first. This will serve to weed out those processes that are not contributing to the defect. A process audit is a must in this situation. Hopefully, you have a reliable supplier or suppliers who work with your company in close partnership. Ongoing process audits jointly and separately performed by your supplier and designated individuals in the fabricator's facility should be standard operating procedure. Process audits alert the manufacturer if a process is "drifting" out of the control window.

Once the team has set up its test plan based on a narrowing of potential causes, the divide and conquer approach will aid in the efforts. For example, if one suspects that thin plating of copper in the hole is caused by problems associated with the electrodeposition process, simply processing the PWB in the acid copper plating solution for the required time and current density should yield whether or not the copper plating process or the equipment (e.g., copper plating anodes, rectifier, electrical connections, etc.) are the cause. If not, then one must examine the previous steps. Are there discontinuities in electroless copper deposit or direct metalization process causing thin plating? Are there voids one cannot see? These are just some of the questions to be asked.

Only a systematic approach will help solve problems expeditiously. Above all, after selecting the processes and test procedures to be implemented, test these assumptions with vigor. Time is money.

Hopefully, these actions will identify the suspect cause(s) of the defect. When the problem is located, corrective action must be implemented. Determine what measures will be taken to ensure that the problem does not reoccur. Redefine the process control window. Set up

permanent controls in order to keep the process within a tighter operating window if necessary. For example:

- Set up process audits at specified times
- Implement process control procedures and measurements
- Preventative maintenance on equipment
- Training of operators
- Maintain or establish close ties with your suppliers

Certainly, this is only a guideline for troubleshooting. The key is to get to the root cause of the problem as soon as possible without taking shortcuts for the sake of time.

There is no substitute for a systematic approach backed by solid knowledge and understanding of the process parameters and the influences of up and downstream processes. Remember, the process in which the defect manifests itself is not always the main cause. Look carefully.

Equipment Issues

It is always quite easy when there is a significant issue to default to the chemical processes. What a mistake! A real life example is shown in Figure 3. The fabricator complained about incomplete etching of the copper, so it must be the fault of the chemistry. Upon examination by the tech team, there was a noticeable residue on the boards in some areas. This residue was inhibiting etching. However, the residue was deposited onto the circuit boards by the equipment rollers.

Figure 3: Transport wheels decomposing. (Source: IPC)

Note that the rollers were actually decomposing. However, this issue was not the fault of the etching solution. The issue relates to a purchase of roller materials that were not compatible with the chemistry. When in doubt read the equipment maintenance guide.

Here is another example of the failure to look at all aspects of the process (and that includes people, materials and machines).

In Figure 4, the fabricator noted copper spots remaining on the innerlayers after develop-etch and strip. So the conventional wisdom is to look at the etching equipment and process chemistry. However, upon further review, it was determined that only one part number showed copper spots. Other designs did not. As the photo in Figure 4 shows, there was exposed dry film resist that was protecting the underlying copper—as it should. However there was to be no exposed resist in this area. Upon examination of the particle phototool used for this part number, there were some very fine clear areas in what is the opaque portion of the tool. Thus, these pinholes allowed UV light to polymerize the resist in these areas. This in turn inhibited the etching, leaving copper spots. Clearly this was not a wet chemistry issue.

The above illustrates the importance of critical thinking (and knowledge) when troubleshooting PCB defects.

And if Things Couldn't be any Worse!

One of the most devastating issues to confront occurs when, despite the best efforts of the fabricator, the EMS company gives you a

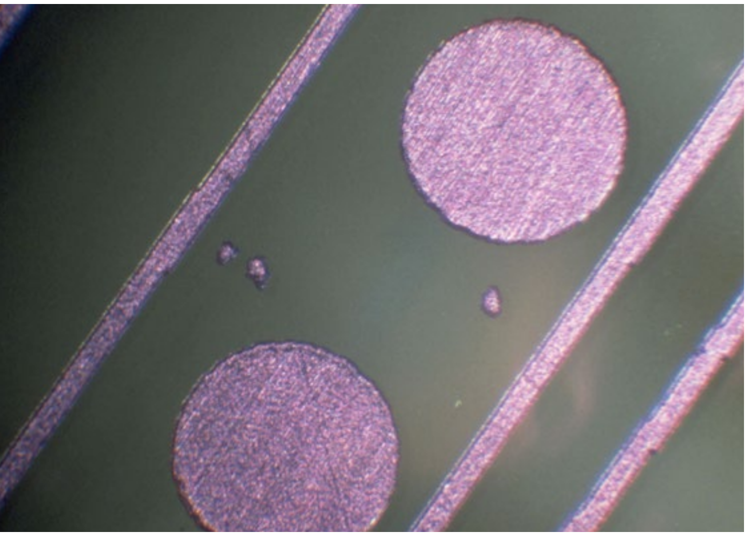


Figure 4: Exposed resist due to pinholes in the phototool. (Source: IPC photo archive)

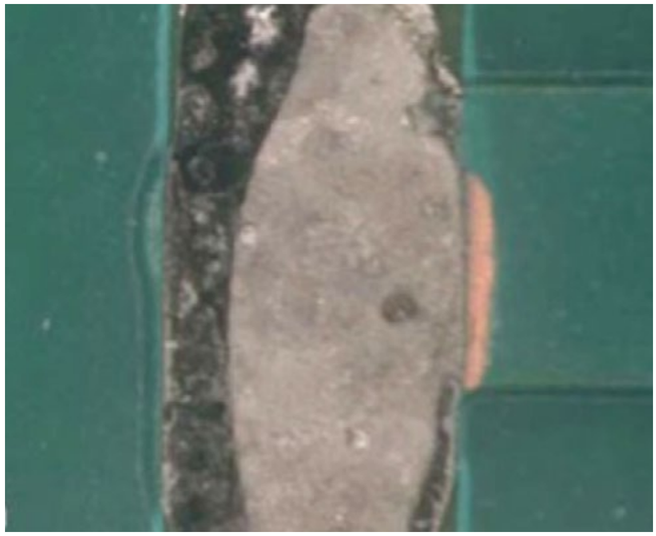


Figure 5: Issues with assembled PWB: dewetting and black residues.

call and complains of solderability defects (Figure 5). Now the team needs to spring into action. At first glance, the fabrication team should not simply assume that the defect that manifested itself through the assembly process was the fault of the bare board. Regardless, the assembly firm most likely will not see it that way. The assembly team argued that there were issues with solder joints not forming properly—dewetting. In addition there were black areas visible across a number of surface mount pads. The final finish in question was ENIG. Now there is concern about hyper-corrosion of the underlying nickel surface.

It would be easy at this point to just call this black pad and allow the PWB fabricator to accept blame. But a truly experienced and effective troubleshooter would ask for more data and conduct additional tests on her own. One issue I sometimes encounter in cases like this is: The EMS company engineer refers the dewetting issue to IPC-610. And yes, the IPC-610 provides guidance on acceptability of wetting, etc. However IPC-610 does not provide adequate vetting in order to screen for solderability concerns or even black pad.

So, what needs to be done here is to take some of the defective boards and cross-section those areas. Refer to IPC-4552 and determine if there is corrosion of the underlying nickel. Keep in mind that minor corrosion spikes in the nickel are not cause for concern (IPC-4552).

At the very minimum, the bare board fabricator must perform a thorough audit of its ENIG process including SEM analysis, gold thickness measurements and solderability testing. However, the assembly company must also provide reflow profiles, information on solder pastes used, as well as testing of the solderability of the components! Leave no stone unturned.

Summary: Guidelines for Effective Troubleshooting and Process Control

One of the keys to effective problem solving is a structured routine that addresses key points each time a major problem is encountered. This section suggests steps to effectively find the cause of a problem and to solve it permanently. Refer to IPC-9191 for greater detail to suggested methodology for SPC.

1. Before beginning a detailed troubleshooting project, use common sense in defining the problem.

- Verify that there is a problem
- Observe the defective product and compare it to the standard
- Identify the standard process and product, and then determine any present deviation from the standard or any change in the product

2. Establish whether operating procedures were followed and whether an assignable cause can be quickly identified as the reason behind the problem.

- Only continue into more detailed analysis if the initial questions do not lead to an obvious answer
- Even if the answer appears to be obvious, confirm the answer by operation of the process before closing the project

3. Develop a clear, concise problem statement that quantifies the problem whenever possible and reduces the scope of the investigation to a manageable size.

4. Gather all pertinent data and facts.

- Use SPC, historical data, records, logs, etc.
- This includes temperature charts, analysis records, maintenance logs, etc.

5. Perform a causal analysis.

- Producing out-of-specification parts requires immediate action (i.e., shut down the process)
- Out-of-control processes require determination as to whether the process can continue to operate
- Severe process variation requires evaluation of the severity and effect of the problem on the final product

6. Develop an action plan that includes the procedures for addressing products produced during out-of-specification or out-of-control conditions. The plan should also indicate who should make those decisions. These issues include but are not limited to:

- Disposition of the defective material (repair, scrap, replace, etc.)
- Checking the effect on scheduled delivery
- Informing the effect on scheduled delivery
- Request for non-conformance authority or material review board (MRB) action
- Establish a corrective action plan to reduce or eliminate the likelihood of recurrence

7. Conduct a measurement system evaluation, which is a means used to detect and identify the problem. This includes not only the measuring apparatus, but also:

- The sampling method
- The operator (and his/her instructions)
- Accuracy and calibration of equipment
- Environmental factors (i.e., lighting, temperature, and relative humidity)

8. The variation inherent in the measurement of attribute data and responses that are subjective in nature can be addressed. The evaluation is more complex in nature, but it is still an essential part of the analysis of the problem. IPC-9191 (General Guidelines for Implementation of SPC) discusses this subject in greater detail.

For further reading and learning on this subject, please review the IPC-9121, a new standard for understanding and preventing printed circuit board defects. This handbook provides problems, causes and possible corrective actions related to PWB manufacturing processes. To keep this document current, readers are encouraged to submit process problems with photos as well as proposed causes and solutions to the IPC 7-24 Printed Board Process Effects Handbook Subcommittee for consideration in future revisions of this document[1]:

Finally, one should never assume that making one small change in a process (new material, photoresist, specialty cleaner, etc.) does not require validation. As an example, a fabricator made a switch to another acid cleaner on its pattern plating line. The thought process was that the new cleaner (similar to the present process) would provide additional residue solubilizing properties. The result of this change was that the new cleaner attacked the sidewalls of the exposed resist, creating plating defects including copper adhesion failures and pitting. In this case the fabricator neglected the cardinal rule for considering a process change: Performing the initial capability study. These capability studies are ideally done before the process is accepted for production. This means creating a match between

the process and the product, and it results in a process control window that is capable of producing the product.

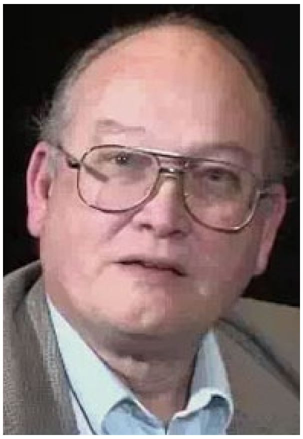
One approach to troubleshooting that quantifies improvement for reporting to management involves a capability assessment. IPC-9191 discusses in greater detail the generation of capability indices. This step promotes a clear understanding of the process matrices, but it requires time and resources. **PCB**

References

1. Click here to access an IPC Standards Improvement Form.

Michael Carano is VP of technology and business development for RBP Chemical Technology. To reach Carano, or read past columns, click here.

Solberg and Holden: Two Valuable Series Available now at I-Connect007

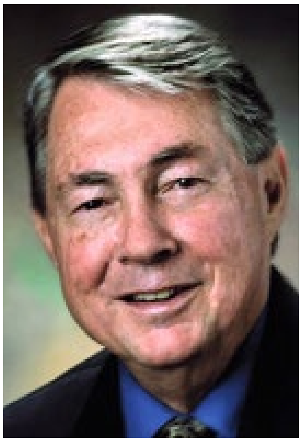


Happy Holden

In early 2016, long-time author, PCB expert, and industry veteran Happy Holden started writing a 25-chapter book, "25 Essential Skills for Engineers." He initiated it with an introductory article in the January issue of The PCB Magazine. Since that time, we have been publishing chapters approximately every three weeks in our I-Connect007 Daily Newsletter, as well as some of our weekly newsletters.

Now Happy as upped the ante. He has been writing steadily and has asked to publish every two weeks, so we said, why not? Watch for his chapters to appear every other Wednesday in the PCB section of the I-Connect007 Daily Newsletter. Chapter 4 is currently scheduled to appear on April 6. It's free to subscribe, so don't miss out on this highly informative and downright useful book. To catch up on the chapters we've already run, check out Happy's columnist page for a complete list of titles and links.

We are fortunate to have a second highly-valuable series, penned by veteran SMT and microelectronics designer, author, and expert Vern Solberg. His six-part series, "Flex and Rigid-Flex Circuit Design Principles" publishes in both the InsideDesign and Flex007 weekly newsletters, as well as the daily newsletter a day or so later.



Vern Solberg

Vern's introduction nicely summarizes the crux of his series: "Flexible circuits represent an advanced approach to total electronics packaging…maintain uniform electrical characteristics, controlling noise, crosstalk, and impedance…saving up to 75% on space and weight…improve overall product reliability…[and] furnish unlimited freedom of packaging geometry while retaining the precision density and repeatability of printed circuits."

In part 1, Vern describes the primary flex structures, design for operating environment and base material selection. In part 2, he discusses supplier assessment, planning the flex-circuit outline and circuit routing principles, while part 3 goes into detail on specifying base materials, copper foil variations and fabrication documentation. Part 4, just published the week of March 30, focuses on rigid-flex construction, conductor routing and mechanical clearances. Part 5 is expected to publish April 27—28. Don't miss it!

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A Johnson Electric Company

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Ending: April 28, 2016 / 11am PDT
Location: San Jose, CA
Preview: April 25, 2016 / 9am - 4pm PDT

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- Barnaby screening table
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- (2) Accuprint 5KW light source
- DuPont SMVL dry film vacuum laminator
- Grieve 3X3X3 oven
- Nuarc stencil making machine
- VWR 2X2X2 dispatch oven

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- PHI 3 opening electric press 24X30 platens
- PHI 4 opening cold press 24X30 platens
- PHI 3 opening electric press 20X18 platens
- All separator plates used in Multilayer presses

DRILLING AND FABRICATION
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- Excellon Century 2001 SP 4 spindle 180,000 Rpm Spindles
- Excellon Mark V with CNC 6 controller with 110,000 RPM spindles
- Excellon EX-200 CNC-6 2 spindles drill router 80,000 RPM spindles
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- All used and new drill bits

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- Chemcut 547 XLI Etcher with main etcher, flood rinse counter flow water rinse and dryer
- Chemcut 547 Stripper strip chamber counter flow water rinse dryer
- Electroless Copper line
- 4X5X4 Copper plating tank with rectifier
- 4X5X4 Solder plating tank with rectifier
- Chemcut 547 developer with developer chamber counter flow water rinse dryer with S wheel
- Reverse osmosis waste treatment systems
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- Grieve 3X3X3 oven
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MilAero007 Highlights

FTG Circuits Qualified to MIL-PRF-31032

The FTG Circuits, Chatsworth, California facility has been qualified to the Department of Defense performance specification MIL-PRF-31032/3 (flexible printed wiring boards) and MIL-PRF-31032/4 (flex-rigid printed wiring boards).

API Technologies to be Acquired by PE Firm

API Technologies Corp., a leading provider of high-performance RF, microwave, millimeterwave, power, and security solutions, announced a definitive agreement providing for the company to be acquired by an affiliate of private equity firm J. F. Lehman & Company (JFLCO), which specializes in the aerospace, maritime and defense industries.

PCi Purchases Polar CITS880s Controlled Impedance Tester

Rigid flex circuit board manufacturer, Printed Circuits Inc., purchased a CITS880 controlled impedance tester from Polar Instruments. Polar Instruments' software and testing equipment is the most popular solution in the PWB manufacturing industry for predicting and verifying controlled impedance circuits in circuit boards.

BAE Systems, Shengyi Receive IPC Corporate Recognition Awards

IPC – Association Connecting Electronics Industries bestowed its highest corporate honors to two member companies, BAE Systems and Shengyi Technology Co. Ltd. During a luncheon at IPC APEX EXPO, the IPC Stan Plzak Corporate Recognition Award was presented to BAE Systems and the IPC Peter Sarmanian Corporate Recognition Award to Shengyi Technology Co. Ltd.

PrecisionHawk Explores Extreme-Weather Testing of Drones at ACE

PrecisionHawk has successfully completed the world's first extreme-weather testing of unmanned aerial vehicles (UAVs) in the ACE climatic wind tunnel at the University of Ontario Institute of Technology (UOIT).

Robots: Eliminating the First Contact with an Enemy Force

"We should be thinking about having a robotic vanguard, particularly for maneuver formations," said Dr. Bob Sadowski. "There's no reason why the first contact with an enemy force should be with a man-platform, because it means that platform is at the greatest risk."

PNC Purchases Universal Pick and Place Equipment

Sam Sangani, president and owner of PNC, has announced that his company recently added a new Universal pick and place machine, model Genesis GI-07, to its fast-growing assembly department.

Configurable Analog Chip Computes with 1,000x Less Power than Digital

Researchers have built and demonstrated a novel configurable computing device that uses 1000x less electrical power—and can be built up to 100 times smaller—than comparable digital floating-gate configurable devices currently in use.

IPC APEX EXPO 2016: Glenn Oliver on His IPC "Best Paper" on High-Frequency Materials

Glenn Oliver of DuPont discusses his award-winning paper, "Round Robin of High-Frequency Test Methods by IPC-D24C Task Group." Co-authors include Jonathan Weldon of DuPont, John Andresakis of Park Electrochemical, Chudy Nwachukwu of Isola, John Coonrod of Rogers Corporation, David L. Wynants of Taconic Advanced Dielectric Division, and Don DeGroot of Connected Community Networks.

Harris Signs Definitive Agreement to Sell Aerostructures Business

Harris Corporation and Albany International Corp. today announced a definitive agreement under which Albany International will acquire Harris' aerostructures business for an enterprise value of $210 million, including $187 million in cash at closing and the assumption of a $23 million capitalized lease.

Process Management: Doing It Right

by Todd Kolmodin
GARDIEN SERVICES USA

The term "process management" is widely used in today's economic theatre, but what is it really? Simply put, it is the idea of figuring out how to do something, documenting it and then monitoring the effectiveness of the steps you created for the end result. Simple, right?

Unfortunately, many who take on this endeavor fall short due to missing some key attributes to creating and maintaining a robust process. It doesn't matter whether we are building a box or building a battleship, the theories are the same. Many consider writing work instruction the process but it is only one of the key attributes. Remembering this will no doubt keep you from the pitfalls of process failure. We all remember what the customer wanted, right?

A process that is unclear when created will undoubtedly result in something like the picture in Figure 1. So let's build a process correct-

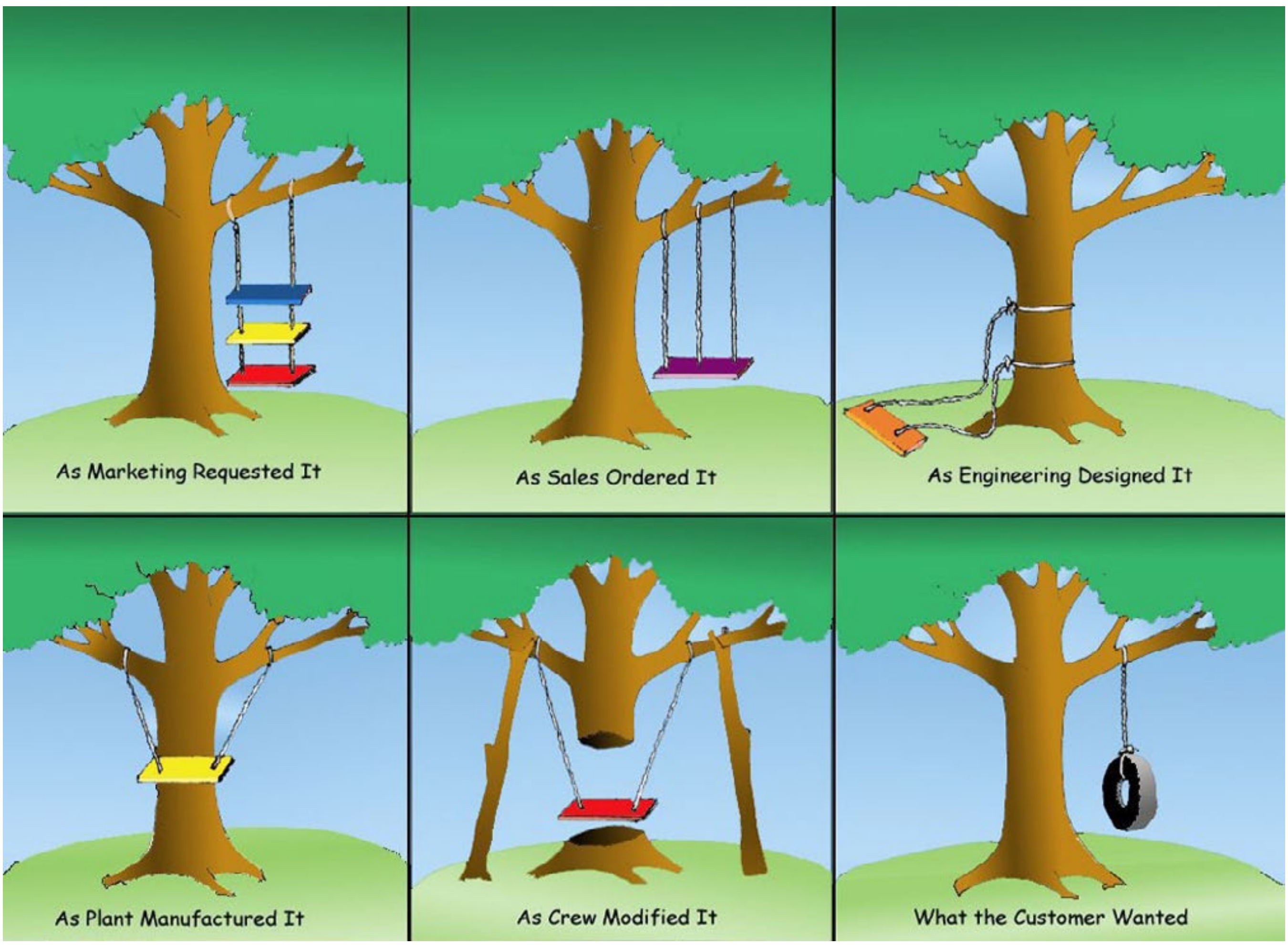


Figure 1: How not to communicate.

ly. There are eight steps in building and maintaining a robust process:

1. Identify the process. What are we trying to do? This may sound a bit general, but it is critical. Write it down.

2. Determine the resources needed for the process. If we are building a box we will need materials such as wood, nails, screws, a hammer, etc. Determine what tools will be needed to create what we defined in Step 1.

3. Decide who is doing it. This is a critical step that many overlook. Who is going to be doing this process? In many cases, the mistake is that the process is written so overly technical that only a Ph.D. or rocket scientist could possibly understand. This leads to breakdown and ultimately, process failure. Now if the process requires a Ph.D. or rocket scientist to perform the steps then by all means write it and include the attributes required for that audience.

4. Create a flowchart/diagram. Now it's time to document your actual steps. This may include more than one document if more than one department or entity is involved. This is your work instruction phase. This is best documented while the actual steps are being performed. It is much more difficult to look at the finished product in a conference room and reverse-engineer by memory. Do it hands-on. It will save edits and missed steps in your process. This is a time to again consider your audience. While in this phase, reflect on what is critically needed for the process and what may be left out if some common knowledge is already indicated.

5. Expand. Now that you have your steps, review each one and expand if necessary to include specifics about a given step. Perhaps a special tool is required in one step or a certain color of paint. This is the time to provide examples. What should the product or activity look like at a certain step? Visual examples work very well to gauge whether the process is developing the desired result. Be careful during this step as to not write yourself into a corner. Consider the future and other integrated processes

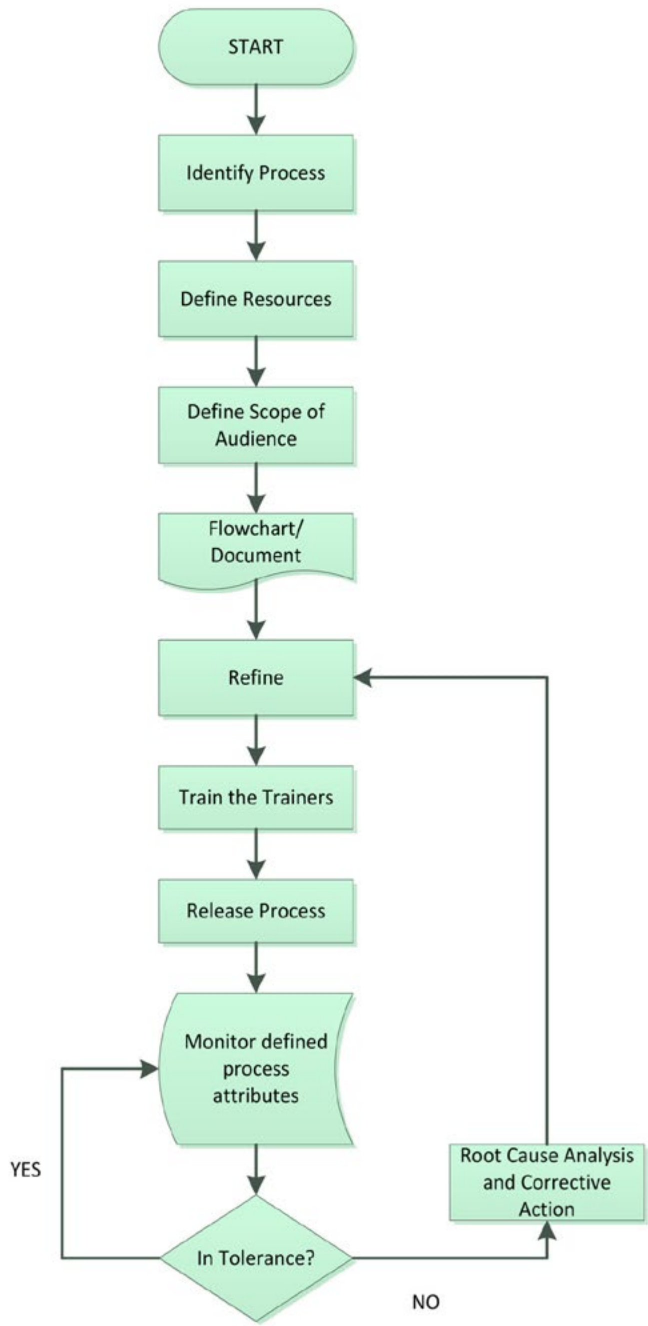


Figure 2: Process-building steps flowchart.

that may work with yours. If your process is too tight, you may have issues with amendments or changes in the future, or have issues modifying your process to accommodate a sister process related to your own.

6. Test the process document. If you wrote it, I don't mean you. Find a volunteer to read

through the document and perform the steps within. Here you will find where something may have been accidentally omitted. Make your correction(s) and do it again using a different volunteer. When you are satisfied with the results it's time to move to the next step.

7. Train the trainers. I can't emphasize this enough. Here is one of the biggest failure mechanisms in process management. You just created a great document and released it to production and you can't figure out why it's not working! Whether your organization is large, with training staff, managers and operators or just a small shop, the focus must be the same. You must train who will be performing the process. Whether it is a workshop-type training session or a one-on-one meeting, you must go through the steps, listen to questions and document who, what, where and why. This is part of your process management: accountability. If there are many sub-processes involved in your final desired outcome (box or battleship) this must be done for each individual sub-process. Don't skip or cheat this step or you will have undesirable results and difficulty finding the root cause of any failure.

8. Monitor. Of all the steps, this final step is the most important. How do you know if the process you created six months ago is still as strong today as it was the day you created it? You need to have your finger on the pulse of that process. How do you do that? Define inspection steps or key objectives to be monitored during the process. Define limits to those attributes and instructions when a control is violated. Doing this can provide immediate attention to the faulting occurrence whether it be equipment, human or unknown at the time. Utilizing '5 Why' root cause analysis can ultimately isolate the out-of-control root cause and you can then correct it but that's for another day.

To conclude, when building and maintaining a process, don't be overwhelmed by the overall scope of the final required result. While some processes may be very large with many integral steps we can break each of these down using the eight steps. These building blocks can then be unified to capture the entire desired result while also monitoring each phase for any out of control conditions that may affect the final result. Use the process building step flowchart to guide you to successful process building. **PCB**

Todd Kolmodin is the vice president of quality for Gardien Services USA, and an expert in electrical test and reliability issues. To read past columns, or to contact Kolmodin, click here.

Focusing on What Matters Most!

by Renato Peres
CIRCUIBRAS

Every company claims to be constantly improving their business or process, but not as many grasp the core idea of continuous improvement and live it daily. This is evident when one analyzes companies competing on the same market, providing quite the same products, yet having totally different results. Improvement is often misunderstood as doing things differently, which is a huge mistake.

Taiichi Ohno was known as the father of the Toyota Production System, helping Toyota to become the best automaker in the world. In the '80s, another engineer and scientist working at Motorola, Bill Smith, had just started a revolutionary culture change at his company. At that time, Motorola was struggling to compete against its rivals, which delivered better products with lower prices. A simple tool wouldn't help them to succeed. They needed a change in their business strategy.

Bob Galvin, who had just stepped down as CEO of the company in 1986, was so amazed by Smith's belief in Six Sigma that he made it a strong component of Motorola's culture.

Since then, Six Sigma has gone through several changes including the substitution of its primary method MAIC (measure, analyze, improve, control) for DMAIC (define, measure, analyze, improve, control). Most recently, it has added the Lean manufacturing practice and philosophy, giving birth to the Lean Six Sigma strategy.

In both cases, the success of the change in business strategy and culture was due to a top-down initiative, and this is a point we should not overlook. I have no doubts that if you just use the tools or methods that are part of Six Sigma or Lean manufacturing, you will get satisfactory outcomes. However, spectacular results will be determined by the deep commitment of the top management.

With this is mind, I will present a quick overview on DMAIC methodology, which is

1798: Eli Whitney, Mass Production and Interchangeable Parts

- Need for consistency.
- Identification of defects.

1924: Walter Shewhart

- Process oriented thinking.
- Control charts (assignable and common cause).

1945: The Japanese Quality Movement Begins

- Statistical methods and use of statisticians.
- Continuous improvement (plan-do-study-act) methodology.
- Active engagement of management and involvement of everyone.
- Diagnostic and remedial journeys.

1973: The Japanese Make Their Move

- Quick responce to changing customer needs.

1980: Philip Crosby and *Quality Is Free*

- Methodology to achieve companywide quality improvement.
- Improve product, process and service. Strive for perfection.

1987: International Organization for Standardization

- Widespread sharing of basic elements of sound quality systems.
- Organizational rally cry for improvement.

1987: Malcolm Baldrige National Quality Award

- Sharing best practices.
- Strong focus on customers and results.

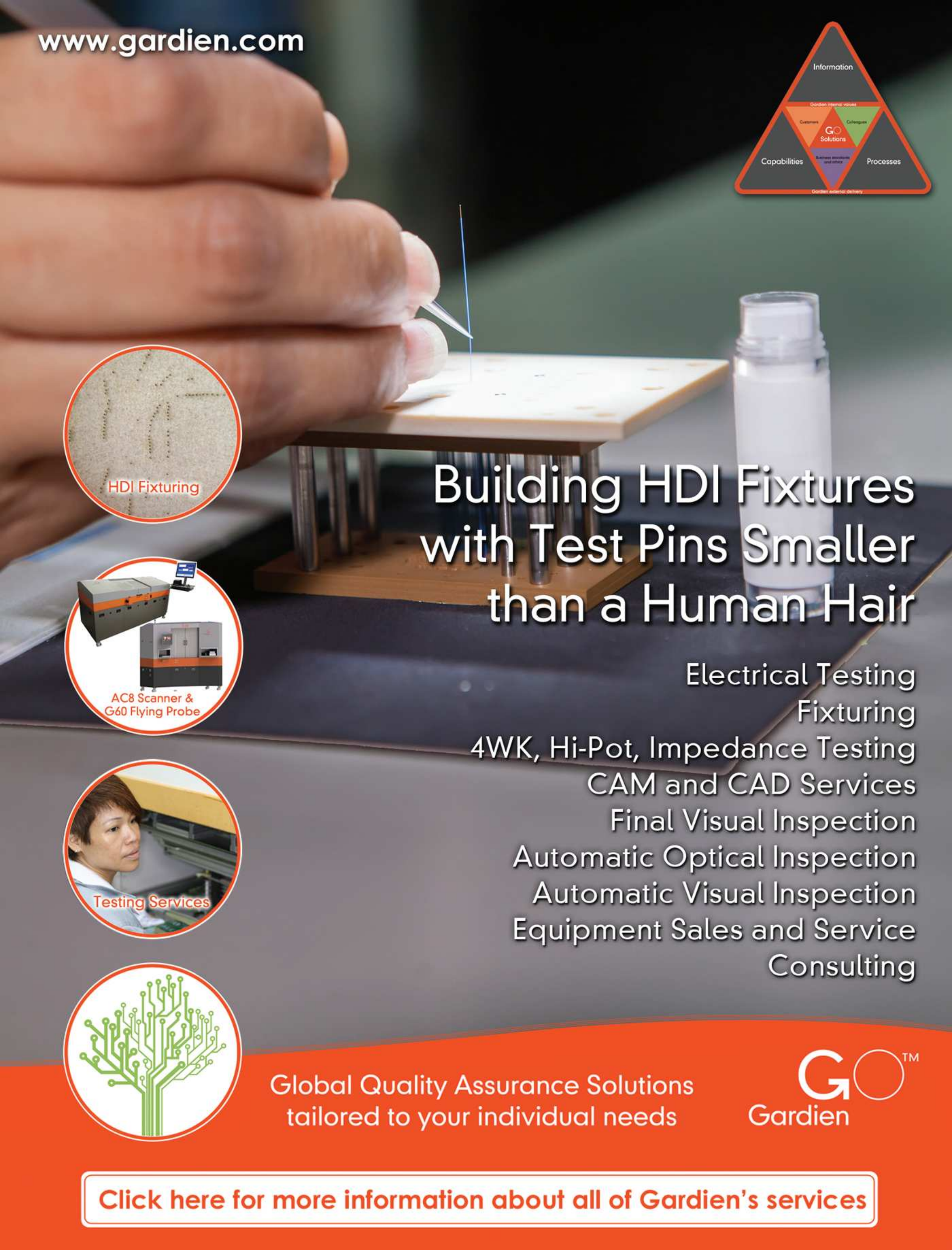
1987: Motorola and Six Sigma

- Focus on customer needs and comparison of process performance to those needs.
- Structured methodology with discipline and proven business results.

1960-1995: Other Initiatives

- Tools to be used by everyone in the organization.

Figure 1: Six Sigma history[1].



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one of the pillars of Six Sigma, and may help you answer questions like:

- How do you know you have improved your process?
- Have you seen better results since last week, month, or year?
- Do you still maintain the results you have achieved?
- Did you or your team help your company to achieve its goals?
- How much money has your company saved?

DMAIC methodology gathers several tools we all have heard about, such as: Pareto analysis, value stream mapping, failure mode and effect analysis, statistical process control, and

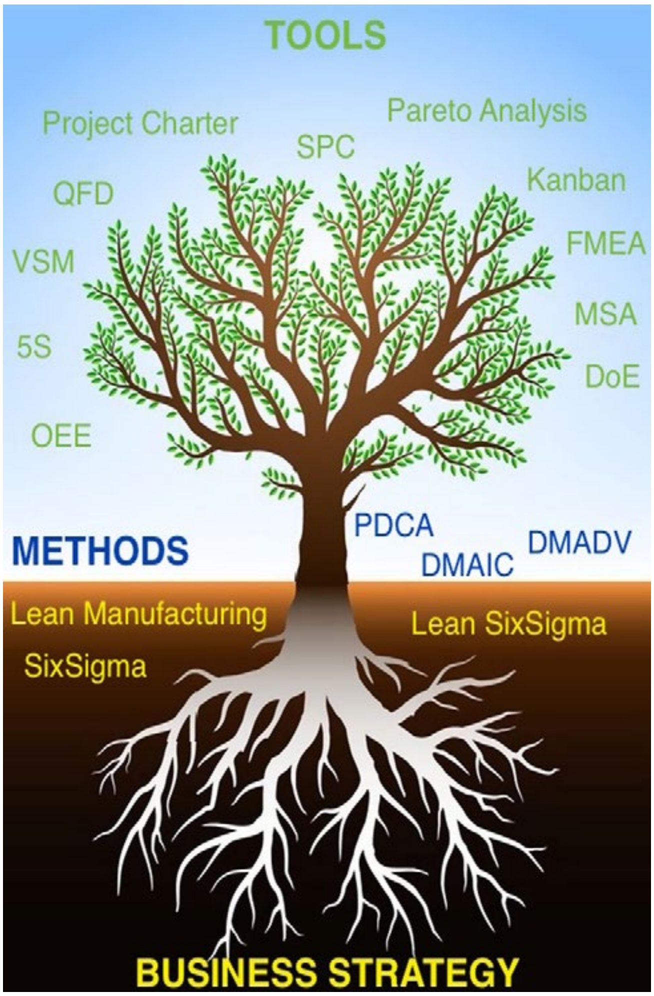

Figure 2: Tools, methods and business strategy.

project charter, to cite some. But it goes further, creating a meticulous path to execute the activities presented on the method, which results in correct conclusions of what must be done.

Define

Everything starts here, and it is said that if you start well, you may finish well.

At this point, it is very important to clearly DEFINE what are the goals and scope of the project.

Remember, the methodology is not only about process improvement, but improving your company's outcome. So it is necessary to make it clear that the goal you set here must be in accordance with your company's goals.

Sometimes, engineers (myself included) want to make excellent that which may not be financially good for the company. If you allow me to offer a piece of advice, keep the focus on the golden pot: customer and money. And always discuss your project with top management.

According to Vicente Falconi Campos, a well-known Brazilian business consultant and writer, a target consists of a management goal, a value, and a deadline. Keep it in mind.

Here are some tools that may guide you through the definition of your goals:

Project charter; financial analysis; voice of the customer (VOC); and value stream mapping (VSM).

Measure

Data is as essential to Six Sigma as the air we breathe. If you want to know what you have improved since last semester, you need to know where you were last semester. Thus, work hard to establish the baseline and the targets for each problem. If you don't have any data, or just have poor data, you will need to plan how to collect new data.

Statistical tools and techniques are widely used on this step: histograms, control charts, boxplots, and Pareto analysis, along with VSM and measurement system analysis (MSA).

Analyze

"Give me six hours to chop down a tree and I will spend the first four sharpening the axe." — Abraham Lincoln

Determining the root cause of the problems identified in the first step is the goal here. This is the last step before you go into action.

Not thoroughly analyzing the root cause will compromise the whole process, because it will drive you to wrong actions. My suggestion: Don't waste your company's and your teams' precious time and money; do your best to get to the root cause.

Some of the tools you may use to achieve your goal include: Eight Disciplines Problem Solving (8D Analysis), 5 Whys, Fishbone Diagram, Brainstorming, Failure Mode and Effect Analysis (FMEA), and Cycle Time Analysis.

Improve

The goal is to come up with ideas to eliminate the fundamental causes of the problems defined (propose), analyze the risk of each action (evaluate) and test the chosen solutions (implement). After testing, it is necessary to check the results and go back to the measure step if necessary.

Control

It seems obvious, but leaders may fail on this step. Have you ever had the feeling that you had already faced a specific problem? If so, it is because the method hasn't come to an end yet. In order to preserve the results, new patterns must be defined and shared through all the organization. A training section must be done, as well as the updates of all your manuals and work instructions. If possible, use automatic devices or methods to prevent failure to occur (Poka-Yoke).

Conclusion

It is not uncommon to see people focused on doing things that are urgent, and sometimes not important and solving immediate problems instead of thinking of the long term. Here in Brazil we have an idiomatic expression for that: "apagar incêndio," which literally means working to extinguish a fire instead of preventing it from happening.

DMAIC works to extinguish the fire and prevent it from happening again.

For more information on Six Sigma visit the website isixsigma.com. **PCB**

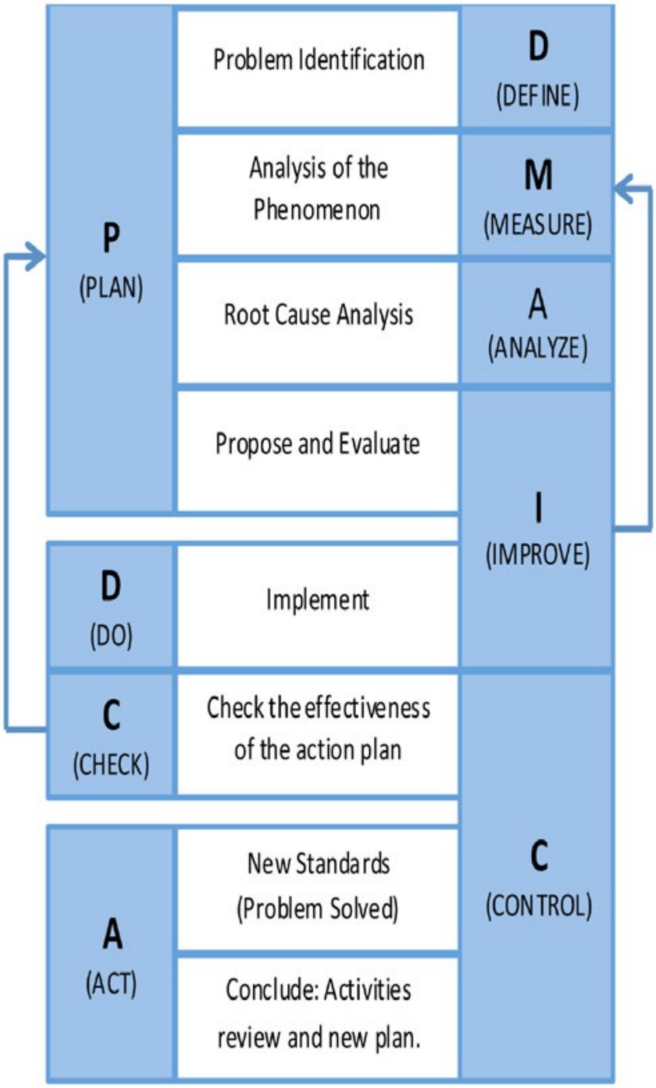

Figure 3: PDCA and DMAIC[2].

References

1. The Evolution of Six Sigma by Jim Folaron, J.P. Morgan Chase & Co, August 2003.
2. Métodos PDCA e DMAIC e Suas Ferramentas Analíticas by Cristina Werkema.

Renato Peres is an industrial engineer and production coordinator with Circuibras Circuitos Impressos Profissionais.

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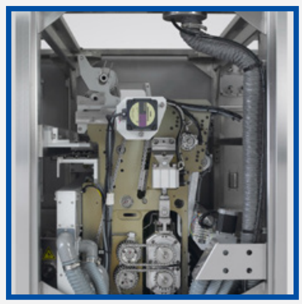

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Highlights

Outstanding Group of Companies and Individuals Receive FlexTech's FLEXI Awards
FlexTech, a SEMI Strategic Association Partner, awarded five FLEXI Awards in the categories of Innovation, Research & Development, Leadership in Education, and in a category new this year, Industry Leadership.

Insulectro Debuts Shikoku New Chemistry Supplier at IPC APEX 2016
Insulectro, a leading supplier of materials for use in the PCB and printed electronics industries, will introduce a new supplier, Shikoku Chemicals Corporation, at IPC APEX EXPO to augment its highly successful chemistry line.

ITL Circuits Invests in Excellon COBRA Hybrid Laser System
Excellon is proud to announce the sale of a COBRA Hybrid Laser System to ITL Circuits in Markham, Ontario. The installation is scheduled for early second quarter of this year.

Speedy and Metro Circuits Install New Chemcut CC 8000
Chemcut Corporation, the United States' leading manufacturer and supplier of develop/etch/strip equipment, announces that PJC Technology Inc., DBA Speedy Circuits and Metro Circuits, have both installed new Chemcut CC 8000 cupric chloride develop-etch-strip systems in their facilities.

Atotech Opens a New Chemical Plant in Penang
With an initial investment of RM 50 M, the new facility will cater to the growing demand of Atotech's solutions in South East Asia.

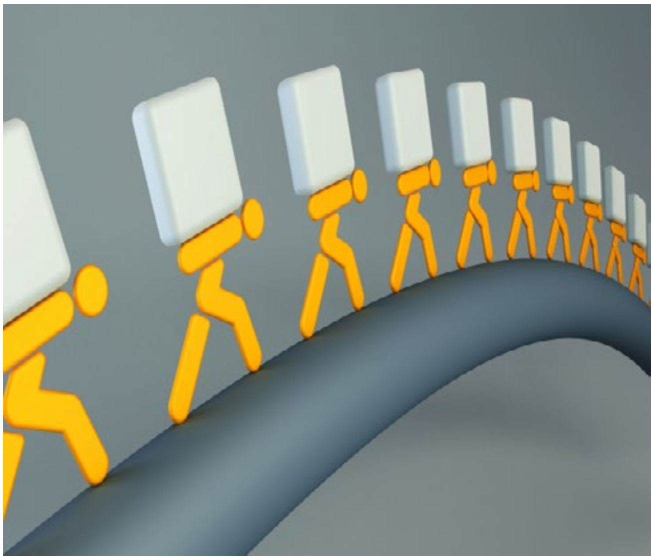
LPKF Launches Entirely New Flex Drilling & Cutting Laser
Electronics manufacturing equipment manufacturer and laser specialist LPKF Laser & Electronics AG is launching an entirely new laser drilling and cutting system specifically tailored to the needs of the flexible circuit industry.

Insulectro Promotes Michelle Walsh to Director of Product Management
Insulectro, a distributor of materials for use in the printed circuit board and printed electronics industries, has promoted long time associate Michelle Walsh to director of product management.

Viking Test Unveils Expansion Activities
Viking Test moved to new UK headquarters facility. The new facility with 15000 sq. space gives Viking enough opportunity to accommodate current workload and future expansion plans.

Insulectro Hires Industry Vet Chris Hrusovsky as VP of Sales for Chemistry
Insulectro has hired industry leader Chris Hrusovsky as VP of Sales for Chemistry. "I am pleased today to announce Chris Hrusovsky has joined the Insulectro family," commented Patrick Redfern, president of Insulectro.

Catching up With Tom Hausherr of PCB Libraries
When fate placed Tom Hausherr and me at PCB West, we made sure to carve out some time together. Tom agreed to have a long breakfast with me so I could learn more about the challenges related to component libraries and how his company addresses these issues. So, pull up a chair and join us for a chat.



Flexible Circuits and Kaizen Events

by Dave Becker
ALL FLEX FLEXIBLE CIRCUITS LLC

All Flex uses a variety of different tools and techniques in its continuous improvement efforts. A Kaizen event or Blitz is one technique that has resulted in significant improvements in our yields, productivity and customer satisfaction. A Kaizen event is a short-term effort using a dedicated team that is highly focused on improving a narrowly defined process. Kaizen teams usually consist of 3–8 members that include operators, engineers and other support personnel. The implementation phase of the event usually lasts 3–6 working days and the team members are removed from their daily duties to focus 100% of their time on the Kaizen effort.

A Kaizen event is highly structured, and while the exact steps may vary from project to project, the process consists of three phases:

- Planning and preparation
- Implementation
- Follow-up and tracking

Action items, analysis and recommendations are formally documented during each phase. The first step is to select and define the project. Kaizen events, as well as other improvement efforts, are selected based on a Pareto analysis that is presented to the management team. Selection is based on the process improvement that would have the biggest impact on one of the following:

- Scrap
- Throughput
- Quality
- Customer satisfaction

The planning and preparation phase of a Kaizen blitz can take 2–6 weeks. During this phase, the project charter is defined, a team is chosen, data collected and project orientation is performed. The Kaizen event can be disruptive, so the affected departments need to plan on how to deal with the potential disruptions.

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Since the team members will be dedicated to the event, replacement personnel may need to be identified and trained.

All Flex often brings in an experienced facilitator to work with the team during the implementation phase. Key elements of the implementation phase are:

1. Understanding the current state
2. Determining the future state
3. Making improvements
4. Standardizing new process
5. Training appropriate personnel
6. Implementing progress tracking

The facilitator will bring in the needed training. For example, the team is often trained on the seven wastes: Transportation, Inventory, Motion, Waiting, Over-production, Over-processing and Defects.

The facilitator may bring in other tools for analysis and implementation as needed. Often, Kaizen events employ analysis tools that include herringbone diagrams, IS/IS NOT charts, scatter diagrams, and process diagramming tools.

As the team analyzes the current state, identified waste elements are documented. An improved process is mapped out with the key waste elements eliminated or reduced. The changes identified in the future state are implemented quickly (within one day or less).

Once the new process is implemented, measurements are put in place to track the improvements. Documentation is modified to standardize the changes and all appropriate personnel are trained. The team also determines future actions needed as well as other opportunities and pitfalls discovered during the event.

Soon after the event, a presentation is made to the management team. The presentation will include future recommendations and a review of open action items. A follow-up meeting is scheduled to review the action items and determine if the improvements are being maintained.

The team members and supporting personnel are formally recognized. The Kaizen event is highly visible throughout the organization. It is important that all members involved find the experience rewarding and look forward to participating in additional Kaizen events.

Kaizen events can be very effective, but it is important to understand when it is appropriate to use this method rather than other techniques. It is tempting to believe that everything can be improved with a quick-fix effort; unfortunately not everything can be solved that way. Some issues, such as process variation, are deep rooted, and can take months of analysis and dozens of designed experiments before the root problems are identified and addressed. Solutions to these problems may require major equipment modifications, new process materials and significant process redesign.

"Some issues, such as process variation, are deep rooted, and can take months of analysis and dozens of designed experiments before the root problems are identified and addressed."

Remember, it is good to use a lot of tools for continuous improvement and to make sure the correct tools are used when attacking a problem.

"If all you have is a hammer, then everything looks like a nail."

—*Abraham Maslow* **PCB**

Dave Becker is the V.P. of sales and marketing at All Flex Flexible Circuits and Heaters. To contact Becker, or read past columns, click here.

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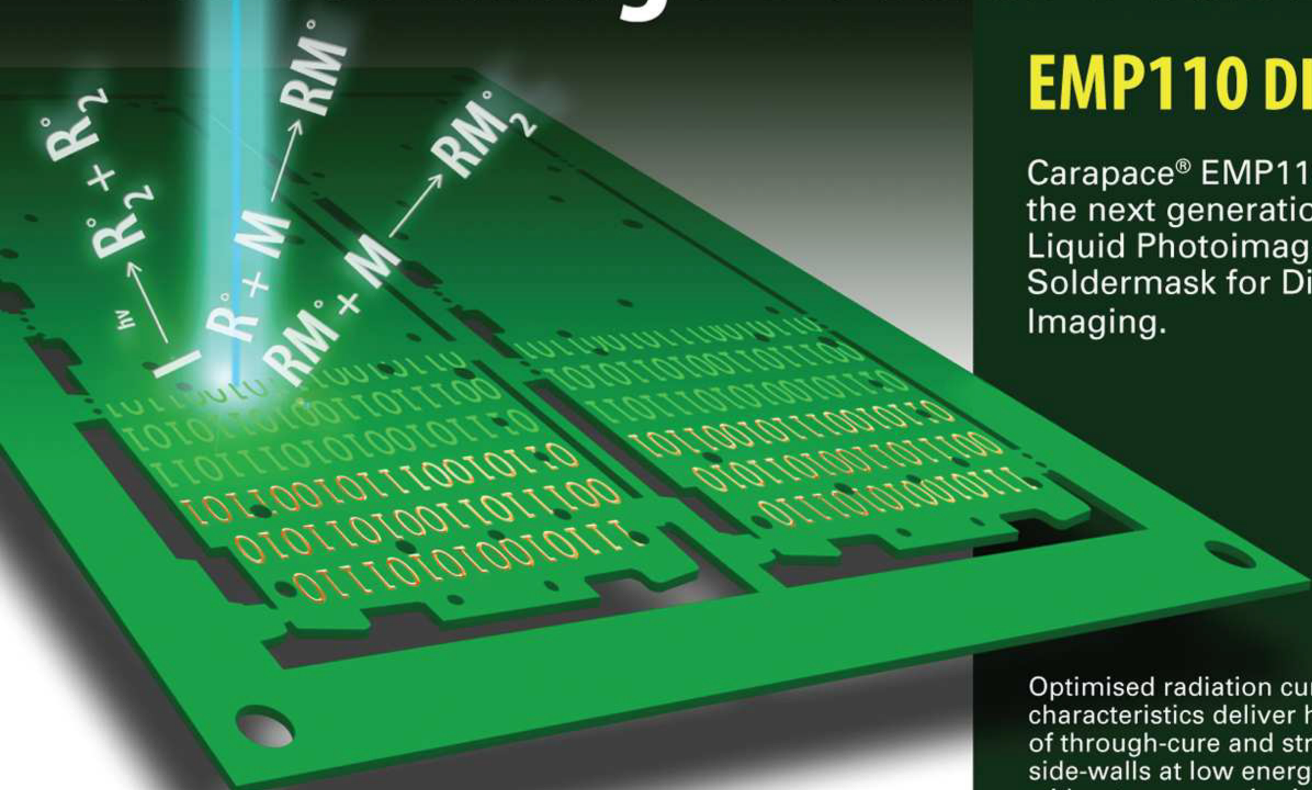

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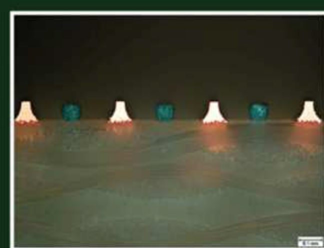

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Best Practices: It's Only Common Sense

by Steve Williams
THE RIGHT APPROACH CONSULTING LLC.

One of the fascinating things about Best Practices is that it is occurring everywhere—and many times without the knowledge of the person or organization doing it! How can this be? Most best practice principles fall under a very old-fashioned ideal that some of us still remember: common sense.

We Don't Need No Stinkin' Lean

I recently visited a small family-owned client, and during the course of a discussion with the owner the topic of Lean came up. Ned, the owner, was more than eager to share his position that they didn't feel the need for Lean. He went on to explain that his company had been in business for over 50 years, and that the average employee tenure was 23 years of service. Ned was very proud to tell me that over the years this experienced workforce had honed their manufacturing best practices to the point that they felt no additional benefit would be gained with Lean. I said, "OK Ned, let's take a walk."

One of the first workstations we visited had a pegboard with all of the operator's hand tools outlined and hanging from it. I asked Ned what this was all about, and he proudly stated, "Rita noticed that her people spent a lot of time looking for their tools every morning before they could start work, so we decided it would be a good idea to place all the tools in easy reach, and give each tool a visual aid for where it belongs." I subtly explained that they had embraced two Lean concepts with this improvement: elimi-

Shadow Board

Cutout Shadow Board

Figure 1: Examples of shadow boards.

nating motion waste (one of the Seven Deadly Wastes) and the 5S methodology of Seiton, or to Set in Order (Figure 1).

At the next workstation I asked Ned why this process was set up in a horseshoe-shaped workflow. Ned said, "Gunther here is my production manager, and he told me one day that a lot of time was being wasted toting product from one end of the plant to the other to different machines for processing. So we decided that it would make sense to physically relocate the machines closer together, in the exact sequence needed, to minimize this wasted time." I gently suggested that the U-shaped cell concept exemplifies the Lean goals of reducing waste and manufacturing footprint while increasing productivity and efficiency. Needless to say, virtually every step throughout Ned's process had its roots in Lean principles. Best practices are everywhere!

An Apple a Day

I happened to have had a very interesting 2015 from a medical sense, and spent a lot of time with my doctors. During a recent appointment, as Kyle, my doctor's P.A., led me down the hall to the little patient room, he said, "The Doc has reorganized his patient rooms to always be scheduled in the three rooms next to his office instead of spread out wherever there is an open room." Finding this curious, I said that the move makes sense, and asked him how he came up with the idea. He told me, "We are doing the whole best practices thing," and continued to tell me that all the medical records are now digital and everyone carries around laptops to always have updated patient information wherever they are.

As we did all the prep work, Kyle brought up my most recent MRI results on his laptop and went over the results (all is well, BTW), and when finished, said the Doc would be right in. Doctor Max came in five minutes later with his iPad, and not only had the same MRI results, but also the notes Kyle had just updated. With all the complaints about the wait time during doctor visits, it was rewarding to see one small practice trying to do something about it. They get it, and this small example personifies the essence of how best practices can work in the service sector. Best practices are everywhere!

Nancy's Sour Cream Poka-Yoke

Although this story is a bit dated, it bears repeating. My wife Nancy and I went out to dinner on a Friday evening, looking forward to a great charbroiled steak. The restaurant was quite busy and the staff was really hustling from the Friday fish fry crowd (a tasty tradition here in Wisconsin). Our dinners arrived, and Nancy

set out loading up her baked potato with butter and sour cream and dug in. As I was enjoying my steak, I looked up to see a dour expression on my wife's face, and remember thinking "this can't be good" when she thrust out her little black cup of sour cream and said "Honey, taste this." Being the good husband that I am, I bravely took a taste and must have had that same look on my face as she said she thought it was tartar sauce, not sour cream.

With the large amount of fish fry orders being served, the waitress must have grabbed the wrong container. When the waitress brought Nancy's replacement potato and the little black cup of sour cream, she said, "You know, they ought to put the tartar sauce in a different colored cup!" I said, "Nice Poka-Yoke sweetheart," to which she replied, "Honey, watch your language, there are kids at the next table."

I quickly explained that Poka-Yoke was a best practices methodology meaning mistake-proofing, and that she had just invented a visual aid Poka-Yoke that would keep the staff from mixing up the sauces. Best practices are everywhere!

It's Only Common Sense

During another recent visit with a long-term client, I had a great discussion with Tom, a fellow old-school manager (and friend) on the merits of best practices. He told me, "Steve, I don't know what all the fuss is about best practices; we have been doing it forever but never called it best practices; it's just common sense," which is the whole point of this article. Best practices truly are everywhere! **PCB**

Steve Williams is the president of The Right Approach Consulting LLC. To read past columns, or to contact Williams, click here.

I-Connect007 Exclusive: Walt Custer Elaborates on his IPC APEX EXPO Industry Forecast

When Walt Custer speaks, the IPC APEX EXPO crowd listens carefully. And as always, his annual presentation forecasting the upcoming year for the industry was much anticipated and well-attended. Publisher Barry Matties had the chance to meet up with Walt at the show, to dig a little deeper into the details of his findings.

In this year's annual presentation, Walt followed the entire electronics supply chain, tracking the economy, electronic equipment demand, components, EMS and ODM companies, materials and more. Leading indicators predict business conditions two to six months in advance, and Walt's suggestion was that business will be nearly flat until at least mid-2016.

Another key factor is currency exchange rates; the U.S. dollar is strong versus other currencies which makes U.S. exports more expensive. This has also affected the financial results of multinational companies that report in U.S. dollars.

With slowing growth of smartphones, tablets and PCs, there is no big end-market driver. Automotive is still key with electronic content constantly rising and self-driving cars on the horizon, but it is not yet robust enough to replace the lost volume. Markets such as wearables, robots and the IoT could become drivers, but are still in their infancy.

Read Walt's in-depth interview with Barry here and learn how you can receive a copy of Walt's entire IPC APEX EXPO 2016 annual presentation.

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Electronics Industry News
Market Highlights

Quantum Computer Factors Numbers, Could be Scaled Up

What are the prime factors, or multipliers, for the number 15? Most grade school students know the answer—3 and 5—by memory. A larger number, such as 91, may take some pen and paper. An even larger number, say with 232 digits, can (and has) taken scientists two years to factor, using hundreds of classical computers operating in parallel.

Building Living, Breathing Supercomputers

The substance that provides energy to all the cells in our bodies, Adenosine triphosphate (ATP), may also be able to power the next generation of supercomputers. That is what an international team of researchers led by Prof. Nicolau, the Chair of the Department of Bioengineering at McGill, believe.

Quantum Dot Solids: This Generation's Silicon Wafer?

Just as the single-crystal silicon wafer forever changed the nature of electronics 60 years ago, a group of Cornell researchers is hoping its work with quantum dot solids—crystals made out of crystals—can help usher in a new era in electronics.

New ORNL Method Could Unleash Solar Power Potential

Measurement and data analysis techniques developed at the Department of Energy's Oak Ridge National Laboratory could provide new insight into performance-robbing flaws in crystalline structures, ultimately improving the performance of solar cells.

In Emergencies, Should You Trust a Robot?

In emergencies, people may trust robots too much for their own safety, a new study suggests. In a mock building fire, test subjects followed instructions from an "emergency guide robot" even after the machine had proven itself unreliable—and after some participants were told that the robot had broken down.

Investors Paying Closer Attention to Corporate Governance Strategies

Poor corporate governance can lead to ineffective strategic decisions and a weak culture and management that can ultimately lead to increased environmental and social risks. For investors, such risks can destroy the value of a business, irrespective of the attractiveness or price of its assets or its market share.

The Future of Fuel Cells: Better-Performing and Less Expensive

To the uninitiated, fuel cells are typically compared to batteries. The working principle of each is generally the same: a chemical reaction produces a quantity of energy which is then converted into usable electric power. But unlike a battery, you never recharge a fuel cell. You keep feeding it fuel and it keeps producing electricity.

Stretchable Electronics that Quadruple in Length

EPFL researchers have developed conductive tracks that can be bent and stretched up to four times their original length. They could be used in artificial skin, connected clothing and on-body sensors.

Emergence of 5G and Industry 4.0 to Ignite the Global Test and Measurement Market

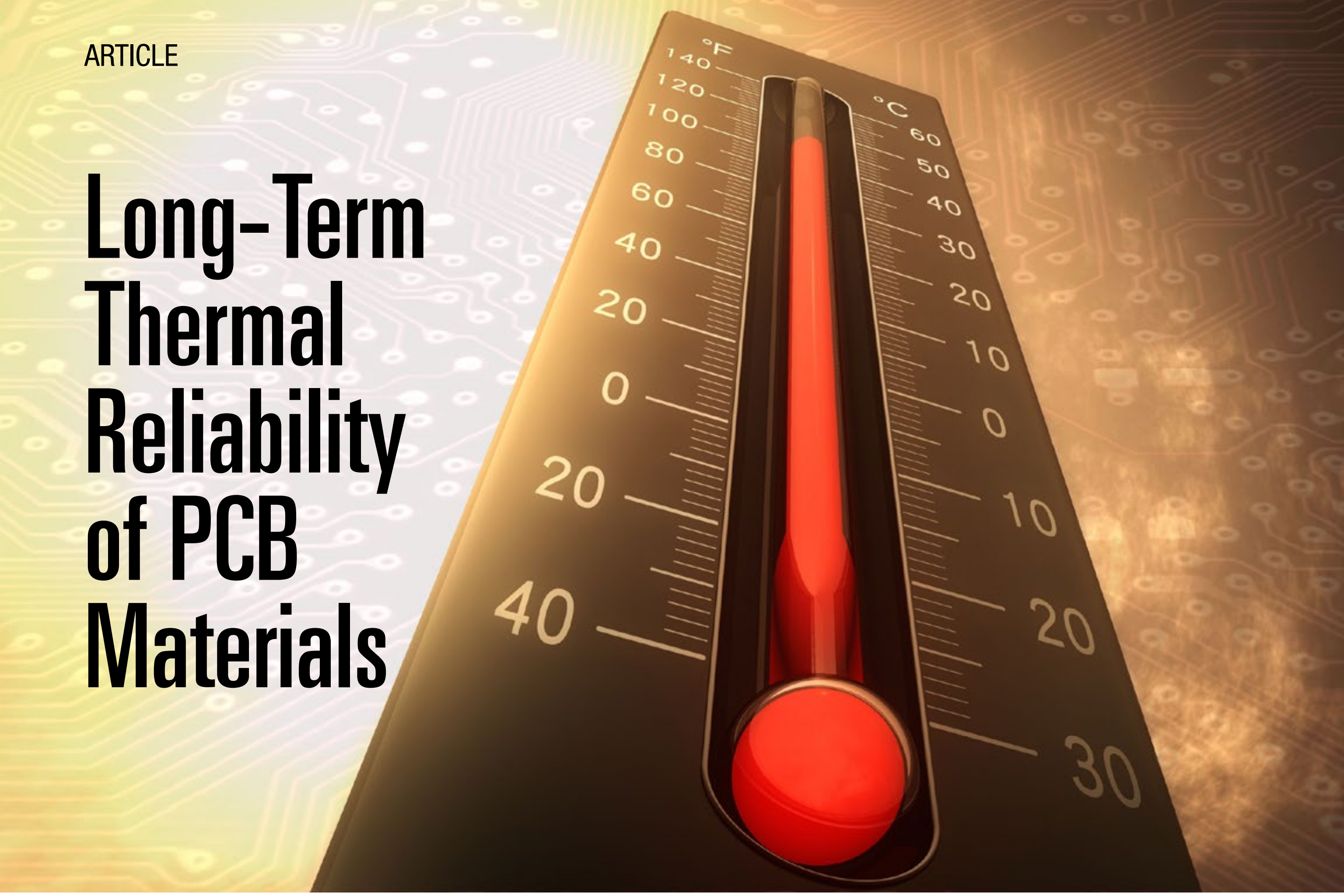
The ubiquity of connected devices and the rising relevance of the Internet of Things (IoT) will provide a huge boost to the test & measurement market, specifically, the communication testing segment.

China's Infrastructure Initiative Driving Financial Reform

China's "Belt and Road" infrastructure initiative is an essential part of the country's domestic economic rebalancing and its outbound ambitions. The initiative entails investing billions of dollars into infrastructure such as railways, highways and ports that link mainland China and the dozens of countries to its west and south.

ARTICLE

Long-Term Thermal Reliability of PCB Materials



by Eva McDermott, Ph.D., Bob McGrath, and Christine Harrington
AMPHENOL PRINTED CIRCUIT BOARD TECHNOLOGY

Abstract

This paper describes the purpose, methodology, and results to date of thermal endurance testing performed at Amphenol Printed Circuit Board Technology in Nashua, NH. The intent of this thermal aging testing is to establish long-term reliability data for PWB materials for use in applications that require 20+ years (100,000+ hours) of operational life under different thermal conditions. Underwriters Laboratory (UL) testing only addresses unclad laminate (resin and glass) and not a fabricated PWB that undergoes many processing steps, includes copper and plated through holes, and has a complex mechanical structure. UL testing is based on a 5000 hour expected operation life of the electronic product. Therefore, there is a need to determine the dielectric breakdown/degradation of the composite PCB material and mechanical structure over time and temperature for mission critical applications.

Thermal aging testing consisted of three phases.

- Phase I: 500-hour pre-screen at four fixed temperatures following IEEE98 A.1 and UL746B 20A[1] (completed)
- Phase II: Short-term aging for 1000 hours at four revised, fixed temperatures. Plated through-hole reliability testing using IST and HATS was also completed
- Phase III: Long-term aging for 25,000 hours at five, revised fixed temperatures

This paper will discuss results of this testing to date.

Introduction

The objective of this testing is to establish the electrical strength-temperature Arrhenius curve (temperature life curve) for materials used in PWB for applications that exceed the typical 5,000 hour end of life test defined in UL Standard UL746B[2]. The test methodology presented in this report generates data representing 25,000 hours of operational life. The 25,000 hour test

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data can then be used to extrapolate out to 100,000 hours to determine the expected electrical strength of the various laminate materials being compared. This data can be applied to the PWB design requirements by balancing the expected material degradation at 100,000 hours against the required dielectric needs throughout the service life of PWB assembly. Design elements can then be adjusted (material selection, stack up, trace size and spacing, copper weight, ground planes, heat sinks, etc.) to ensure that the PWB remains within the thermal boundaries established by the temperature life curve.

Loss of electrical strength due to thermal exposure must be a key consideration in the design of a PWB for the expected life of an application. Chemical changes within laminate are accelerated when the insulation of the PWB is exposed to elevated operating temperatures. Oxidation occurs degrading the physical and electrical properties of printed wiring board causing embrittlement, discoloration, and delamination. The thermal-aging characteristics of a laminate can be determined by measuring the changes in its properties to a predetermined level by aging at each of several elevated temperatures. In this study, dielectric strength is used to determine the relative effects of different temperatures on the end of life for a given insulating system. It is also used to compare different insulating systems at a given temperature. It is important that the design and construction of the PWB test vehicles are representative of the intended application and be consistent from laminate to laminate.

Most data available on the thermal aging of laminate materials was specifically developed on the unclad laminate composite (resin and glass). To properly determine the thermal aging characteristics of a PWB, temperature life testing must be performed on a manufactured PWB, not raw laminate. The internal structure of the board itself (amount of heat sinking capacity, density of power generating components) and the intended use environment will also affect the operational life of a PWB. In addition, manufacturing processes can be deleterious to the operational life of a fabricated PWB. Laminates will experience a number of chemical exposures, thermal excursions, and mechanical stresses during fabrication. Good process control is critical in eliminating contaminants, obtaining proper bonding surfaces and good adhesion, and preventing mechanical and thermal damage to the laminate itself. If these processes go out of control or are poorly defined, operational life can be adversely affected. These intangibles must be taken into consideration when analyzing data and predicting the operational life of a PWB.

The times to failure in thermal aging test cannot be quantitatively related to the operational life of a laminate system in actual use. However, they do provide a relative indication of a PWB's service life under the specific conditions of the test. Results of shorter time tests at higher temperatures can be extrapolated to longer times at lower temperatures. Material aging standards such as UL 746B and IEEE STD 99 limit the degree to which material life data can be extrapolated. They indicate that material thermal aging testing should be performed for at least 25% of the desired operation life of the material. In order to obtain sufficient aging data for 100,000-hour operational life requirements, test duration must be at least 25,000 hours.

Test Methodology

Determining the operational life of printed circuit board laminates after thermal aging consisted of a three step approach following test details and calculations outlined in IEEE98 A.1 and UL746B. Testing materials with this approach helps marry material capabilities with design requirements so proper trace spacing or other counter measures can be implemented to meet an intended design operational life of 100,000 hours. Guidance on the test methodology was provided by DfR Solutions.

Phase I: 500 hours pre-screen at four fixed temperatures following IEEE98 A.1 and UL746B 20A to estimate the high temperature test boundary for long-term aging of PWB laminate material capabilities. Pre-screen data is used as an initial sort on best performing material. Criteria evaluated include highest dielectric strength, lowest overall degradation, lowest percent change in degradation, and anomalous or unexpected behavior (indicating instability).

A pre-screening test lasting 500 hours was first employed using four fixed temperatures to estimate the high-temperature test boundary for long-term aging testing of PWB laminate material capabilities. The four temperatures used varied by material with the Tg (glass transition temperature) of the material being weighed heavily in selection of the upper temperature range. Dielectric breakdown voltage was measured at time zero and after 500 hours at elevated temperatures using a Hipotronics 750-2D149 AC Dielectric Analyzer. The % retention of dielectric strength compared to baseline measurements was calculated for each temperature. From these results, the 50% EOL (end of life) was assigned. Due to the nature of short-term testing, it was not used to estimate low temperature boundaries as insufficient material change would be expected when testing at a low temperature for a short period of time. This test is largely based on the testing outlined in IEEE STD 98, Annex A, fixed time frame method (FTFM) of sampling.

Phase II: Short-term aging for 1,000 hours at four revised, fixed temperatures was used to develop a thermal endurance graph to extrapolate and validate 500 hour degradation temperature and the 5,000 hour degradation temperature for the 25,000-hour life test. After performing the pre-screen analysis, this data was used to help guide selection of aging temperatures. The 1000 hour test used more aggressive temperatures as bounded by the pre-screen data and UL746A procedure. Data was first analyzed in a similar fashion to the pre-screen data to identify potential outliers or worrisome behavior. Arrhenius plots were constructed for an initial prediction on behavior and performance.

For short-term aging for 1,000 hours at four revised temperatures was run next, % retention of dielectric strength was calculated at each temperature. Next, % retention data (one curve per temperature) was plotted vs. time (X-axis). From this data, 50% end of life was determined for each material. A thermal endurance graph was generated in order to extrapolate and validate the 500-hour degradation temperature and 5,000-hour degradation temperature to select the temperatures for the long-term operational life test for 25,000 hours.

In addition to the thermal endurance testing, interconnect stress testing (IST) and highly accelerated thermal shock (HATS) testing were also performed to assess mechanical robustness of plated through holes for each laminate. Outside testing services PWB Interconnect Solutions, Inc. and Integrated Reliability Test System, Inc. were used respectively.

Phase III: Long-term aging for 25,000 hours at four revised, fixed temperatures was used to develop a thermal endurance graph to extrapolate and validate 100,000-hour operational life temperature. Testing is approximately 40% complete at this time. Long-term aging will be performed for a minimum of 25,000 hours. Arrhenius plots from the six-week test were used to predict a certain degradation percentage in a given time frame.

Long-term aging for 25,000 hours at five revised temperatures was run next. Again, % retention of dielectric strength was calculated at each temperature. Next % retention data (one curve

Material	Descriptor	Descriptor 2	Tg, °C	RTI, Electrical
Laminate A	Widely Used	Standard Performance Epoxy	180	130
Laminate B	Limited Use – Application Specific	High Speed Performance - Non-Epoxy Filled	200	130
Laminate C	Limited Use – Application Specific	High Temperature Resistant – Filled	190	130
Laminate D	Limited Use – Application Specific	High Temperature Resistant – Filled	160	160
Laminate E	Specific Use (RF)	High Temperature / Microwave – Filled	>280	160

Table 1: Materials Tested.

per temperature) was plotted vs. time (X-axis). From this data, 50% end of life was determined. A thermal endurance graph was generated in order to extrapolate and validate the 100,000 hour life temperature. The importance of the 25,000 hour test is based on industry practices of extrapolation of life expectancy data. In order to have any confidence of predicting material properties at 100,000 hours, the test length has to be 25% in duration.

The following materials in Table 1 were down selected from a much longer list of PWB laminates. Press fit compatibility; comparative tracking index (CTI), flammability, dielectric breakdown voltage, and glass transition temperature (Tg) were used to select five laminates for thermal aging testing.

Thermal aging of PCB laminates was performed on three manufactured lots of PCB test vehicles. Testing a processed PWB is necessary because manufacturing processes expose the laminate to a number of thermal and chemical cycles. These exposures can have an effect on the material's properties and robustness. In Amphenol's study, the test vehicle consisted of a fourteen layer printed circuit board manufactured in accordance with IPC-6012, Class 3 meeting the workmanship standards of IPC-A-610, Class 3. Copper foil weights were 2 oz. for all inner layers and 1 oz. for both outer layers to simulate actual design stack up for the specific application and intended use.

Test coupons were designed to allow separate tests to be performed at three design regions on the board. Figure 1 illustrates the stack up used as well as the test points—X/Y test point within the plane of an inner layer across a 10 mil gap, Z-Core test point between the plane of the inner layer (Z-axis of a core, 5 mil span), and Z-Fill test point between the plane of the fill (Z-axis through prepreg, 10 mil span).

Ten test specimens were used for each set for thermal end point testing. For each material the following test specimen quantities were used. Eight sets per temperature x 5 temperatures = 400 test specimens. Six spares per temperature x 5 temperatures = 30 test specimens. Materials tested include Laminate A, B, C, D and E. Twenty test specimens per material were used to establish the baseline for dielectric strength testing. For each manufacturing lot of material included in the test, there were a minimum of five test specimens from each manufacturing were included in the baseline dielectric strength test.

Control materials with known performance were tested in conjunction with the test materials. The control material configuration was in the form of 3" x 5" sheet (unclad) to match

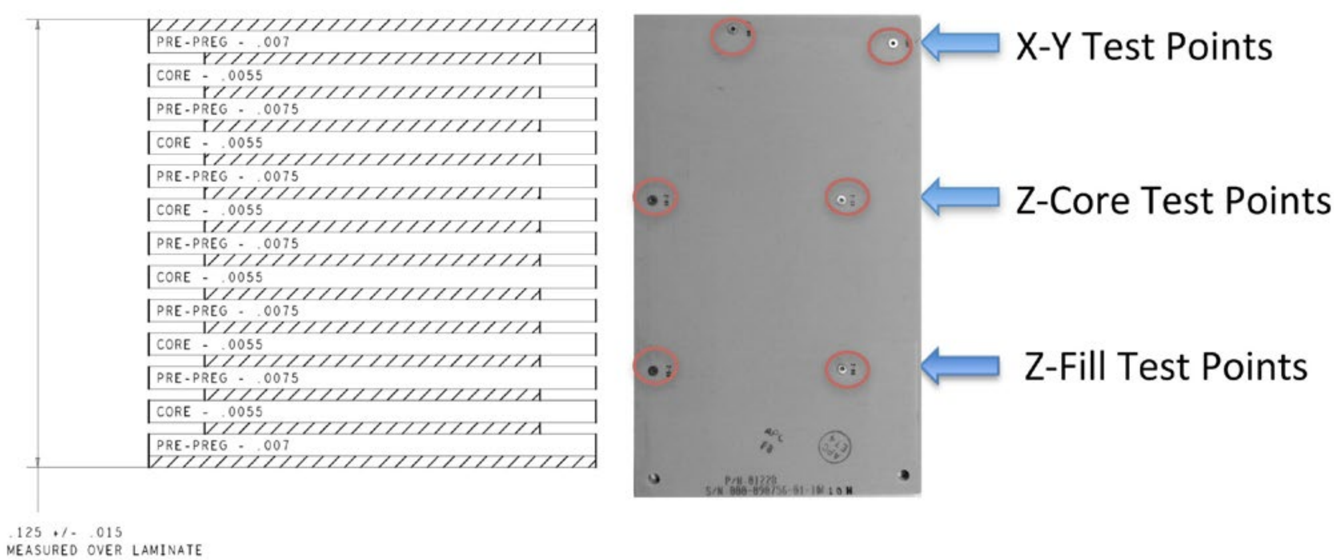


Figure 1: Test vehicle stack-up and test points on test vehicle.

original testing of the control material by the supplier and UL. Control materials were selected so that at least two temperatures/data points overlapped with the materials under evaluation. Multiple test materials were used to address the range of test temperatures for the materials being tested and included Control 1, 2, and 3. Control materials were included in each oven being used for thermal aging testing. Control material data was compared to existing data from suppliers and UL to prove out the PWB test validity.

All samples (controls, baselines, and thermally aged test vehicles) were pre-conditioned following ASTM D618: Standard Practice for Conditioning Plastics for Testing, 48 hours at 25°C and 50% relative humidity. Dielectric breakdown voltage was determined following ASTM D149: Standard Test Method for Dielectric Breakdown Voltage and Dielectric Strength of Solid Electrical Insulating Materials at Commercial Power Frequencies[4]. The test was performed at a frequency of 60Hz and a voltage ramp rate of 500V/sec using a Hipotronics 750-2D149 AC Dielectric Analyzer. The fixture used for hipot testing the test vehicles is shown below in Figure 2. Each test vehicle was tested in the X-Y (PTH to PTH), Z-Core (laminate core), and Z-Fill (prepreg). Dielectric failure or dielectric breakdown consists of an increase in conductance, limiting the electric field that can be sustained.

Randomization of samples was carefully considered through all test phases. This included sample selection based on sample ID which contained Lot #, Panel #, and Panel Position, A–P (Figure 3). It is theorized that similar colored circuits will have reasonably similar electrical performance.

Oven location was also planned and noted on all oven sample logs. Samples and controls were mixed within a rack (typically no more three in a row of either). Rack number and position of rack in oven were meticulously tracked. It should also be noted that bromine containing laminates were thermally aged in separate ovens than the non-bromine containing laminate systems. This was done to prevent any cross contamination that may arise due to out gassing during the thermal aging tests. A total of twelve Sun Electronic System, Inc. ovens, Model EC16HA-LM were used for thermal aging. All ovens were continuously monitored for temperature stability using an Agilent 34972A LXI Data Acquisition/Switch Unit with an Agilent 20 Channel Multiplexer Model 34901A. All ovens had two thermocouples for redundancy. Figure 4 illustrates sample racking and sample location in oven.

The test plan followed is presented in the flow diagram in Figure 5. It illustrates the preconditioning, weighing, aging, post conditioning, final weighing, and dielectric breakdown test sequence for controls and test vehicles.

Results and Discussion

500-Hour Pre-Screen Testing

The 500-hour pre-screen at four fixed temperatures was executed following IEEE98 A.1[3]

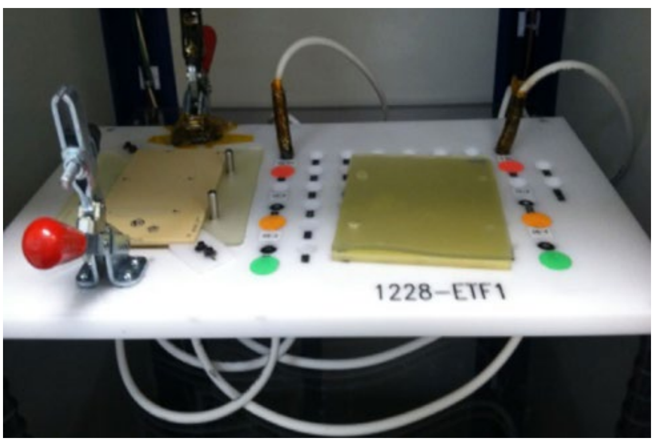


Figure 2: Hipot test fixture.

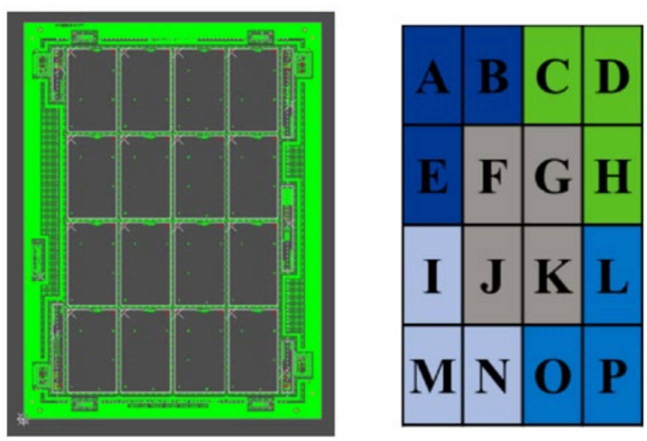


Figure 3: Circuit location on panel.

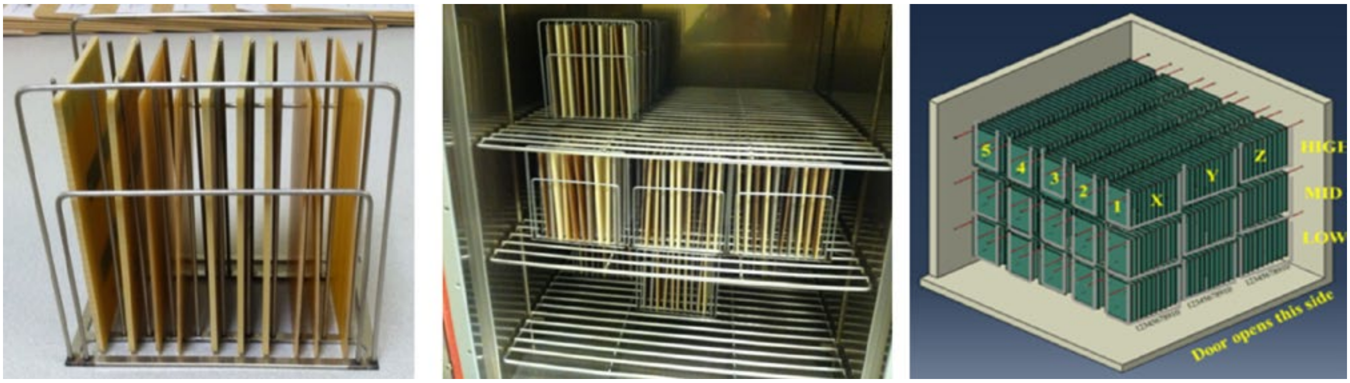
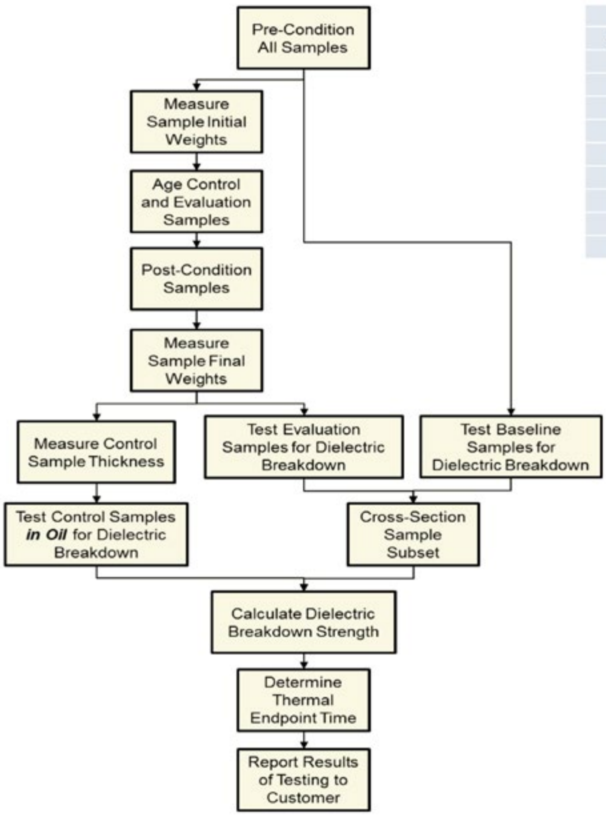


Figure 4: Sample racking, racks in oven, and sample location naming scheme.



1000 Hour Sampling Schedule				
Set	Remove from Oven (days)			
	T1	T2	T3	T4
1	1	1	1	1
2	3	3	3	3
3	7	7	7	7
4	14	14	14	14
5	21	21	21	21
6	28	28	28	28
7	35	35	35	35
8	42	42	42	42

Long Term Sampling Schedule Duration (days)					
Test	T5	T4	T3	T2	T1
Sets 1-5 In	3D	7D	14D	28D	42D
Set 6 In	3	7	14	28	42
Set 7 In	6	14	28	56	84
Set 8 In	9	21	42	84	126
Set 1	9	21	42	84	126
Set 2	21	49	98	196	294
Set 3	33	77	154	308	462
Set 4	45	105	210	420	630
Set 5	57	133	266	532	798
Set 6	63	147	294	588	882
Set 7	69	161	322	644	966
Set 8	75	175	350	700	1050

Figure 5: Flow diagram of testing sequence for controls and test vehicles for Phase I through III along with sample schedules for the 1000-hour test and two-year long-term test.

and UL746B 20A[1] to estimate the high-temperature test boundary for long-term aging of PWB laminate material capabilities. Pre-screen data is used as an initial sort on best performing material. Criteria evaluated include highest dielectric strength, lowest overall degradation, lowest percent change in degradation, and anomalous or unexpected behavior (indicating instability).

DfR Solutions completed the first portion of testing, consisting of a 500-hour prescreen aging test of five materials at four different temperatures. Results from the 500-hour prescreen were used to adjust test parameters for the next phases of testing. Data collected includes weight loss, sample thickness, dielectric breakdown voltage for baseline and sample coupons after exposure to for different temperatures for 500 hours. Five data points were collected per measurement point.

Each material was tested to collect ten baseline data points in the X-Y, Z-Core and Z-Fill areas of the test vehicle. Using the published electric strength data—the estimated dielectric withstand voltage (DWV) failure point was calculated. Average, standard deviation, and range were calculated. A summary of the baseline averages is presented below in Table 3. Laminate C and Laminate D have the highest dielectric withstand voltage values compared to the others in the test set.

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Material	Tg, °C	T1, °C	T2, °C	T3, °C	T4, °C
Laminate A	180	165	175	185	195
Laminate B	200	175	185	195	205
Laminate C	190	175	185	195	205
Laminate D	160	165	175	185	195
Laminate E	>280	220	240	260	280

Table 2: Temperatures Used for 500-Hour Test Based on Tg of Material and Supplier's Recommendations.

Average Breakdown Voltage (V)	Laminate A	Laminate B	Laminate C	Laminate D	Laminate E
X-Y	17005	14758	22581	18889	13181
Std. Dev.	1841	1666	2612	2162	1413
Z-Core	9560	9523	11281	12823	8923
Std. Dev.	598	611	1541	977	585
Z-Fill	13956	19185	23893	17096	12530
Std. Dev.	1304	2075	1448	3088	1169

Table 3: Average Breakdown Voltage Time Zero.

Results for the average percentage change in weight are illustrated in Figure 6. Weight measurements indicate a general trend of increasing weight loss as aging temperature increases in all materials. This indicates that the boards are generally degrading as expected, with oxidation accelerated at higher temperatures. All aged boards showed discoloration to various extents at the end of testing. Laminate A and Laminate E boards also exhibited delamination at higher aging temperatures. It was later discovered that temperatures selected for Laminate E were too high. Figure 7 illustrates the average percentage change in thickness for each laminate. Laminate A had obvious delamination at T3 (185°C) and T4 (195°C). Laminate E showed delamination at all four temperatures tested (220°C, 240°C, 260°C, and 280°C).

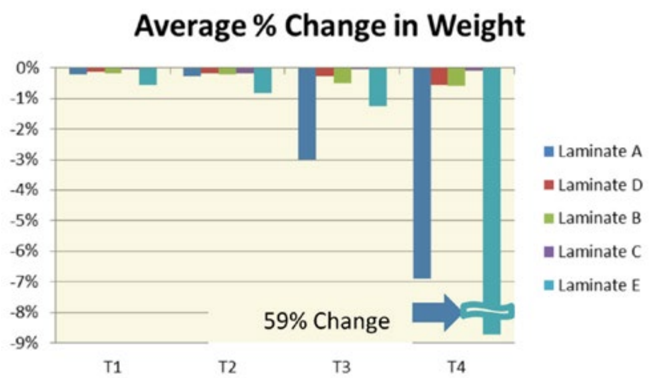

Figure 6: Average % change in weight for 500-hour test vehicles.

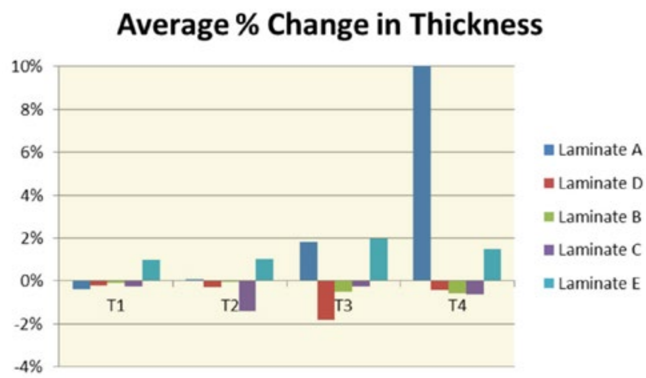

Figure 7: Average % change in thickness for 500-hour test vehicles.

Dielectric breakdown voltage varied by material and test region. Laminate A breakdown voltages remained steady up to T3 (185°C), where the voltages in all regions sharply dropped. Laminate D breakdown voltages remained fairly steady in all aging temperatures and test regions. Laminate B breakdown voltages remained fairly steady in all aging temperatures and test regions. Laminate C breakdown voltages demonstrated a decline in strength, particularly at higher temperatures. Laminate E breakdown voltages declined steadily, but unexpectedly recovered at T4 (280°C).

The increase in Laminate E breakdown voltages at T4 corresponds with a sharp increase in weight loss at that temperature, as well increased delamination and general degradation of the board condition. The higher breakdown voltages could be caused by a number of factors, and do not necessarily indicate a higher dielectric strength in the material at that temperature. Heavy delamination may have resulted in the copper components of the board being exposed to more air, causing formation of copper oxides and degrading the test circuit's ability to conduct electricity. The markedly increased weight loss, -9% at 280°C compared to -1% at 260°C, indicates the higher temperature may be causing certain compounds in the material to decompose or react in ways that aren't possible at lower temperatures. The high degree of delamination, degradation of copper components, and general changes in the physical geometry and condition of the board may have altered the way the voltage is applied during the test. It was later determined after discussions with Laminate E supplier that the temperatures selected for Laminate E were too high. This was taken into consideration when selecting temperatures for the 1000-hour test.

It was theorized here that the influence of the PWB heterogeneous stack up vs. the laminate manufacturer's homogeneous stack up will have a significant influence on the change in robustness of the materials at elevated temperatures. This difference highlights the need and value of performing thermal endurance testing on a manufactured PWB. By doing so, the possible influence of different manufacturers and process sets are also taken into account.

Dielectric strength was calculated by dividing dielectric breakdown voltage by thickness tested. % retention was calculated using the following equation:

$$\%Retention = (1-((DS_{T0} - DS_{T552})/ DS_{T0}))*100$$

Where DS_{T0} = Dielectric Strength Time Zero and DS_{T552} = Dielectric Strength at 552 hours.

A plot was then created of % retention (x) vs. temperature (y) for each laminate which is presented in Figure 4a through 4e below. Data is fitted to a line or curve. In the data presented below, regression was used to determine the equation that fits the data best. % retention value desired (y) is substituted into the equation to find the corresponding temperature (x) to predict the highest temperature to be used in the 1,000-hour aging test. Data can be fit multiple ways, linear, polynomial, or logarithmic.

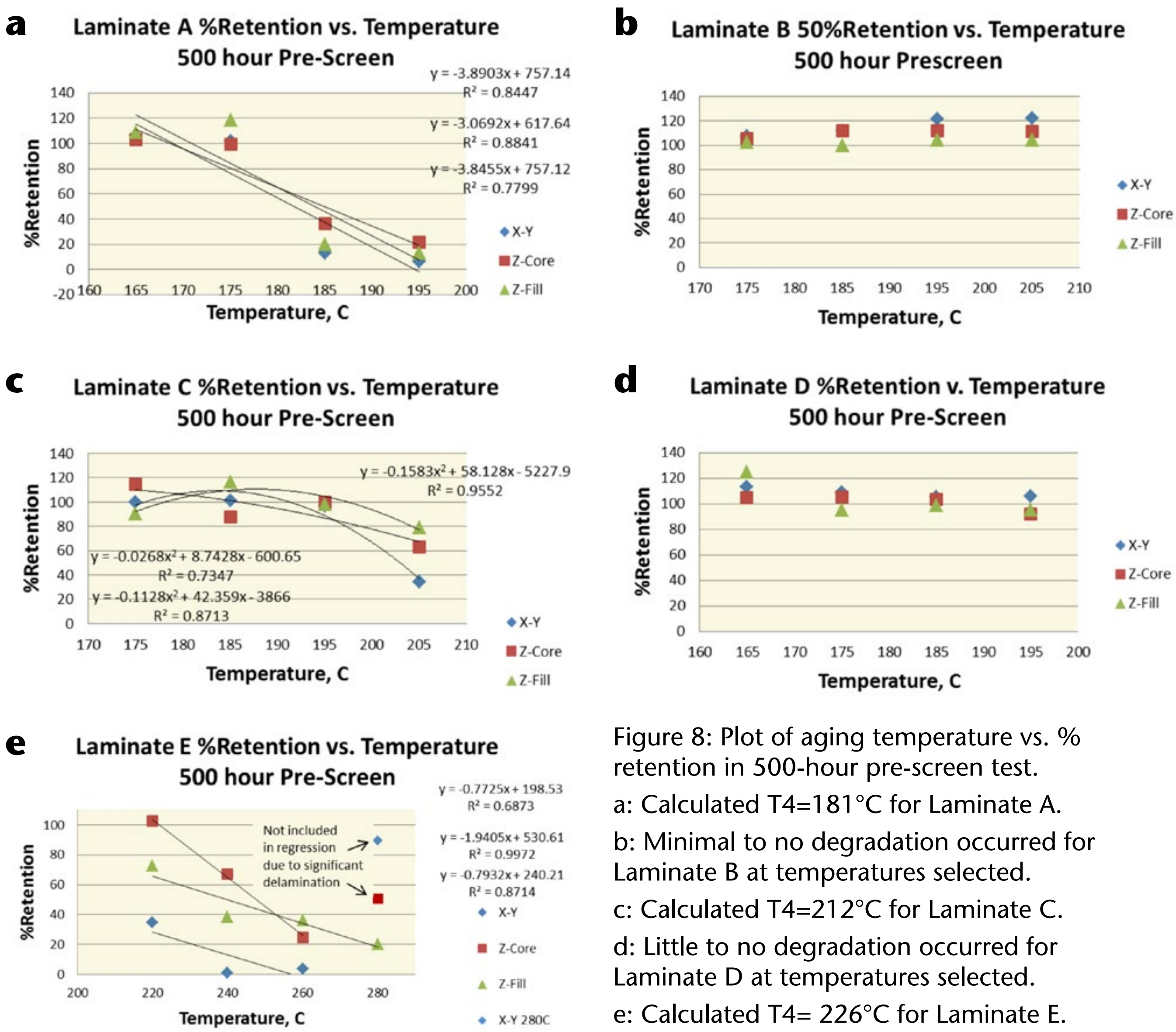

Figure 8: Plot of aging temperature vs. % retention in 500-hour pre-screen test.

a: Calculated T4=181°C for Laminate A.

b: Minimal to no degradation occurred for Laminate B at temperatures selected.

c: Calculated T4=212°C for Laminate C.

d: Little to no degradation occurred for Laminate D at temperatures selected.

e: Calculated T4= 226°C for Laminate E.

In this instance a linear and 2nd degree polynomial fits were used certain the data sets. The regression fit used for each sample's (X-Y, Z-Core, and Z-Fill % Regression vs. Temperature, °C are presented on each plot in that order. The 1,000 hours test data can be used in a similar fashion to validate this conclusion and to forecast the lowest temperature (5,000-hour failure) for the final long-term aging test. These plots are produced for each material independently. Solving the equation for $y_{50\%}$ yields a temperature that becomes the T4 (highest temperature) for the six-week test. Results for 50% degradation for each material are presented in Table 8.

Lack of degradation in dielectric strength for Laminates B and D prohibited calculation and extrapolation of 50% retention temperature. A test temperature 280°C was too high for Laminate E creating severe delamination. These data points were excluded from the regression analysis.

1000-Hour Testing

Pre-screen analysis data was used to help guide selection of aging temperatures. The 1,000-hour test used more aggressive temperatures as bounded by the pre-screen data and UL746A procedure. Data was first analyzed in a similar fashion to the pre-screen data to iden-

	Calculated 50% Retention X-Y	Calculated 50% Retention Z-Core	Calculated 50% Retention Z-Fill	Average 50% Retention X-Y, Z-Core, Z-Fill
Laminate A	175	184	184	181
Laminate B	Could not calculate %Retention due to lack of degradation (100% retention) of dielectric strength at temperatures selected.			
Laminate C	203	213	219	212
Laminate D	Could not calculate %Retention due to lack of degradation (100% retention) of dielectric strength at temperatures selected.			
Laminate E	191	248	239	226

Table 4: Calculated 50% Retention using Regression Analysis of 500-Hour Data. (Used for guidance in T4 temperature selection for 1000-hour test.)

tify potential outliers or worrisome behavior. Arrhenius plots were constructed for an initial prediction on behavior and performance for the 25,000-hour test.

Baseline dielectric breakdown voltage data was collected for each laminate. Dielectric strength was then calculated by dividing dielectric breakdown voltage by thickness tested. Dielectric breakdown voltage (V/mil) for each laminate is summarized in Table 5. A graphical representation of dielectric strength data is presented in Figure 9.

Table 6 provides a qualitative comparison between the five laminates. Laminates B and D have the overall high-

Baseline	X-Y Breakdown Strength (V/mil)	Z-Core Breakdown Strength (V/mil)	Z-Fill Breakdown Strength (V/mil)
Laminate A	1854	1983	1430
Std. Dev.	157	229	159
Laminate B	2040	3095	2167
Std. Dev.	449	189	293
Laminate C	2768	2029	1772
Std. Dev.	322	210	182
Laminate D	2289	2385	2252
Std. Dev.	247	223	317
Laminate E	1227	1574	1349
Std. Dev.	135	178	94

Table 5: Baseline—Average Breakdown Strength, V/mil.


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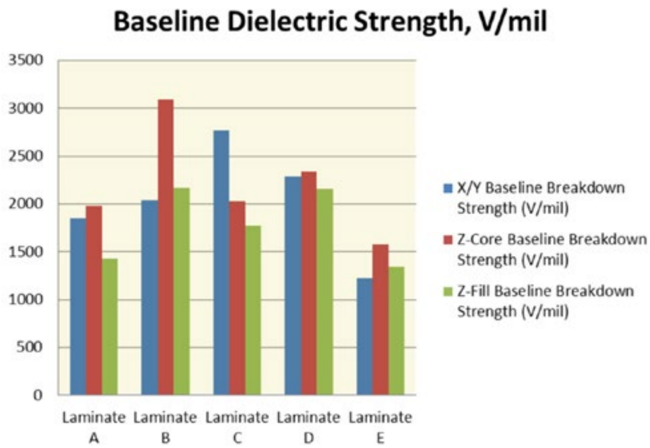


Figure 9: Graphical representation of baseline average breakdown strength, V/mil.

Breakdown Strength (V/mil)	X/Y	Z-Fill	Z-Core
Highest	Laminate C	Laminate B	Laminate B
	Laminate D	Laminate D	Laminate D
	Laminate B	Laminate C	Laminate C
	Laminate A	Laminate A	Laminate A
Lowest	Laminate E	Laminate E	Laminate E

Table 6: Comparative Analysis Baseline Average Breakdown Strength—Laminates.

Dielectric Strength	Laminate A	Laminate B	Laminate C	Laminate D	Laminate E
Highest	Z-Core	Z-Core	X-Y	Z-Core	Z-Core
	X-Y	Z-Fill	Z-Core	X-Y	Z-Fill
Lowest	Z-Fill	X-Y	Z-Fill	Z-Fill	X-Y

Table 7: Comparative Analysis Baseline Average Breakdown Strength—Board Location.

est dielectric breakdown strength before thermal aging while Laminate E has the lowest.

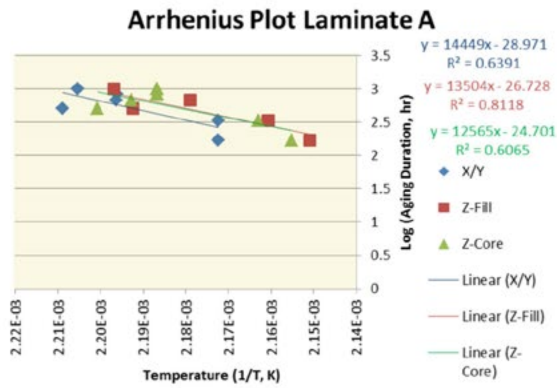
In general, the Z-Core was more robust with respect to dielectric breakdown. The Z-Fill (prepreg layer) was the less robust even though it thickness was almost twice that of the Z-Core. These results are summarized in Table 7.

The % retention was calculated using the same methodology that was used calculate T4 for the 1,000-hour test using the 500 hour pre-screening data. The 50% EOL point was calculated for each temperature. An Arrhenius plot was generated for each material plotting 1/T (K) on the X-axis vs. Log

Material	T1, °C	T2, °C	T3, °C	T4, °C
Laminate A	165	175	185	195
Laminate B	185	195	205	215
Laminate C	185	195	205	215
Laminate D	185	195	205	215
Laminate E	245	255	265*	275*
Laminate E Retest	195	205	215	225

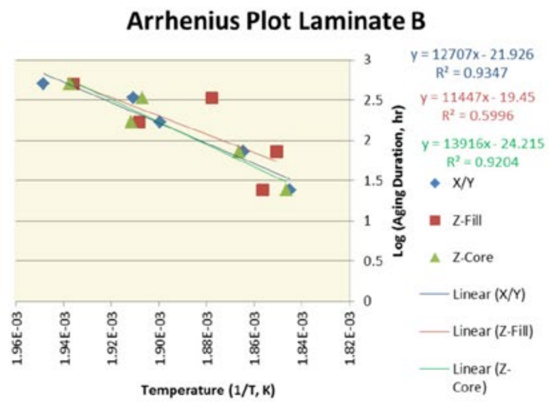
*Temperatures too high; 1,000 hour Test repeated for Laminate E

Table 8: Temperatures for 1,000-Hour Test Based on 500-Hour Test and Input from Laminate Suppliers.



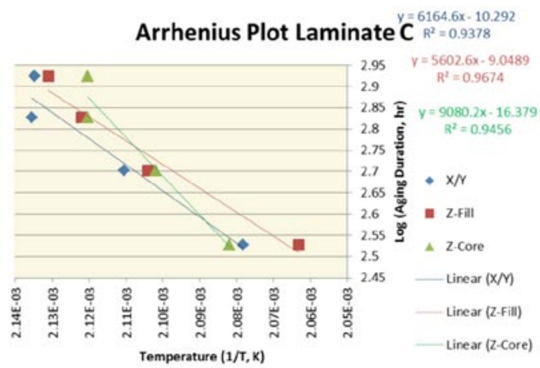
Laminate A	Failure hrs	X/Y Calculated 50% End of Life	Z-Fill Calculated 50% End of Life	Z-Core Calculate 50% End of Life	Temperature Used in 25,000 Hour Test
T5	1368	177	179	178	180
T4	3192	172	174	172	170
T3	6384	168	169	168	150
T2	12768	164	165	163	133
T1	25000	NA	NA	NA	105

Figure 10a: Arrhenius Plots 1/Temperature (K) vs Log (Aging Duration, hr.) for Laminate A; Calculated 50% EOL.



Laminate B	Failure hrs	X/Y Calculated 50% End of Life	Z-Fill Calculated 50% End of Life	Z-Core Calculate 50% End of Life	Temperature Used in 25,000 Hour Test
T5	1368	234	234	236	230
T4	3192	227	226	229	225
T3	6384	221	219	224	220
T2	12768	215	213	218	215
T1	25000	NA	NA	NA	105

Figure 10b: Arrhenius Plots 1/Temperature (K) vs Log (Aging Duration, hr.) for Laminate B; Calculated 50% EOL.

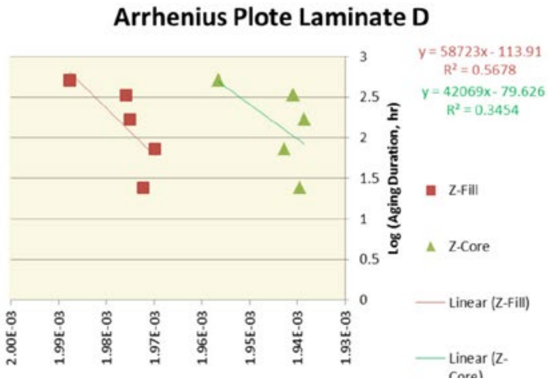


Laminate C	Failure hrs	X/Y Calculated 50% End of Life	Z-Fill Calculated 50% End of Life	Z-Core Calculate 50% End of Life	Temperature Used in 25,000 Hour Test
T5	1368	192	187	186	185
T4	3192	184	173	174	170
T3	6384	177	163	164	165
T2	12768	170	153	155	150
T1	25000	NA	NA	NA	105

Figure 10c: Arrhenius Plots 1/Temperature (K) vs Log (Aging Duration, hr.) for Laminate C; Calculated 50% EOL.

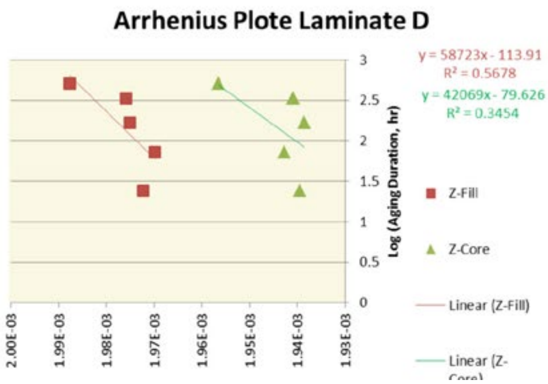
(Aging Duration [hours]) in the Y-axis. These are presented in Figure 10 for each laminate. In this instance a linear fit was used for the data sets.

Temperatures where 50% retention would be reached for 1368, 3192, 6384, and 12,768 hours were calculated using the linear equation generated for each laminate. For all laminates, 105°C was chosen for T1. Temperatures T2, T3,



Laminate D	Failure hrs	X/Y Calculated 50% End of Life	Z-Fill Calculated 50% End of Life	Z-Core Calculate 50% End of Life	Temperature Used in 25,000 Hour Test
T5	1368	NA	229	235	240
T4	3192	NA	227	233	232
T3	6384	NA	226	231	222
T2	12768	NA	225	229	195, 205, 215
T1	25000	NA	NA	NA	105

Figure 10d: Arrhenius Plots 1/Temperature (K) vs Log (Aging Duration, hr.) for Laminate D; Calculated 50% EOL.



Laminate D	Failure hrs	X/Y Calculated 50% End of Life	Z-Fill Calculated 50% End of Life	Z-Core Calculate 50% End of Life	Temperature Used in 25,000 Hour Test
T5	1368	NA	229	235	240
T4	3192	NA	227	233	232
T3	6384	NA	226	231	222
T2	12768	NA	225	229	195, 205, 215
T1	25000	NA	NA	NA	105

Figure 10e: Arrhenius Plots 1/Temperature (K) vs Log (Aging Duration, hr.) for Laminate E; Calculated 50% EOL.

T4, and T5 were selected using both the calculated (predicted) values as well as basic knowledge of material characteristics and behavior at higher operating temperatures.

Temperatures used in the long-term test are presented in Table 9. Temperature T2 was split into several groupings for laminates D and E to cover additional temperatures based on early results of the T4 and T5 tests.

Interconnect Stress Testing (IST) and Highly Accelerated Thermal Stress Testing (HATS)

In addition to thermal endurance testing, interconnect reliability was assessed using Interconnect Stress Testing (IST) and Highly Accelerated Thermal Stress (HATS).

IST measures changes in resistance of plated-through hole barrels and internal layer connections as holes are subjected to thermal cycling. Thermal cycling is produced by the application of a current through a specific coupon configuration. In this technique, the test coupon is resistance heated by passing DC current through the internal layer connection to the barrel for three minutes to bring the temperature of the copper to a designated temperature, in this test 150°C. Switching the current on and off creates thermal cycles between room temperature and the designated temperature within the sample. Thermal cycling induces cyclic fatigue strain in the plated-through hole barrels and internal layer interconnects and accelerates any latent defects. The number of cycles achieved permits quantitative assessments of the performance of the entire interconnect. A 10% Change in resistance measurement is considered a failure. Although there none of the samples developed a 10% change in resistance, Laminate B

Material	T1, ^{0}C	T2, ^{0}C	T3, ^{0}C	T4, ^{0}C	T5, ^{0}C
Laminate A	105	133	150	170	180
Laminate B	105	215	220	225	230
Laminate C	105	150	165	175	185
Laminate D	105	195, 205,215*	222	232	240
Laminate E	105	145, 160*	190	200	210

*T2 sample group was split to cover additional temperatures based on early results of the T4 and T5 tests.

Table 9: Temperatures used for Long-Term Test Based on 1,000-Hour Test Prediction and Input from Suppliers.

	1000 Cycles	Δ Power %	Δ Sense A %	Δ Sense B %
Laminate A	Pass	1.3 ± 0.5	1.0 ± 0.5	0.8 ± 0.4
Laminate B	Pass	1.7 ± 0.4	5.2 ± 2.7	1.3 ± 0.7
Laminate C	N/A	N/A	N/A	N/A
Laminate D	Pass	0.9 ± 0.5	0.7 ± 0.5	0.5 ± 0.4
Laminate E	Pass	1.5 ± 0.7	1.5 ± 0.8	1.0 ± 0.7

Table 10: IST Results.

performed worse than Laminates A, D, and E. Upon cross sectioning, defects were found in the plated-through hole. Laminate C was not tested.

The HATS method differs from IST in that it uses high volumes of hot and cold air to rapidly heat and cool the sample coupons between -55°C to +150°C. This rapid thermal transition makes HATS a more stressful test than IST. A change in resistance greater than 10% is considered a failure. Samples were subjected to 500, 1000, 1500, and 2000 cycles. Each cycle took 19 minutes. Results are presented below. Laminate B again performed the worse with failures starting as early as 150 cycles. A retest of a modified formulation of Laminate B, Laminate B*, did pass 1000 cycles however, Laminate E followed by D provided the best plated through hole reliability.

Long-Term Testing

Using the 1000 hour test data and +25,000-hour test data from T3, T4, and T5, an Arrhenius plot of 50% EOL (hours) vs. 1/Temperature (K) was generated for each laminate in Figure 11. Data is still being collected for T1 and T2

	500 Cycles	1,000 Cycles	1,500 Cycles	2,000 Cycles
Laminate A	Pass	Fail 3/9	Fail 1/1	N/A
Laminate B	Fail 9/9	N/A	N/A	N/A
Laminate B*	Pass	Pass	Fail 6/28	Fail 19/22
Laminate C	Pass	Pass	N/A	N/A
Laminate D	Pass	Pass	Pass	Fail 1/8
Laminate E	Pass	Pass	Pass	Fail 1/9

*Laminate B was retested using a modified formulation.

Table 11: HATS Results.

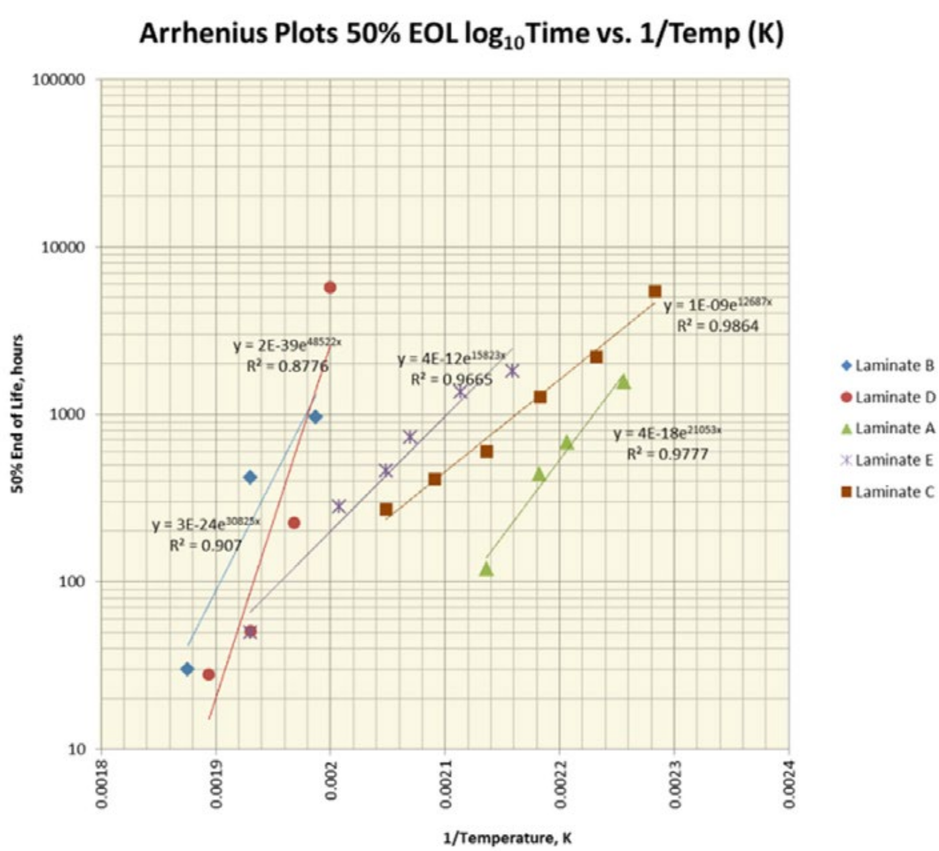


Figure 11: Arrhenius Plots of 50% log10 Time (hours) vs. 1/Temperature (K).

Laminate A	135°C
Laminate B	196°C
Laminate C	130°C
Laminate D	209°C
Laminate E	146°C

Table 12: Calculated Maximum Operating Temperatures for each Laminate Based on Data Collected to Date. (Results from T1 and T2 will be incorporated once testing is completed.)

tests which will conclude in the first quarter of 2016. Based on these Arrhenius plots, Laminate D appears to be the most robust laminate over time and at higher temperatures while Laminate A is the least robust laminate. Although laminate B appears to maintain its dielectric breakdown strength at high temperature, it was found to be mechanically unstable in HATS testing and had many plated-through hole failures before 500 cycles. A modified version of laminate B was retested in HATS and it passed 1000 cycles.

Based on these Arrhenius plots laminate D is the most robust laminate over time and at higher temperatures while laminate A is the least robust. While laminate B appears to maintain its dielectric breakdown strength at high temperature, it was mechanically unstable during initial HATS testing. Modified laminate B which is currently being tested in the two-year test, passed 1000 cycles HATS. Maximum operating temperature obtained by extrapolating each line to 100,000 hours is presented in the Table 12 below for each laminate.

Material	Overall Performance	Dielectric Breakdown Strength Retention	Estimated Usage in Comparison
Laminate A	Poor high temperature performance. Delamination at higher temperatures. Poor HATS* performance.	Quickly lost dielectric strength at moderately high temperatures.	Widely used
Laminate B	Second best high temperature performance. Poor performance in HATS* testing. HATS repeated on modified Laminate B - passed 1000 cycles. Some delamination at 230C.	Highest initial dielectric breakdown strength Z-Core. Second best for retention of dielectric strength at high temperature.	Limited Use – Application specific.
Laminate C	Second worst high temperature performance. Some warpage seen at all test temperatures. Passed 1000 cycles HATS*	Highest initial dielectric breakdown strength X/Y Declined in strength particularly at higher temperatures.	Limited Use – Application specific.
Laminate D	Best high temperature performance. Some warpage seen at all test temperatures. Passed 1000 cycles HATS*	Best overall initial dielectric breakdown strength. Best for retention of dielectric strength at high temperature.	Limited Use – Application specific.
Laminate E	Third best high temperature performance. Good mechanical integrity - no warpage or delamination observed. Passed 1500 cycles HATS*	Lowest initial dielectric strength. Declined slowly at higher temperatures but retain dielectric strength compared to Laminate A and E.	Specific Use (RF)

*HATS – Highly Accelerated Thermal Shock used to assess plated-through hole integrity

Table 13: Summary of Results.

Summary

The following conclusions are based on data from 1,000-hour test data and +25,000-hour test data (T3, T4, and T5) and are summarized in Table 13. Some materials that were base lined with a high dielectric strength did not maintain (hold) their advantage over other materials. Laminate E with the lowest initial dielectric strength was more capable of maintaining its performance over time and at higher temperatures than some of other laminates. Thermal aging tests showed not all materials are viable for rigorous applications where thermal excursions, high temperatures, high power, or high voltages are involved. Both laminate A and laminate B had delamination as time increased at temperature. Laminates C and D tended to warp as time increased with temperature. Laminates D, B, and E performed better in thermal aging tests especially at higher temperatures while laminate E and D performed the best in PTH reliability tests.

Some of the more commonly used materials types, such as Laminate A, are at high risk for failure over long periods of time at high temperatures, over many thermal cycles, or in high power and high voltage applications. Families of materials less commonly used are more appropriate for these applications and include B, C, D, and E laminate systems. The application demands for long-term reliability must be considered in PWB materials selection. **PCB**

Acknowledgments

DfR Solutions provided guidance on test methodology, background information, and also performed the testing and analytical services for the Phase 1, 500-hour pre-screen test.

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Eva McDermott is materials engineer at Amphenol Printed Circuit Board Technology.

Bob McGrath is manager of applications engineering at Amphenol Printed Circuit Board Technology.

Christine Harrington is director of operations at Amphenol Printed Circuit Board Technology.

Recent Highlights from PCB007

1 DuPont, Taconic and PFC Team-Up for High-Speed Flex


Glenn Oliver

At DesignCon, I sat down with three flex circuit specialists: Glenn Oliver of DuPont, Tom McCarthy of Taconic, and Steve Kelly of PFC Flexible Circuits. Our discussion covered a lot of territory, most notably the findings they described in the paper they were about to present later that day at DesignCon, and more.

2 Rex Rozario: The PCB Industry's True Renaissance Man

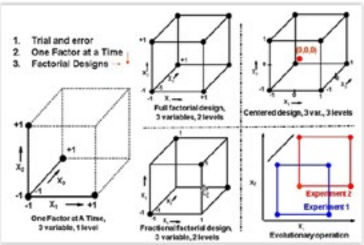

Rex Rozario

In this exclusive multi-part interview that was conducted recently, I-Connect007's Barry Matties will introduce you to all of the people that Rex Rozario is, and where he, his team, and Graphic PLC are headed to next.

3 Happy's Essential Skills: Problem Solving

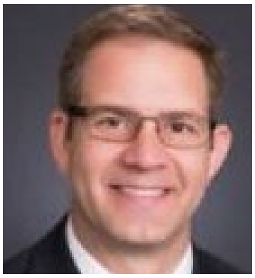
Related to TQC and a very important role of an engineer is solving problems. Using a problem-solving methodology is a job that all engineers will use sooner or later, but if you are in product or process engineering in manufacturing, it will be sooner! This was the situation that introduced me to printed circuit manufacturing.

4 Happy's Essential Skills: Design of Experiments



Design of experiments (DOE) is one of the most powerful and influential engineering tools for product yield improvements, new products or processes development, or for problem solving. As mentioned in my last column, process problems led me to a career in printed circuits, and quickly solving those problems led me to a bonus stock award and a great life.

5 Manufacturing Institutes can Boost the Nation



In his most recent State of the Union address, President Obama highlighted a remarkable trend of recent years: the turnaround in many corners of America's manufacturing sector. Nearly 900,000 new jobs have been created by U.S. manufacturers in the last six years.

6 Copper Via-Fill Technology in Development

The use of via-in-pad technology is increasing rapidly in today's PCB designs. The need for miniaturization, combined with the rapidly decreasing pitch of component footprints, drives printed circuit board designers here. Via-in-pad requires the vias to be filled, planarized and then over-plated with copper.

7 The Quiet Mainstreaming of HDI Manufacturing

Advances in technology continue to push the envelope of what's possible. And nowhere has the impact of those advances been felt more profoundly than in the evolution of the current class of mobile devices. Although design engineers have driven this evolution, the push to meet the associated manufacturing challenges has been responsible for a revolution in PCB manufacturing.

8 Weiner's World

Gene Weiner discusses PhiChem's upcoming open house event at its global HQ and R&D center in Shanghai during SEMICON China 2016, CPCA 2016 and productronica China 2016. He also focuses on the IPC Ambassador Council's plans to produce an executive forum in conjunction with IPC APEX EXPO 2017, IPC's association with NextFlex, and much more.

9 The Sum of All Parts: The Cost of Quality

Throughout the decades, irrespective of industry or sector, markets have thrived on competition. They have, however, also relied upon some semblance of unity within their respective competitors. Industries rely upon their individual member companies' ability to work together for the greater good.

10 Rex Rozario, Part 4: A 10,000-ft. view of his Business Ventures, the Industry, and Life

In our final installment, Rex describes the common thread woven through all of his successful business ventures and varied interests: confidence and the fortitude to follow his dreams until they are realized. Rex also takes a look back at the evolution of the global PCB industry, and explains his approach to profitability, which includes building (and rewarding) a successful team.

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Events

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For the SMTA Calendar of Events, click here.

For the iNEMI Calendar of Events, click here.

For the complete PCB007 Calendar of Events, click here.

2016 Annual Foundation Course (ICT)
April 11–14, 2016
Loughborough, England

Thailand PCB Expo 2016
April 19–22, 2016
Bangkok, Thailand

KPCA-KIEP Show 2016
April 26–28, 2016
KINTEX, Gyeonggi-do, S. Korea

JPCA Show 2016
June 1–3, 2016
Tokyo Big Sight
Tokyo, Japan

IPCA EXPO 2016
August 18–20, 2016
Delhi, India

IPC Fall Meetings
September 24–30, 2016
Rosemont, Illinois, USA

SMTA International 2016
September 25–29, 2016
Rosemont, Illinois, USA

electronicAsia
October 13–16, 2016
Hong Kong

TPCA Show 2016
October 26–28, 2016
Taipei Nangang Exhibition Center
Taipei, Taiwan

Electronica
November 8–11, 2016
Munich, Germany

International Printed Circuit & Apex South China Fair (HKPCA)
December 7–9, 2016
Shenzhen, China

PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

SALES: **ANGELA ALEXANDER**
(408) 489-8389; angela@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**
(916) 266-9160; tobey@iconnect007.com

EDITORIAL:
MANAGING EDITOR: **PATRICIA GOLDMAN**
(724) 299-8633; patty@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

MAGAZINE PRODUCTION CREW:
PRODUCTION MANAGER: **MIKE RADOGNA**
mike@iconnect007.com

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **MIKE RADOGNA, SHELLY STEIN, TOBEY MARSICOVETERE**

INNOVATIVE TECHNOLOGY: **BRYSON MATTIES**

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June—
Let's Talk Technical!
The impact of finer lines, features and tolerances