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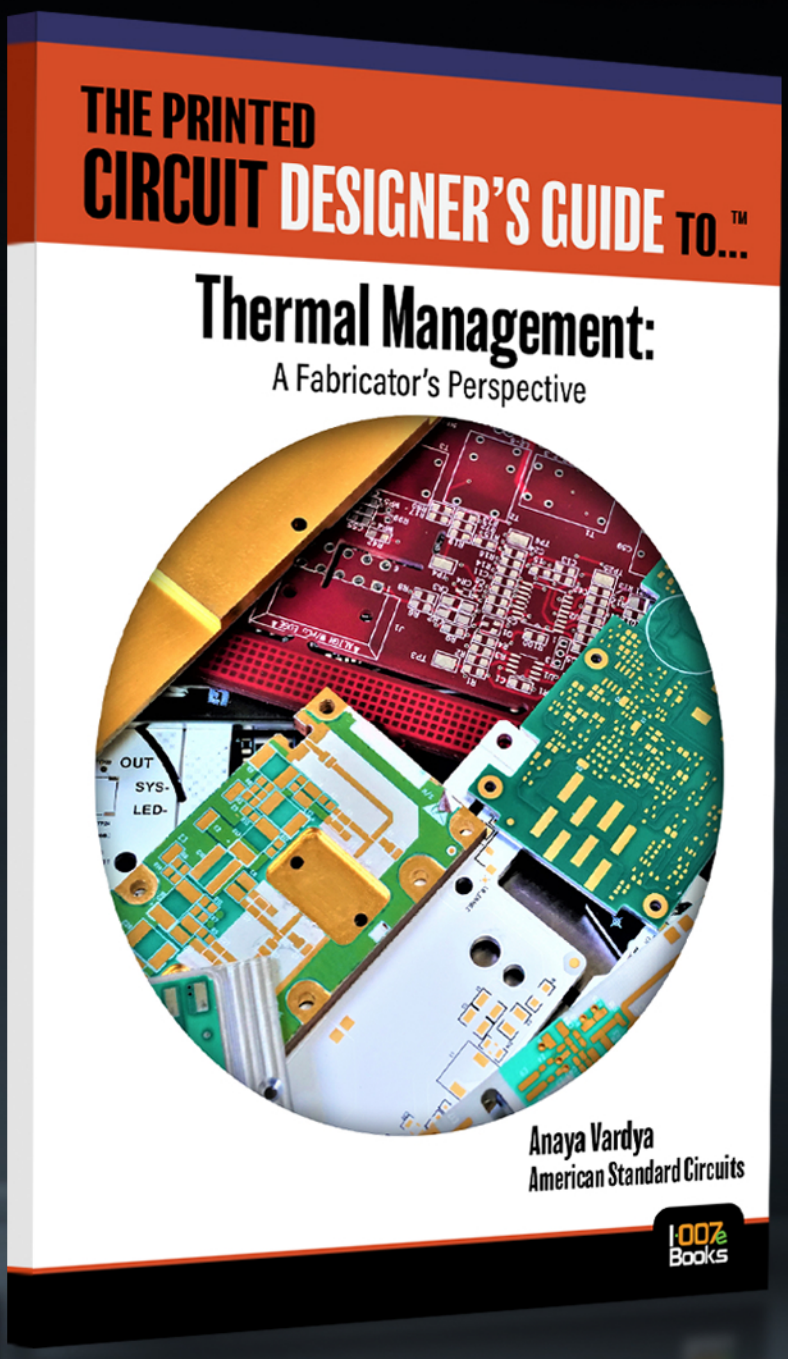

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Footprints and Library Management

Many designers count footprints among their most common headaches. This is a critical point in the design process; errors at this stage can wind up having ramifications far downstream. Something as simple as an incorrect pad size can lead to bad solder joints or components floating during reflow. So, this month, we asked our expert contributors to share their thoughts on proper footprint creation and CAD library management.


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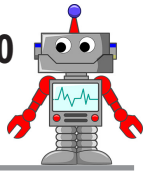

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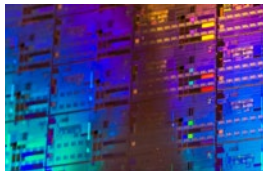

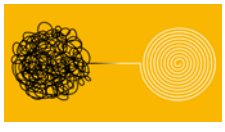

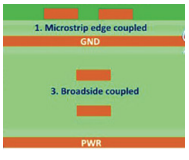

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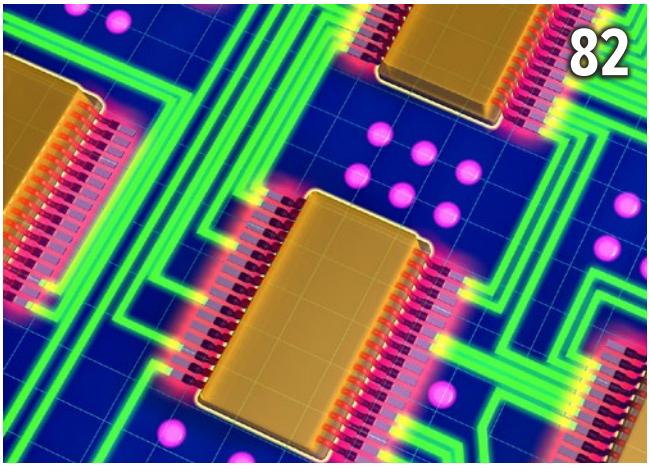
This Month in Flex

Managing and creating footprints for rigid boards can be a complex task, but flexible and rigid-flex circuits offer their own set of distinct issues. If you're new to flex design, all of this can seem intimidating. This month, we break down the ins and outs of footprint design, and what it means to flex designers.



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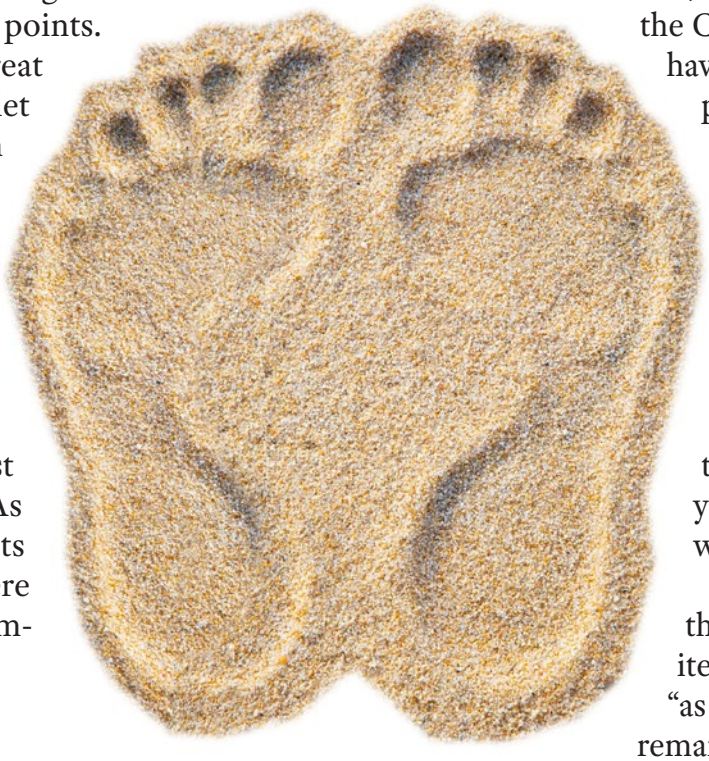
Footprints and Library Management

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

When we began planning this month's issue of *Design007 Magazine,* we looked at some of our recent surveys to get a feel for some of your pain points. These surveys are a great resource for us; they let us hear directly from the horse's mouth—in this case, the mouths of designers and design engineers.



In our last few surveys, many respondents mentioned footprints among their most common headaches. As always, the comments were illustrative. Here is a sample of the comments:

- Legacy issues with libraries, including traceability of footprints when used on PCBs across multiple projects over several years
- Wrong component footprints
- Incorrect footprint (smaller)
- Footprints are changed but not documented
- Errors on new footprints
- Incorrect footprints, as in just wrong (never been used previously, dimensionally incorrect)

I hear this sort of thing all the time from younger and veteran designers alike. As you can see, these issues all begin in the CAD library. If you don't have traceability for footprints that are used on a variety of PCBs over the years, you have a serious problem. When your designers are changing footprints and not documenting the changes, you're just asking for trouble. Who's running your CAD library anyway?

The last comment on the list above is my favorite! You can tell by the "as in just wrong" snide remark that the respondent is exasperated by the whole situation. It makes you wonder: Who signed off on these new footprints that were dimensionally incorrect? Does the company even have a sign-off process? If so, does it include a quarantine for new footprints? It seems a little too easy for bad data to wander into this respondent's CAD library. It sounds like this company needs to install a Ring doorbell on their library so they can see who's coming and going.

In addition to bad or non-existent library management processes, there is another culprit: footprint creation itself. It's not a fun

task by any means, and it's not creative. Most designers and engineers don't want to spend their time creating PCB footprints, so the job often goes to a young designer or junior design engineer, and they can't wait to get out of the library and back to the real fun in schematics, layout, and simulation.

This is a critical point in the design process; errors at this stage can wind up having ramifications far downstream. Something as simple as an incorrect pad size can lead to bad solder joints or components floating during reflow.

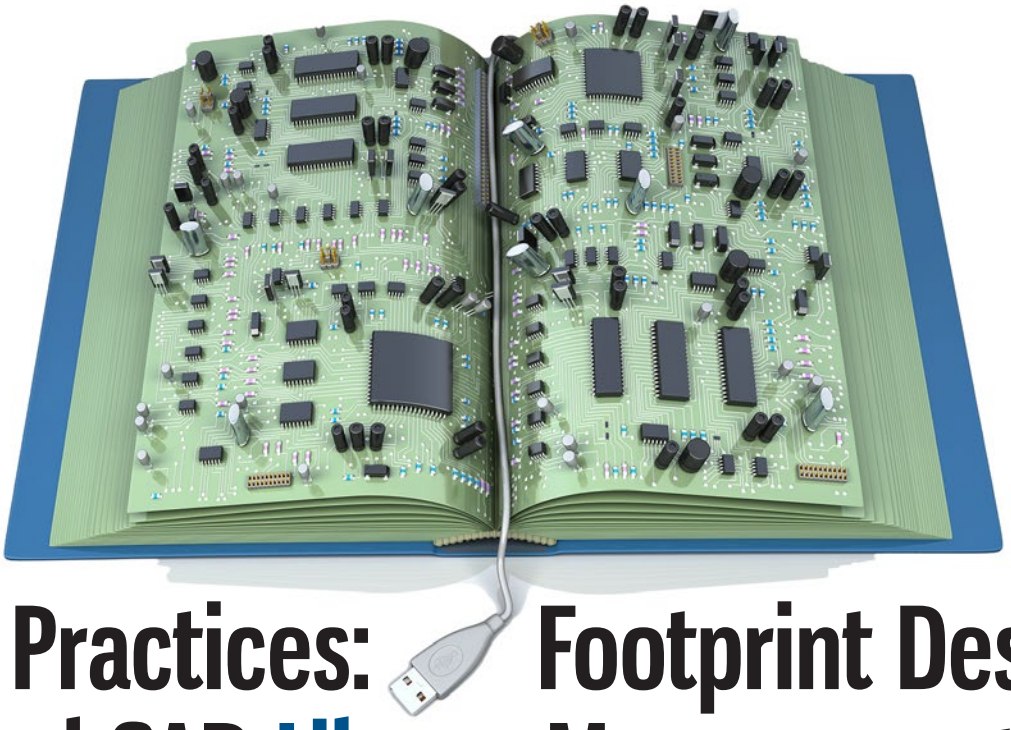
So, mistakes are made, and many of these are "organic" mistakes created in-house, not imported in from a third party. But from an optimist's viewpoint, this just makes these mistakes easier to correct.

So, we asked our expert contributors to share their thoughts on proper footprint creation and CAD library management. First, we have an interview with Altium's John Watson, who shares a few horror stories to illustrate why the CAD librarian may be the most important person in your company. We also have an interview with Tom Hausherr of PCB Libraries, who explains sound library management processes and how to avoid many of the common hurdles along the way. Then, Matt Walsh of Siemens Digital Industries Software discusses the role of the EDA company in footprint creation and library management. We have an article by EPTAC's Kelly Dack that's full of tips and tricks for better library management. Stephen V. Chavez of Rockwell Collins discusses the need for proper, documented communication when utilizing your CAD library. Geof Lipman of Octoparts explains the type of data their customers are asking for, and offers advice for designers who are facing footprint challenges.

It's a busy time. We're getting ready to cover the virtual IPC APEX EXPO 2021, March 8–12. DesignCon has been pushed back to August 16–18 in the hopes that it can be an in-person show. I don't know about you, but I'd kill to go to a trade show!

See you next month. **DESIGN007**

Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 20 years. He can be reached by clicking here.



Best Practices: Footprint Design and CAD Library Management

Feature Interview by the I-Connect007 Editorial Team

The I-Connect team spoke with Altium's John Watson about the hurdles surrounding footprints and footprint design. John talks about how being proactive and improving the CAD library can better QC processes and help protect against footprint difficulties.

Andy Shaughnessy: I'm here today with John Watson from Altium to discuss footprints, footprint design, and what can be done to achieve best practices. This came about because we recently conducted surveys asking for design problems. The results came mainly from designers, and around a quarter of them said footprint issues were a big problem.

John Watson: There's a real conflict in a lot of companies. They want to get their product to market. So, I think that the first issue that comes in with anything in a design is this conflict between the management schedule and the design schedule. If you're creating a new component, for example, number one is that component needs to be put into quarantine. It's not used in new designs. It needs to be put into quarantine and checked. There's such a rush to say, "We've got to get this done and get it out." And there's just too much going on in a design to catch things that are wrong like that.

Barry Matties: How long should it be in quarantine?

Watson: It stays in quarantine until a couple of processes are completed. Number one, there is a QC process that's done on that component, and that QC process is actually multi-level. There will be different steps involved. For example, if you have a new component, you bring that component in or that footprint in, and you verify that footprint to the datasheet. On this first level of QC, you want to set up your verification documents to that footprint. What are we going to be looking at? We're going to be comparing this footprint to the datasheet, we're going to be looking at IPC standards, whatever the standards are that you're going to

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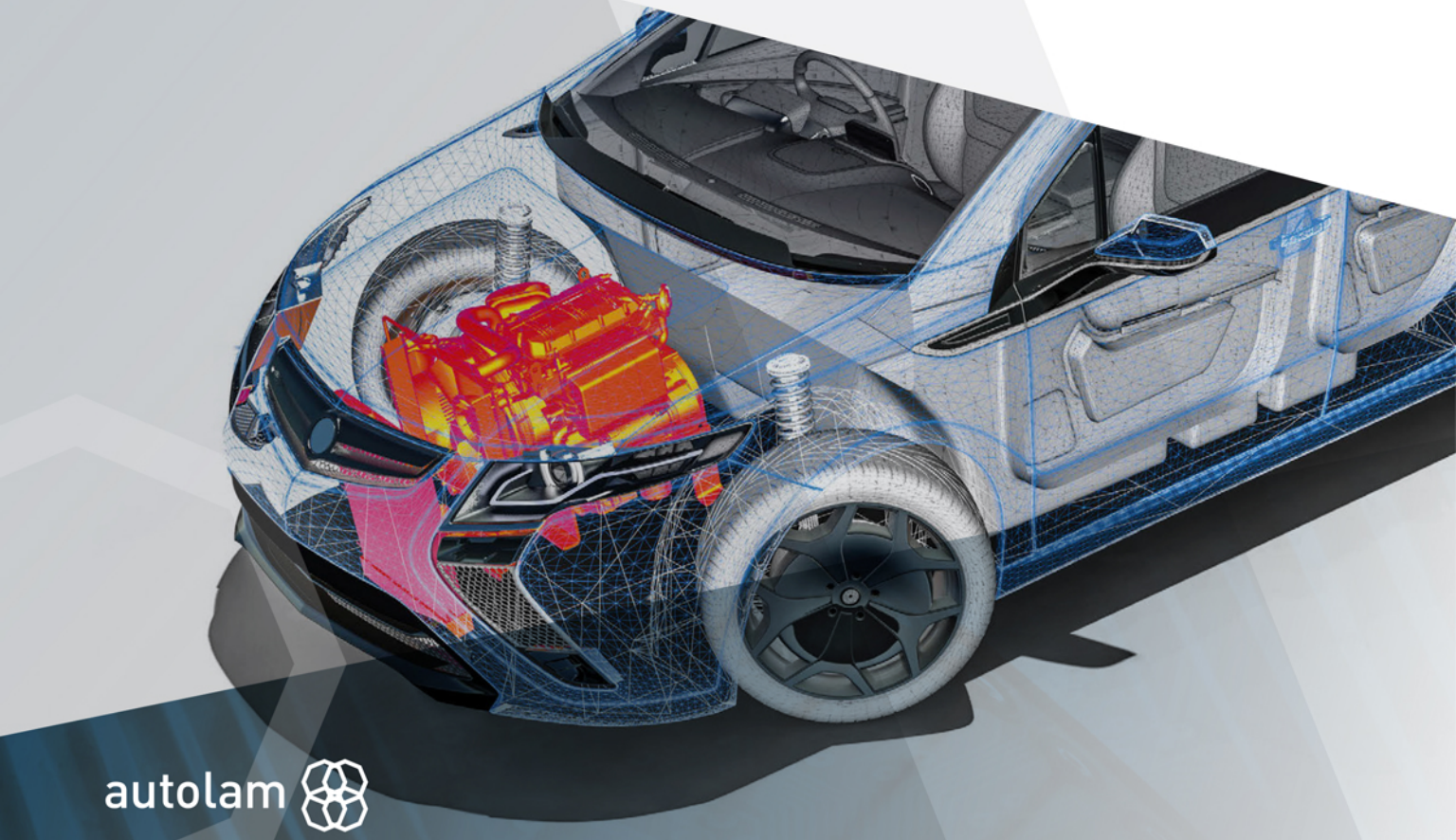

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be lining this footprint up with. That's going to be your first level of QC, but I've actually seen where there's a second level of QC that's done. Once that part has been verified to the datasheet, that part then goes into what's called the prototype status; what it does is that component is then put onto a PCB, kind of a live test.

When that board comes back with the component on it, you look at it under the scope to see if there are any issues with the soldering. It's like a real-world environment. Those are the two levels of QC. Number one, you compare it to the documentation, and then you have a real-world environment that you take it through. That step and those processes are what you go through. That way, you've actually had both sides of it: You have your side of it, and then also the assembler's side of it. I've found that a lot of times, believe it or not—I know it's a shocking comment I'm about to make—but datasheets have been known to be wrong. VPs have no understanding of what it takes to put a PCB design out—the steps, the checks that you have to do, all these different things. Often, that's lost in this whole process.

Matties: You mentioned time is a critical factor, but what about communication?

Watson: That's huge. Especially on the communication. Cool Hand Luke had it right in the movie: What we have here is a failure to communicate.

Dan Feinberg: John, along with what you were just saying, so many customers are saying the footprint is so wrong. I mean, they're emphasizing that. Do designers not realize that the footprints are so wrong or deemed to be so wrong? What's happening with the communication that they should be so surprised that it's wrong?

Watson: I would totally agree with that. There is a huge lack of communication. Especially with what I've seen for the past year, with

John Watson

everything that's been going on. Teams have been put into a lean mode, where you don't have as many people working on projects anymore. The very first rule of QC is not to check your own work. You never QC your own work. You always have another set of eyes look at it and then line it up with the verification documents. Too often now, that is being skipped over.

With that said, another issue that comes up a lot is that minimal pieces of that footprint are put in. If you took a footprint of a component, it's a cookie cutter; each footprint should have exactly the same thing in it. There should be the copper, solder paste, and the solder mask. There should then be the placement courtyard for that component, and there should be assembly information in that footprint. But because of time and manpower issues, shortcuts are taken, and every time you take a shortcut in a PCB design, it's absolutely adding risk to that design. It's something you just can't play around with when it comes to the PCB design.

When I joined Legrand, an engineer pulled me aside to his desk, and opened a drawer half-full of FR-4 boards. He said, "Those were our

failures." I was shocked, but once I learned more details, I found that over 30% of the boards were failing to get through fabrication because of problems with footprints or things like that. Now, we go back to cause and effect. "Okay, what's the cause?" It was our multiple libraries.

As a matter of fact, we had 1,123 libraries that we were working from in Legrand, and you cannot manage that many libraries. You just can't do it. You must have a singular library that can be managed. One Friday evening, after everybody went home, I deleted every single one of their libraries and their backups, and I purposely came in late on Monday morning. I knew what was about to go down.

As soon as I walked in, the whispers began: "He's here." Everybody was in the conference room, and I said, "As you probably have now realized, all your libraries are gone. We're starting over, and we're starting with a singular library which we can manage and control." I knew it was the only way you could fix the effect. The effect was bad boards, and we had to go back to the root cause.

Matties: One thing you did was to require everybody to stop doing their busy work and take that time. They're under time pressure, and a lot of companies may not be willing to take that time, I would think.

Watson: Yes, you've got to look at the whole picture, though. "Okay, we're losing time redesigning a board."

Matties: People don't stop to delete thousands of libraries because the thinking is they don't have the time to do it.

Watson: Exactly. Why is it that we have time to do something again, but we don't have the time to do it right the first time? We kind of compartmentalize our processes and we don't look at the big picture. We always talk about saving money. How much money was wasted in an engineering drawer of boards that were just wasted?

The other comment I wanted to make about libraries and footprints is you've got to have a single library, period, because that's what's managed and what's controlled. Now, there are changes that happen all the time on libraries. IPC, for example, just came out with 7351C. There were some real major changes they did with footprints from revision B. That's where they brought in rounding off the pads and different things like that. How do you make those changes in your library when you've got 1,000 libraries?

Shaughnessy: Nobody likes dealing with that stuff. How did they get to that point? How would you know where to look and which library to look in? I mean, I guess that's a whole other string of nomenclature or whatever. What a nightmare.

Watson: It was actually a living nightmare. Usually, every design that went through had its own library, and every designer had their own library, what they liked, what they preferred, and what their standards of a component were. I've been doing design for 20 years. When we first began, we used to take a resistor that consisted of a symbol and a footprint. We would lay down 0603 resistors of a certain value, we would just copy that same resistor, lay it down, change the value—just copy and paste. That's the way we did our schematics. Now, components have so much in them, which is phenomenal. This is really nice.

When you have a component, what are we looking at? We're looking at the symbol and at the footprint, but now we're also adding in parametric information in that component. Now we have sourcing, we have the manufacturers who will build that component for you who will be your vendors, who will sell it to you. Now we've even tied in component dynamic information: What are your vendors' quantities right now and what is their pricing?

What are their price breaks for that component? It's all inside that component now. It's not the old days anymore.

There's another great point I would like to make. There needs to be a signing off the footprint, and of the process. It's amazing that people's memory doesn't last more than six months when it comes to the mistakes that they make. They say, "I didn't approve that." But I reply, "Okay, well, there's your signature." And some of the solutions involved are going to be, first, biting a really difficult bullet for some people. That's because it needs changing, and people don't want to change.

Matties: When you talk about the root cause, how are they going to identify the root cause? What process would you use?

Watson: I would go through the five whys. That's how I get to the root cause of an issue. You look at the problem and ask why it happened. Then you go back one step, and ask why that happened? Let me give you an example. If my battery was dead in my car, my first question is, why is my battery dead? The answer to that question is my alternator was not charging my battery. Okay, why wasn't my alternator charging my battery? Because of a loose belt on the alternator. But why was there a loose belt on the alternator? Well, because I haven't replaced it for five years. So why haven't you replaced it for five years?

You keep walking back through the problem like that and you go back five whys and you start getting into the root cause. I go back to the fifth reason and find out I don't follow the maintenance schedule on my vehicle. So that's where you begin. There are different systems like that. And fishbone charts can help you figure out what your root causes are.

Matties: When you talk about market changes, how do they affect footprints?

Watson: The only effects of the market on the footprint would probably be big swings. I know when we went to solderless, the solderless manufacturing had a big impact on footprints and solderability. We saw how the market trending affected how the footprint was, but these are going to be common changes; maybe not common, but these will be changes in the market, and there will be changes that happen in footprints. Like I mentioned about IPC, they suggested, "Okay, now let's round off your corners." So, they put out the general direction to improve the footprint. IPC is really strong on that side of it, to watch what is affecting the footprint.

The other thing is just that the effect is more how those components are controlled and managed. How do you handle these changes? There are always going to be changes, so how you handle those changes is what's more important. How do you implement the changes? How do you go ahead and make a change on a footprint, for example? It goes back into the QC process. Make sure that the change was correct, and that it's done right. Then you take it back into the prototype stage, put a real component on that part, put it under a microscope, look at the solder joints and things like that, and understand what looks good; that's the way it should be.

Matties: What's a typical timeline for that process? Is that a day or a couple of weeks?

Watson: No, it could be within a day. It's very easy. It's a very good process.

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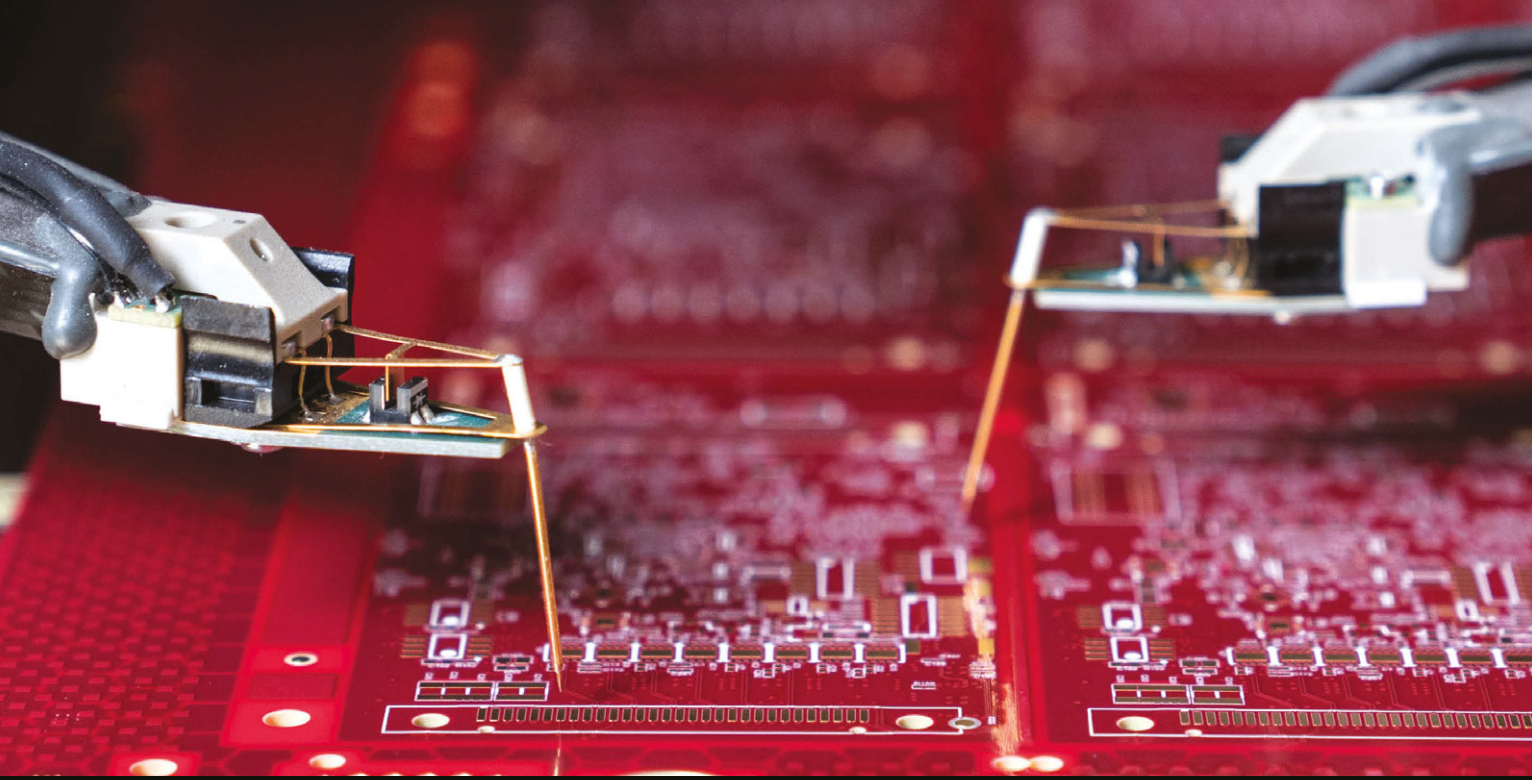

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Matties: What I'm looking at is keeping this QC and this quarantine process in mind, balanced with the time pressure.

Watson: That's true. You have to take the steps to be proactive in this process. You can't be reactive. That's probably what is really key; you have to not assume that that component is correct. You assume it's not correct until you prove differently, and that's probably the motto that should be plastered onto anybody who even touches a component. It is wrong until you prove it otherwise.

Nolan Johnson: John, that raises a good point as far as where these footprints are coming from in the first place. You have to assume it's wrong until you prove them right. So where do they come from in the first place?

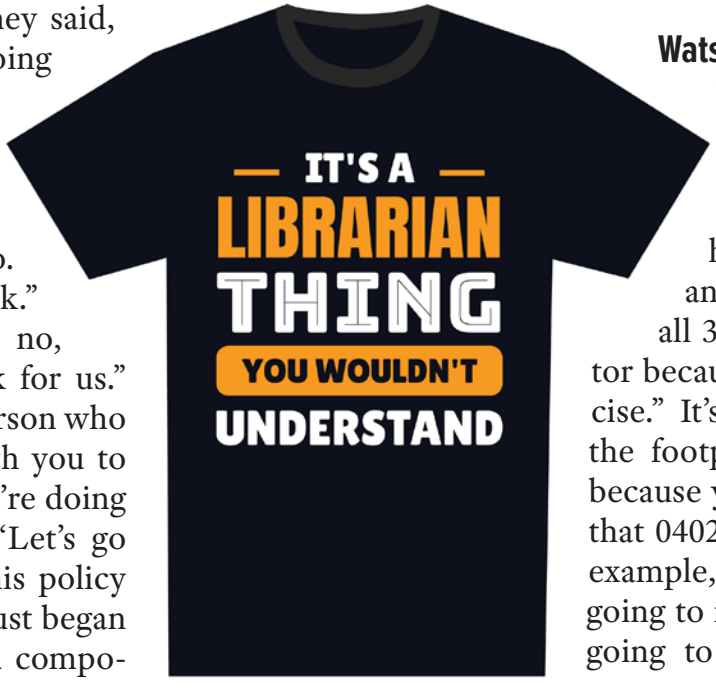
Watson: Probably one of the biggest mistakes I've seen in companies is that they give edit rights or permission to everybody to create libraries or create a component. They think it's more efficient for them to let everybody create components. This was actually a policy I saw done in a company when we were setting up their libraries and getting this started for them. I said, "So who's going to be your librarian?" They said, "Oh, no, we're not going to have a librarian. Everybody's going to be able to create components." I said, "I would suggest not to. That's not going to work." Their reply was, "No, no, no. It's going to work for us." I'm not the sort of person who goes nose to nose with you to prove to you what you're doing is wrong. So I said, "Let's go ahead and let's run this policy to see how it goes." I just began putting footprints and components up on the screen, and I said, "What do you see wrong here?" I mean, there would be stuff that was just so blatant, like rotated pads, everything.

That just brings up the complete process. First off, who's touching these components? Who has the permission? I would say that you give one individual or maybe a couple individuals that right. I label the librarian as the most important person on my team.

Johnson: One of the things that I'm hearing here is there's a lot of design team attention and effort being put into parts, components and footprints; into managing and verifying those, and making sure they're accurate. And yet, at the same time, if a CAD tool is like a word processor, the mark definitions are like fonts. Why do we have individual design teams out there building all their own fonts?

Watson: That's a really good point and a really good question. I don't understand exactly why they would do that, to be honest.

Shaughnessy: Would it be because they can't trust the datasheets? If you're assuming it's wrong, do you build a better mousetrap? Or do you work with what they gave you?



Watson: Yes, exactly. It's why I've actually seen libraries, when you go in there, they're like, "We're going to have an 0402 resistor, and we're going to put in all 32 heights of that resistor because we want to be precise." It's a lot less impact on the footprint of a component because you're going to perfect that 0402 resistor footprint, for example, and then you're just going to repeat that. You're just going to reuse that footprint.

You're going to start seeing that get cleaned up and then it just goes from there.

Johnson: John, on average in a new design, how much of the design time do you think typically is devoted to making footprints, verifying footprints, and getting that in order of the overall design?

Watson: I would say, number one, it's once you establish the sound processes of the process flow from the time that a component is needed to the time it's QC'd. I will say the initial QC, when it goes on a board, is probably about only about 10–15% of the process. Because what can happen is you then start cookie cutting. A component is going to have the same exact pieces to it, and then you can start cookie cutting it and then it's very minimal. I mean, if you have a very established process, it's very secure and also very low risk.

Johnson: Right. That makes sense; if you can get it to a well-defined process that is probably down to the 10–15% range. If you don't have good processing, you're probably up in the 30% range.

Watson: Exactly. And then you're going to see other effects of having bad components also. You know, when you have 30%, when you have no process, the chaos begins. I've used this analogy before but imagine if the mayor or government official would come forward and say, "Okay, no more rules. No one's going to be arrested for anything. You're on your own." What is the result of saying we have no processes, no rules, nothing? The result is chaos. That's what happens. There has to be the rules and the processes. Right now, I'm working with a couple of companies regarding their libraries and establishing their processes on a consulting basis, and I can tell you that one of them said, "We really don't know what we're doing." Okay, good. That's a good position to be in.

Matties: You've got to start with the truth, right?

Watson: Exactly. I told them that it's a great position to be in because now you're like clay; you just mold yourself into the processes that you want and put those processes in place and make sure that your components are correct and everything else. It has hit all of us at some point when I think about it. It's a nerve-wracking feeling when you've put out a PCB design, and you haven't checked footprints. You wait for that phone call from the assembly house to tell you, "Oh, by the way, we can't put your component on your board." And then you have to make the long walk into your manager's office to explain to them why you just wasted tens of thousands of dollars on a board that is now wasted and you're just going to turn them into coffee cup coasters.

It's a nerve-wracking feeling when you've put out a PCB design, and you haven't checked footprints.

You're actually talking about increasing the value of your team. When you become more efficient and run more efficiently, it's not just adding another PCB design to your team, it's also adding another team member, for example, or the value of a team member to the team. Because now you're running much more efficiently.

Matties: And the thing about $X = X_C - 1$ is you get to identify what your X is, and what we're saying is it doesn't have to be a grand slam because continuous improvement is an incremental endeavor. Reduce your spins by one, reduce your design time by a day, reduce your

rotation, etc. Really, to use $X = X_C - 1$, you have to incorporate your five whys.

Watson: Exactly. You have to get back to the root cause. What is not working? I mean, you've got to look at the backend. But there's another process here also, once you've taken a component through creating it, first defining who's going to do it, creating the process, taking it into quarantine, QCing that process, and getting it into prototype. Yes, it looks good from there. The one thing I've actually written about is that there's never a finish line in the library. It's not like you look at your library and say, "We're all done." There's always going to be that tailoring process at the very end where you now get more information from people. Everything filters back. It's one big circle.

Matties: In your experience, John, do you find the 80/20 rule to be true? That 80% of the issues come from the library?

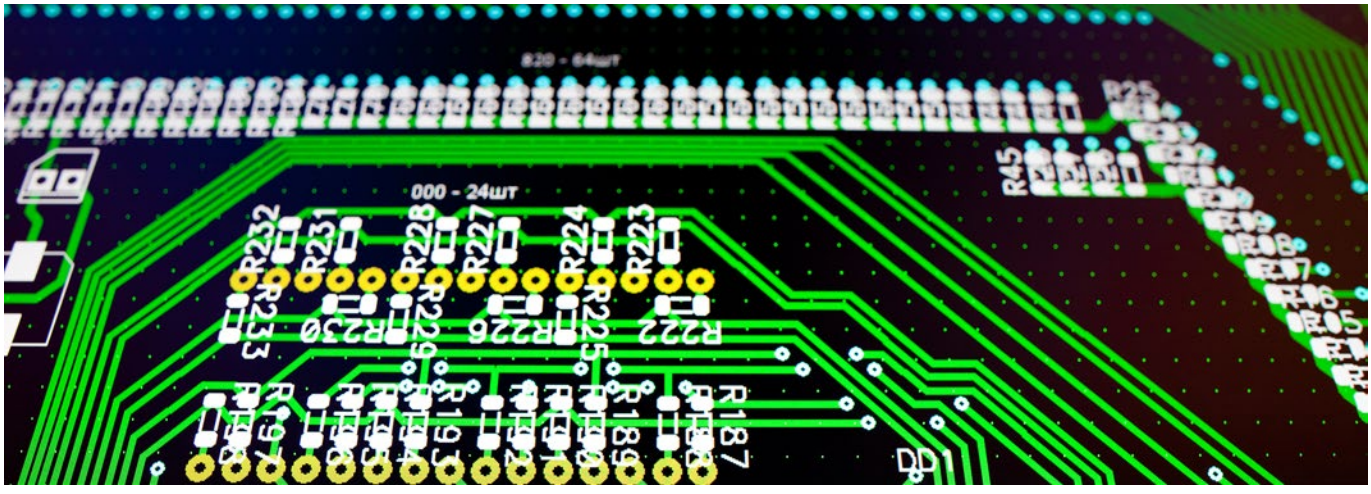
Watson: Yes, exactly. A lot of the issues that occur on the library are filtered back to the library. A lot of times when you have a library that you've been working with for a while you stop the tailoring process. You never look at your footprints and ask how you can improve this footprint. It's always going to be improved on. You're always going to say, "Yes, this can be improved on here by doing this or that." Maybe there are now recommendations coming in from IPC. There's always that polishing of that component. It's a complete process here; it's not straight or linear, it's circular.

Matties: How many points of data or information would one component have in the library? Is that user defined, or is there a standard that you would follow?

Watson: It could vary. When you're talking about parametric information on a component, that could be endless, actually. What will happen is you begin to categorize components into what would be categories and families. If you go into Digi-Key and pull up a component, it will show you this is your category, and this is your family of components. Those families of components will start having a generalized parameter of information. The families will have general parameters of information attached to each family. And that's kind of the way you would organize your library also.

There are two things about a library. Number one is you want to be able to find things quickly and find them accurately, and then number two is you want to structure your library in a way where it rolls with the company. A library is not a static item. It's a very, very dynamic item. It has to grow with your company.

Matties: Do you think that if a process is followed as you're describing, you'll never miss a footprint?



Watson: If you do, I would go back to the five whys.

Matties: But the odds of missing it have to be reduced.

Watson: Yes, it has now decreased considerably. What you're pulling out of this is that your "minus one" is risk. You're pulling risk out. You're not just creating a component and throwing it against the wall and hoping it sticks. That's the real concern with that. The other thing is that with some of the comments I've heard about components, for example, we get replies from people and they say, "It's close enough, the component, the model. It's pretty good." But is it correct?

Just because you're able to put a component in a spot on the board does not mean the footprint was correct. That just means you got lucky. There are situations where footprints have been wrong and after a time those problems show up. Let's say you had a wrong pad size that caused a short or less solder. After a time, now you're seeing problems introduced and issues that come up with that footprint. But a lot of times, the mentality is, "We got it. We made it."

Matties: But it's still a science and not an art, correct?

Watson: I would think so, yes.

Matties: Again, if you follow the process.

Watson: If you follow the process, yes.

Happy Holden: I was involved in design with a company that had been doing it for 50 or 60 years like I was, and nobody was a librarian out of 300 or 400 PC designers, and that's because they learned the hard way that components are so important and that components have a life. It was better to have corporate engineering create all the libraries worldwide, including the expensive models and things like that, but also to be tied in very tightly with corporate quality and field service. Once a component was approved, and the model and the footprint were generated, it was tied to the purchase of that part and put away in a catalog so that design engineers could select from the catalog, and specifically in that catalog was the cost and the field service quality. Bad parts that were coming back from the field, not due to manufacturing errors, but the component itself were highlighted in those lists to stay away from these "known bad actors."

Watson: Right. As I said, the librarian is the most important person on my team.

Matties: John, this has been a very informative conversation. Any final thoughts to this conversation?

Watson: I would say that whenever there's a problem or issue like wrong footprints, you're going to have to take a step back, take a deep breath, look at it in a more objective way and ask yourself this one question: What went wrong and why? What happened here? Why did it happen? Be honest with yourself. I mean, people should be able to say, "Yes, the buck stops with me. I made a mistake." And then deal with those mistakes and issues and move forward.

And watch out with connectors. Your biggest problem will be with connectors, because the datasheet does not tell you how the pin numberings are, whether they are one down the row or they're alternating, and that actually will cause major problems when you get into fabrication.

Shaughnessy: This was really good. Thanks, John.

Watson: Guys, thank you very much. DESIGN007

Developing Panel Level Semiconductor Packaging

Designers Notebook
by Vern Solberg, CONSULTANT

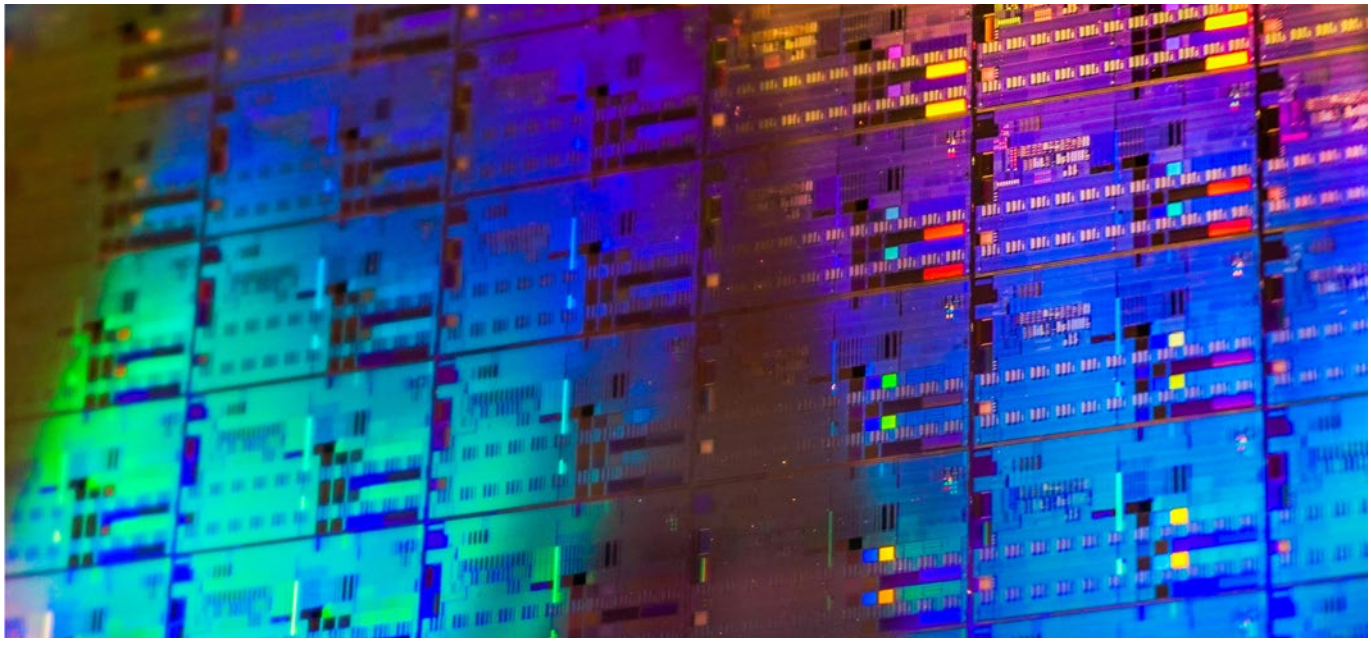
Semiconductor packaging has traditionally utilized a narrow strip of organic copper-clad organic-based laminate and wire-bond processing for the single-die BGA. Companies furnishing devices for high-volume markets are now implementing very fine-pitch alloy bumped flip-chip package technologies that enable face-down interface. The terminal size and pitch are often, however, far too small for conventional organic circuit board fabrication capability. To better accommodate die-to-substrate interface, several companies are successfully adopting wafer-level and panel-level package technologies.

Wafer Level Packaging

Silicon materials are commonly furnished in a 200-300 mm diameter wafer format sized to be compliant with the existing semiconductor fabrication infrastructure. Most commercial semiconductor manufacturers utilize these thin silicon wafers to provide a stable base for integrated circuit processing, but the silicon-based material has also proven to be an excellent choice for wafer-level packaging because it perfectly matches the CTE of the silicon die element(s) that will be mounted onto its surface.

Fabrication of the fan-out or fan-in/fan-out interposer is commonly performed within the semiconductor foundry environment. Die elements are arranged on the wafer's surface in a row and column format, with the active surface facing up for wire-bond interconnect or face-down when furnished with alloy bump terminals.

The processes for via-hole ablation and metallization in the silicon material are very different from the basic semiconductor man-



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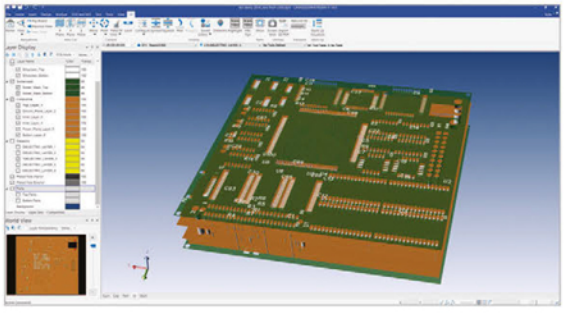

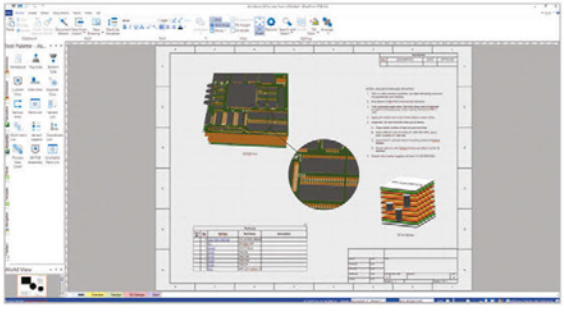

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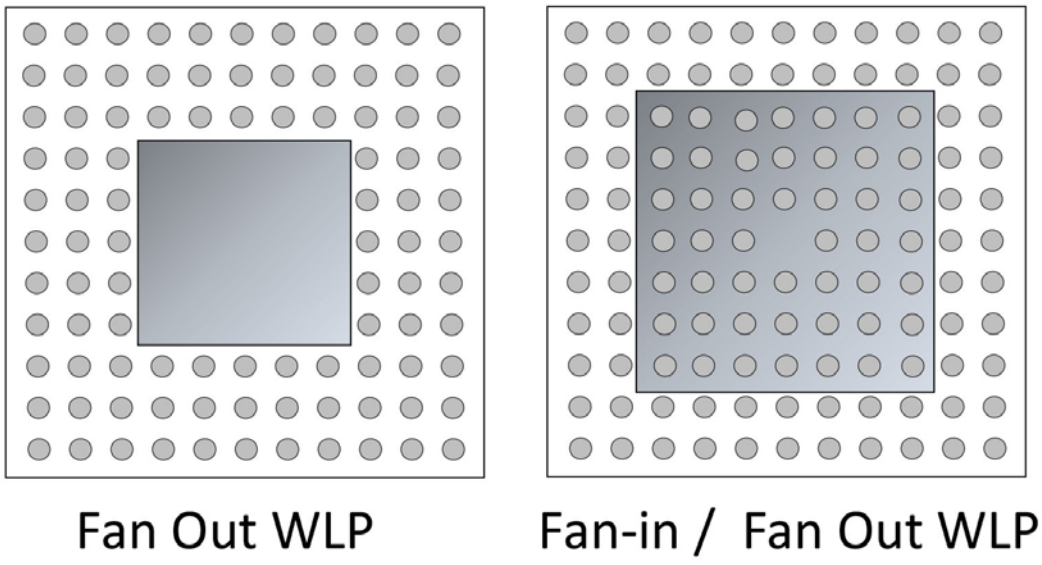

Figure 1: Comparing the fan-out to the fan-in/fan-out wafer-level package.

ufacturing processes. Metal deposition processes developed for the silicon-based interposer enable the redistribution of the very closely spaced terminals on the die element's perimeter to a uniform and wider spaced array pattern that will enable a more efficient package substrate interface (Figure 1).

Although the silicon wafer packaging process has proven robust and reliable, the cost associated with silicon-based interposer fabrication has been a primary detractor, and because the wafers are round, there is a great deal of surface area at the wafer perimeter that cannot be populated. In the effort to trim overall packaging expense several alternative panel-level packaging methodologies have emerged.

Panel Level Packaging

Both independently and through consortia of academia and industry, several viable solutions have evolved that provide the same fan-out and fan-in/fan-out interface capability. Panel-level packaging will continue to use silicon as a base, but alternative lower cost organic epoxy-glass laminate and panel formatted glass are viable options.

Silicon and Glass Panel Development

To gain better utilization of the silicon base, some companies have moved away from the traditional wafer level format to a square silicon or glass panel format where the individual die elements can be arranged in the same row and column format with minimal base material waste.

Silicon Interposer Base Material

To maximize assembly efficiency the base material can be furnished as 300 mm and 500 mm square panels, but some companies looking to maximize package assembly efficiencies are fabricating panels as large as 600 mm square.

Silicon-based interposer fabrication requires a rather specialized and complex sequence of processes that begin with via-hole formation. Although laser ablation can be adopted for forming the micro-via holes, the process most commonly employed for volume applications uses a deep reactive-ion etching (DRIE) process (often referred to as the "Bosch" process). This methodology can provide very small hole diameters that range between 5–20 microns. In preparation for conductor forming and via filling, a seed layer of copper or tungsten is applied to enable electroplating the additional copper required to complete the via-fill operation. Further pattern imaging and plating pro-

cesses are engaged to provide interconnect features on the outer surfaces of the silicon substrate.

Glass Interposer Base Material

Significantly less costly than silicon, glass panels are being supplied by several companies specializing in manufacturing a physically durable glass with properties suitable for fan-out and/or fan-in package applications. The nominal CTE of the metalized glass panel is also a very close match to the silicon die (3 ppm/°C).

Glass is available in panel thicknesses that range from 50 µm to ≥700 µm, and the process differs significantly from silicon wafers because it will not require back grinding and polishing prior to via ablation and plating operations. The via-hole forming processes for glass include laser and electrostatic discharge as well as mechanical drilling using micro-sand-blasting. Metallization on glass begins with a vapor deposition (PVD) process of copper or silver ink deposition to furnish the base for filling vias and interconnect circuitry.

High Tg, Low CTE Organic Base Material

One of the more promising materials for the high-density organic package substrate applications is promoted as an ultra-low CTE organic glass reinforced bismaleimide triazine (BT) based laminate.

While many organic dielectric materials have traditionally proven suitable for a broad range of wire-bond package applications, several leading suppliers have developed a more advanced laminate material that closely matches the very low thermal coefficient of expansion (CTE) of the silicon die element, as well as meeting the fine-line interconnect challenge for new generations of high I/O face-down mounted semiconductors. The manufacturer promises that the laminate will provide a more stable platform for mounting silicon-based semiconductor elements.

The design guidelines furnished in Table 1 relate to copper alloy via filling and conductor formation for the three base material candidates for panel-level semiconductor packaging. The geometries furnished were developed from research by the author and consensus

Attribute	Silicon Base Material	Glass Base Material	CTE Matching Organic Material
Substrate Panel Thickness	200µm to 3mm (~.008" to .120")	200µm to 3mm (~.008" to .120")	100 to 800µm (~.004" to .032")
µVia Hole Diameter	5µm to 20µm (~0002 to.0008")	10µm to 30µm (~.0004 to.0012")	10µm min. (~.0004")
µVia Land Diameter	15 to 25µm (~.0006 to .001")	25 to 50µm (~.001 to .002")	20µm min. (~.0008")
µVia Hole Pitch	30 to 50µm (~.0012 to .002")	50 to 100µm (~.002 to .004")	40µm min. (~.0016")
Base Core Line/Spaces	2µm min. (~ .00008")	1µm to 5µm (~ .00004-.0002")	3µm min. (~ .00012")
Build-up Lines/Spaces	2µm min. (~ .00008")	1µm to 5µm (~ .00004-.0002")	3µm min. (~ .00012")

Table 1: Panel-level package design guide.

among several colleagues involved in the technology.

The data shown may not reflect the capability of all suppliers in their respective categories, but supplier companies will generally furnish the designer with alternative design guidance related to their material sets and specific process capabilities. The supplier-developed interposer design guidelines will generally reflect factors derived from their experience, ensuring that they will likely furnish a reliable product with a high degree of quality and process yield.

Key Planning Issues for Panel Level Packaging

Assembly process methodologies will vary a great deal. Issues that will need to be resolved prior to beginning the development process include:

- Availability of semiconductors prepared for face-down mounting
- Establishing reliable sources for semiconductor elements
- Specifying physical and environmental operating conditions
- Defining package design constraints and process protocols
- Stipulating electrical test method and post assembly inspection criteria

Semiconductor packaging methodology will continue to evolve, and market analysts project a steady growth in semiconductor package applications.

There is presently a global effort by members of SEMI (Semiconductor Equipment and Materials International) to develop standards for manufacturing panel-level packaging. The standards have already established panel size variations and thickness, as well as surface topography and panel warpage limitations.

IPC is currently in the formation stage to develop a standard guidance document for an organic-based panel format that is defined as "a wiring structure produced with a printed circuit board fabrication process that provides the final electrical interface between microelectronic devices and the underlying circuit structure." Printed circuit manufacturing process characteristics include the use of square or rectangular panels with build-up circuit layers applied to both sides of the base using organic dielectric materials. **DESIGN007**

Vern Solberg is an independent technical consultant specializing in SMT and microelectronics design and manufacturing technology. To read past columns or contact Solberg, click here.

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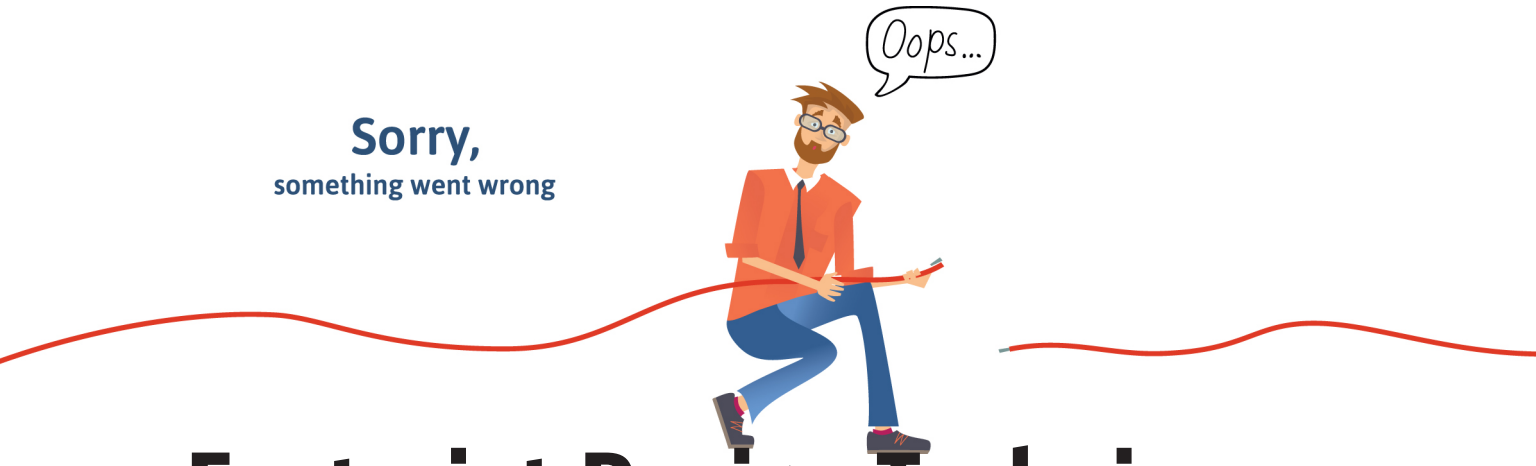

Footprint Design Techniques: Don't Trust Datasheets

Feature Interview by the I-Connect007 Editorial Team

The I-Connect007 Editorial Team recently spoke with PCB Libraries CEO Tom Hausherr, who has spent much of his professional life dialing in the processes related to footprints and CAD libraries. We asked him to run down some of the more common challenges that he sees, as well as some solutions and workarounds. One point emerged several times during our chat: Don't trust datasheets.

Andy Shaughnessy: Tom, our readers tell us in surveys that footprints are a huge problem for them, and a lot of it seems to come from bad CAD library management. What are some of the more common challenges you see with footprints?

Tom Hausherr: The number one mistake today is the polarity marking on diodes, where the EE engineer puts Pin 1 on the cathode and puts Pin 2 on the anode. Then the designer does the opposite. They populate the boards and when they plug them in, something smokes or doesn't work properly.

Barry Matties: That is a pretty common problem that we hear about. Why isn't more care given to that if it's such a common problem, Tom?

Hausherr: I try to label the pins of the diode C and A on both the schematic symbol and PCB footprint so that you cannot possibly get it wrong—C for cathode, A for anode. But then again, when you're dealing with LEDs, many manufacturers put the polarity on the anode side of the component package. Electrically, the anode is the positive pin, and the cathode is the negative pin. But the marking indicator is on the cathode for diodes. To eliminate error rate, double check all diode and LED connections.

Matties: Right. We hear the same, not just with the LEDs, but with connectors, too, being a big issue with pin orientation.

Hausherr: A lot of the connector manufacturers do not provide any pin assignments on their datasheets. I run into this all the time. You should coordinate connector pin assignments with the EE engineer's schematic. Also,

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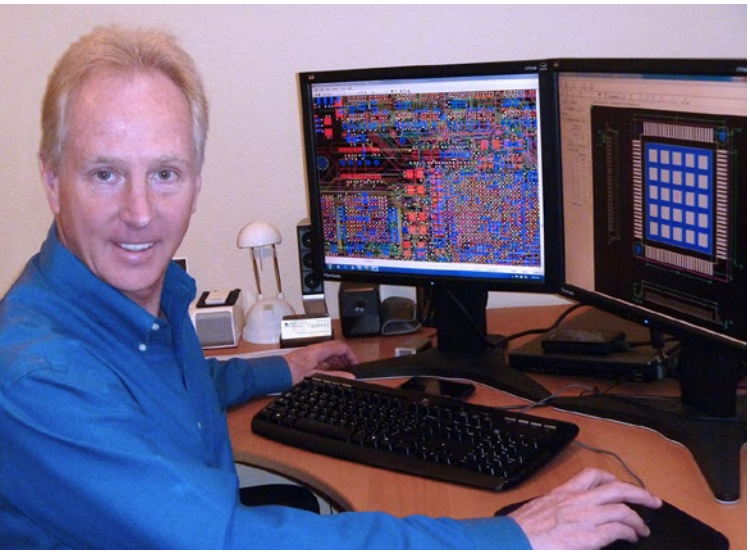


Tom Hausherr

some of the connector manufacturers give you the location of Pin 1 but not Pin 2. I wish all component manufacturers knew what information to provide in their datasheets to make our job easier.

The number one feature that's missing in most component datasheets is the manufacturer-recommended footprint pattern almost never provides dimensional data from the hole or surface mount pattern to the edge of the connector body. This is a necessary piece of missing information that causes errors. This can be checked when the 3D model is inserted into the footprint pattern to ensure the silkscreen and assembly outline matches the package boundary.

Another thing about the connectors: You must use their manufacturer-recommended pattern. There's no IPC calculator or magic formula for calculating a complex connector pattern. Many of the connectors today are a mixture of plated-through mounting holes and slots, non-plated alignment holes, surface mount pads, and every type of combination. So, you must use the manufacturer pattern.

I just did a library part last week, a 15-pin D-Sub miniature connector. We built it per the manufacturer pattern and exactly per their dimensions, but there was a datasheet typo. The only thing that saved us from duplicating the error in the datasheet was the 3D model. The mounting holes lined up with the 3D model, but all the pins were in the wrong location.

I looked at it, measured everything, and everything was correct by the datasheet. And then I found out that the manufacturer had one dimension wrong. They dimensioned the mounting hole to Pin 1 but the value was to Pin 5. In other words, there was an inherent typographical error in the manufacturer's datasheet. So that's another thing to be very careful about. Double check with the 3D model.

Shaughnessy: Datasheets have errors after all.

Hausherr: Right! Hard to believe. Let me give you an example. I did a design a couple of years ago with a large 200-pin LGA. I sent the design Gerber data to a fabricator. Before they built the boards, they ran a Valor VPL check. And there was nothing wrong with the pad sizes or the land pattern, but they did catch an error in the pin assignment. The component manufacturer did not indicate "top or bottom" view, so I guessed. The alphanumeric pin assignments were all incorrect.

When they ran the Valor VPL check they discovered that all the pin numbers were backward. Now, let's say that they didn't run the Valor VPL check. They would have manufactured and assembled the boards, and everything would have assembled perfectly. But when the EE engineer turned on power, none of the PCB functions would have worked.

In my case, all the terminal leads were fine, but it was the pin assignment that was totally backward. The Valor VPL check caught that mistake. Unfortunately, I had to redesign the board at my expense. But that one little catch saved thousands of dollars in fabrication, assembly, and components. The board would have been declared a door stop.

Shaughnessy: What is the cause of that in the first place?

Hausherr: When the manufacturer's datasheet shows the top view and the bottom view, they must clearly define which is the top view and which is the bottom view, and what you are looking at. Often, they mark the pin assignments, and some manufacturers are kind of lax at labeling all this documentation. Also, the LGA package pin assignments are sometimes intentionally mirrored.

Nowadays, the component manufacturers are giving acceptable recommended footprint land patterns. They call them the "Recommended Footprint Pattern," just the "Recommended Pattern," or "Solder Pattern." PCB designers or CAD managers are split in two. I would say that half of the global PCB industry prefers the manufacturer pattern, the other half of the industry prefers to use the IPC calculator pattern, and there are some who use a combination of both. But land pattern calculators are software code that are not flexible enough for non-standard packages. As we move to the future, standard packages are being replaced with complex non-standard packages to intentionally eliminate competitors from producing lower cost alternatives. These new non-standard packages require manufacturer-recommended patterns.

We have 100,000 users of our software program worldwide and we run into this every day. We add the manufacturer-recommended pattern data in all our CAD library data files, but those can be turned off and revert to the IPC pattern. We have several millions of manufacturer part numbers on our cloud database. For instance, Boeing would download a bunch of parts and then say, "Why do you put the manufacturer's pattern in here?" I said, "Well, it's easier for us to do that because all you have to do is uncheck a box and then it defaults to the IPC pattern." And they said, "Yeah, but we downloaded the whole bill of material with the parts and now we've got to go and uncheck all these boxes and resave every part to get the IPC pattern."

It's really hard to please everybody. You go after the manufacturer's pattern, and a lot of times the manufacturer's pattern is superior to the IPC specifications. I've downloaded millions of datasheets and checked everything out, checking against both different mathematical models and the manufacturer's recommendation. Then, it's knowing which pattern is best after looking at millions of land patterns and millions of footprints. However, we've been creating land pattern calculators for 20 years and no one has ever complained about creating a bad footprint.

Alternatively, we've never heard of anyone complaining about using a manufacturer's recommended pattern, as long as the terminal leads are on the pad. I'm sure that there are typos in datasheets, so the PCB designer must ensure that the terminal lead is on the pad and our software calculators clearly indicate both the terminal lead location in respect to the pad location.

And it's difficult. If you have a QFN bottom terminal component with a thermal tab, some manufacturers provide recommended stencil data pattern. You have to know stencil data pattern rules. You've got to have a 0.20 mm "minimum" web between these patterns and stay within 0.10 mm from the pad edge. And if the calculator calculates anything less than that, you're going to get a small web in between the stencil apertures. When they go to assemble it, they're going to use that stencil a dozen times and shred it because the web between the apertures is so small. But the stencil manufacturers should know this. And they should make the stencil a bit more rugged for the paste mask application process.

Shaughnessy: Tom, Happy mentioned a few weeks ago that the standards in some countries and some of the manufacturers' own numbers were far superior to IPC's standards.

Happy Holden: Yes, JPCA had been using lead-free solders for a lot longer than we had. And because of their focus on miniaturization and the fact that lead-free solder was much stron-

ger than tin-lead solders, their land patterns were much, much smaller than ours.

Matties: So, Tom, when you are perhaps instructing a class or educating your customers, what would you tell your students regarding footprints and how to avoid a failure?

Hausherr: If I were going to do a class, I would say that accurate 3D models would have to be mandatory for quality control. I went to work for a company in Orange County, California, five years ago and I worked side by side with

If I were going to do a class, I would say that accurate 3D models would have to be mandatory for quality control.

a gentleman who knew SolidWorks inside out. He did everything backward: He took the package dimensions and meticulously drew the 3D component model in SolidWorks, then took that model and designed a pad pattern underneath it. He created his own toe, heel, and side solder joints from the 3D model. It was kind of like reverse engineering. You create the 3D model first and then you create the solder pattern after the 3D model.

Matties: If you follow that strategy, whether you do it first or second, the modeling shouldn't have any errors related to footprint mismatch.

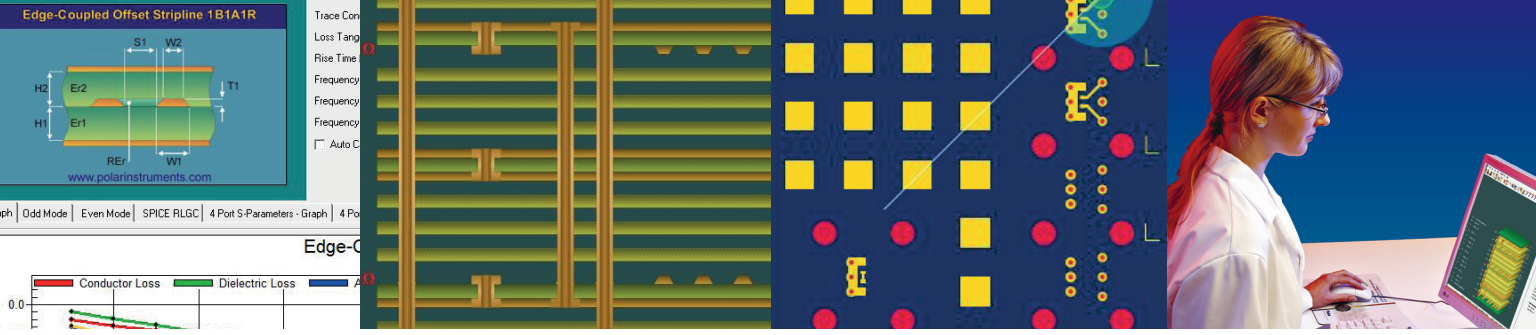
Hausherr: Yes, the 3D modeling must have the highest integrity. The model must be created using the exact package and terminal lead dimensions. When you have the 3D STEP modeling, it's really easy to detect an error in a through-hole footprint. But for surface mount, you put the 3D model on a surface mount pattern, you look at it and you think, "Well, I don't know if it's right or not. Is the toe correct? Is the heel correct?" A basic understanding of terminal lead style rules and their respective solder joint goals would help you make that determination.

If I were to do a class on land patterns the first topic would be that 80% of the parts on a circuit board are chip resistors, capacitors, inductors, and filters. I would say, "Let's design a pattern for each package size because there's not one magic formula." An 01005 chip package requires a unique land pattern, then then you have a 0201 and it requires its own unique toe, heel, and side. You have a 0402, a 0603, a 0805, and they all require unique patterns.

The IPC-J-STD-001 standard is my leading document. When I took the IPC-J-STD-001 class, I learned how to hand solder and learned all about solder joints. I learned a lot of information about solder joint acceptability for assembly. The very first sentence in IPC-7351 land pattern guideline reads, "This document should adhere to the IPC-J-STD-001." Actually, it doesn't, as far as solder joint goals for various chip sizes and gull wing pin pitches. However, the IPC-7351 mathematical model for calculating an accurate land pattern has stood the test of time for the past 34 years, but the solder joint goal values for toe, heel, and side need to be updated for microminiature components and fine pitch packages.

Matties: How are the datasheets? When you come in and you're dealing with a new component, do you validate the datasheets on your own? Do you trust them? What's your strategy there?

Hausherr: The datasheets provide the package dimensions. And most datasheets today provide the recommended pattern. Some of the patterns are getting so complex that it's like designing a mini circuit board. It takes five hours to design one pattern. Today's manufac-



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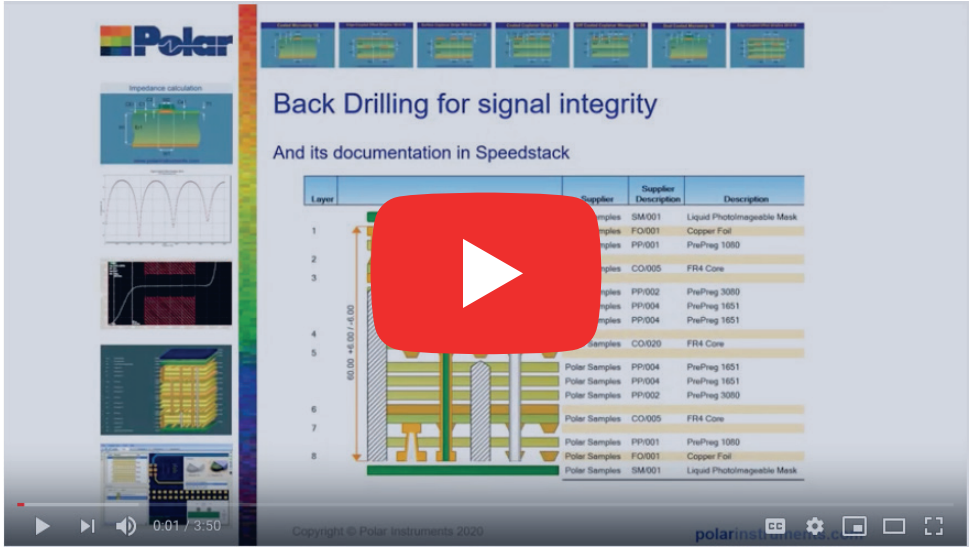

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turers are designing tiny 7 mm x 5 mm packages with a gazillion pins underneath them. They're bottom terminal only, and every pin seems to have a different size and location with a different solder and paste mask. They'll have one page in the datasheet set aside just for the pad dimensions, another page for the pad locations, another page for the solder mask dimensions, solder mask locations, the paste mask dimensions and another of the paste mask locations. It gets to be really, really technical with a lot of geometry mathematics involved.

Dieter Bergman and I tried to figure out how much money is being spent in the industry in library part creation for schematic symbols, footprints, and 3D models. We looked worldwide at all the companies, patterns, and boards that are being made. We concluded that to be an expense of about $1 billion a year. The $1 billion includes salaries, computers, CAD tool software, furniture, training, and compensating for errors and mistakes in library creation. A lot of revenue goes into PCB library creation globally and the main reason why the yearly expense for creating PCB libraries is so high is because most companies create their own library parts using their company rule set and that contributes to massive duplication of effort. However, we can greatly reduce cost and error rate by having access to all the schematic symbols, standard package dimensions, non-standard manufacturer footprints, and 3D STEP models in a single location on the cloud. This is a tremendous never-ending project as the number of new component packages every week is overwhelming. This year, over 20 million brand-new electronic component part numbers will be introduced.

Digi-Key currently has 11.5 million parts on its website. The Valor Parts Library contains over 35 million part numbers for PCB mount components. SiliconExpert supports datasheets on over 1 billion electronic part numbers for both current and obsolete parts. That's a lot of symbols, footprints, and 3D models.

The concept of reducing cost and errors of PCB library creation is a reality. You need a software program that only requires package and terminal lead dimensions, and tolerances and a user-defined set of options to define all your personal library construction rules. This way you get consistent quality in your PCB library. Also, you can change any of your personal options or your CAD tool and regenerate your complete PCB library from scratch using your collection of package dimensions and tolerances.

Matties: Well, this has been really good. Any final thoughts, Tom?

Hausherr: I have one final thought. In your PCB library calculator tool, you have a nominal 1:1 scale image package outline and terminal leads; when the terminal leads fall somewhere on the pad, you'll be fine. It's when the pad falls away from the terminal lead that you run into trouble. And that's where the Valor PL and the 3D model can reduce errors.

In our software calculator tool, Footprint Expert, we draw the rectangular shape of the terminal lead on the pad, so when the user calculates the IPC pattern, enters the manufacturer component recommended pattern dimension, and the pad falls off the terminal lead, you must go back to the IPC pattern. In this case, the manufacturer pattern dimensional data could have a typographical error.

IPC's mathematical model for land pattern calculation comes all the way from the 1987 release of IPC-SM-782 for 18 years, into the IPC-7351, all the way up to today. Now, things are changing; tolerances used to be robust, but tolerances today are getting smaller and smaller, because the manufacturers are getting better, high-quality machines to manufacture their component packages.

I hear this all the time: "I want to use a single 0603 footprint for all my 0603 resistor packages. There are about 22 manufacturers who create 0603 resistors, and I want to use the same footprint pattern and 3D model for all of them."

Well, guess what? You could do that, but you must use the same exact package dimensions and tolerances. If one manufacturer's dimensions and tolerances fall out of your master set, then throw that manufacturer off to the side. All of your manufacturers for an 0603-resistor package should have the same dimensions and tolerances. There is no standard for resistor package dimensions and tolerances, but if we band together and reject packages that fall outside the mainstream, a de facto standard will eventually emerge. Most chip package dimensions are standard. The package tolerances make a messy PCB library where it generates all these different patterns for an 0603 pattern for a resistor. The main reason for standardizing package dimensions and tolerances is to reduce the number of footprints in your CAD library. But the big problem is that you can use one manufacturer in your BOM, but the assembly shop may save you money by using a different manufacturer's chips that they have in stock. That's okay, as long as the parts they use match your package dimensions and tolerances.

I want to mention that the package and terminal tolerances affect the resulting pad stack size and placement. You can have identical nominal package and terminal dimensions, but different tolerances will produce different footprints. The IPC mathematical includes the tolerances in the land pattern calculation to allow proper solder joints in case the component is delivered in the minimum, nominal, or maximum material condition. However, I've heard from many assembly shops that most component packages are delivered in the nominal material condition. Therefore, you can use a tolerance of zero and greatly reduce the size of your PCB library. If you must use tolerances, standardize them.

Matties: Thanks for your time, Tom.

Hausherr: Thank you. I enjoyed it. DESIGN007

Shell, C3 AI, Baker Hughes, Microsoft Launch Open AI Energy Initiative

Shell, C3 AI, Baker Hughes, and Microsoft announced the launch of the Open AI Energy Initiative (OAI), a first-of-its-kind open ecosystem of artificial intelligence (AI)-based solutions for the energy and process industries. The OAI provides a framework for energy operators, service providers, equipment providers, and independent software vendors for energy services to offer interoperable solutions, including AI and physics-based models, monitoring, diagnostics, prescriptive actions, and services, powered by the BHC3 AI Suite and Microsoft Azure.

The initial OAI reliability solutions offered by Shell and Baker Hughes enable interoperability between BHC3 Reliability, OAI modules, and existing industry solutions for such applications. Solutions available today include proven and tested equipment- and process-specific modules with pre-trained AI models, codified subject matter expertise, low-latency data connectors, thermodynamic and operating parameter libraries, global health monitoring services, deep diagnostics, failure prevention recommendations, and prescriptive actions.

(Source: Business Wire)

Avoiding 'Blushing' and 'Bubbling' in Conformal Coatings

Sensible Design

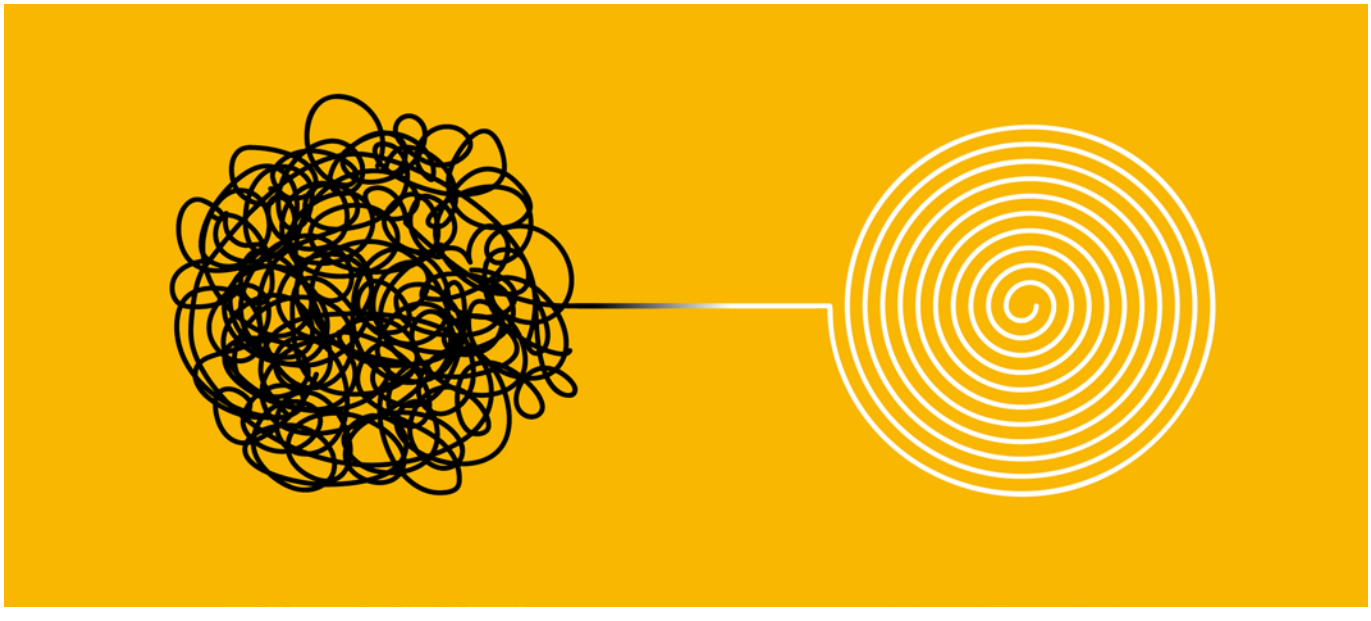
by Phil Kinner, ELECTROLUBE

The performance requirements of conformal coatings continue to become ever more challenging as electronic assemblies are becoming smaller and smaller and subjected to increasingly hostile operating environments. The perfect conformal coating would retain high elasticity at both high and low temperature extremes and would maintain its properties at high temperatures with no out-gassing. It would also provide an excellent barrier to moisture, both in terms of humid environments and where there is a risk of liquid water splash. It would be highly resistant to solvents and corrosive gases but be easy to remove when repairs or modifications need to be carried out. Ultimately, the perfect coating would be intelligent, self-applying and, of course, free of charge—but then that's a whole different ball game.

In this month's column, I will revisit a couple of general enquiries we have received about "bubbling" as well as the less common appearance of cloudy white patches following the application of a conformal coating.

Blushing

Naturally, we are all aware of the many potentially problematic encounters that can occur when using conformal coatings. The usual suspects tend to be contamination leading to corrosion, cracking, blistering, fisheyes, de-wetting, and so forth. However, one of the rarer problems that can occur is "blushing." If you have the misfortune of discovering that your coating isn't as clear or transparent as it should be, and instead, looks dull and cloudy white, then the chances are you have stumbled upon this particular coating issue.



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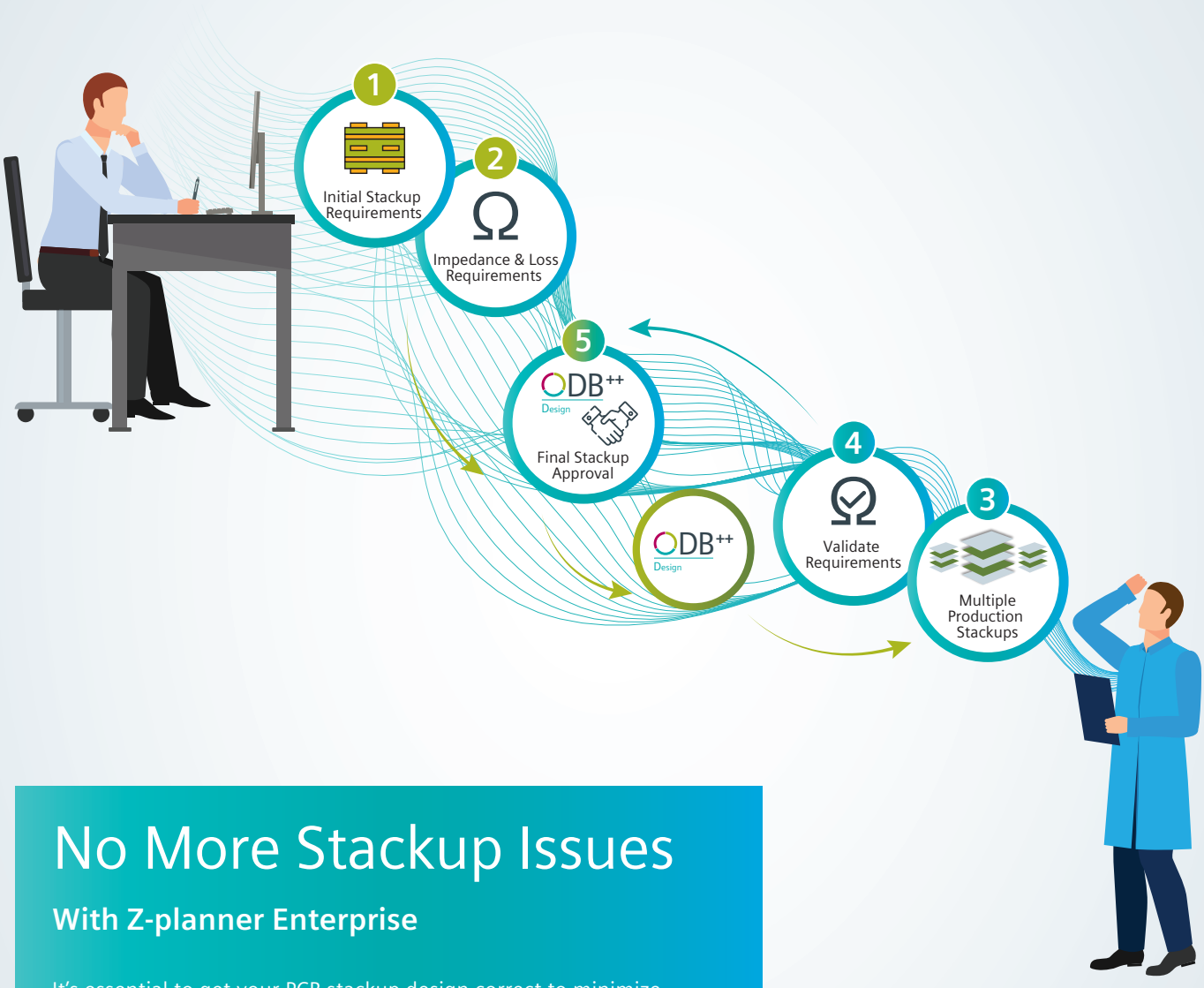

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The main reason why coatings can become milky is largely due to moisture absorption. High levels of atmospheric moisture can create havoc with certain solvent-based materials. As the solvents evaporate from the coating, a cooling effect is experienced. If this cooling effect drops the coating below the dew point, then water will condense onto and into the coating as it dries. This can range from a reversible cosmetic effect (heat it up and the discoloration should disappear) to problems with the coating developing adhesion, or its full protective properties. Blushing can be identified when the conformal coating becomes cloudy, hazy, or milky in appearance. Humidity is a big issue, especially if it exceeds 65%. Equally, low temperatures can also wreak havoc at lower than 15°C. Issues that arise from assemblies/components stored in environments with excessive moisture can be addressed by baking the boards.

Some of the problems that can arise from blushing include:

- Surface tackiness
- Poor adhesion
- Incomplete cure
- Poor adhesion with second coating
- Dull, matte finish

Blushing can occur when using aerosol coatings. To avoid blushing when coating via aerosol, there are some important points to remember. First, there is no need to shake the aerosol can before use, as this can add bubbles to the mixture which can then be transferred to the board. The board should be at a 45-degree angle to the can, (e.g., if the board is flat, the can should be at 45 degrees) and around 20-30 cm away from the can. Spray the board in a continuous steady Z motion, coating evenly. The board should then be rotated 90 degrees, the coating applied again using the same motion, and the board rotated again, repeating the process until you have rotated the board a full 360 degrees. This allows an even coating of the correct coating thickness and ensures the coating can cover raised components and leads from different angles, thus ensuring the best coverage possible. A turntable can be used to aid this process.

Other factors to help prevent blushing include maintaining a stable humidity and temperature in the production environment. At Electrolube, we recommend humidity between 50-65% and an ambient temperature environment between 15°C and 25°C to help combat blushing. Ensuring adequate time between coating and cure is also advisable to allow solvents to evaporate fully. The use of slower thinners can also assist with the potential reduction of evaporation/condensation to reduce blushing incidences. Baking assemblies following the cleaning process can also eliminate moisture, as well as ensuring all storage atmospheres and containers are sufficient against moisture.

The quality and performance of a conformal coating material could also be compromised according to the method of application. This is commonly encountered when a product is transferred from one circuit manufacturer to another; for example, a product may be dip-coated in one country but selectively coated in another with the specification requiring that the same material be used at both sites. The problem that arises here, however, is that using a material formulated for dip coating in selective coating equipment can result in poor yield due to it being excessively fast drying, leading to bubble entrapment. You want fundamentally different behaviour from a material in a dip-coating application than in a selective spray application. One of my customers spent six months trying to solve a bubble issue internally, without realising that the root cause of this problem lay in the material formulation. Working with the customer, it became clear that by changing the solvent blend, the bubble entrapment issue could easily be resolved. Moreover, this solution simplified the process and reduced the cycle time significantly. And since the non-volatile formulation remained the same, there was no need to re-qualify.

Bubbling

When solvents or air become trapped and can't escape the coating material, the chances of bubble formation are more than likely. Bubbles in a conformal coating can lead to product reliability issues further down the line and even possible failures. The IPC specification allows a dry film thickness of 30–130 microns, the greater thickness being achieved by the application of multiple coating layers. Trying to achieve a 130-micron dry film thickness from a single selective-coating process with a solvent-based acrylic material is a recipe for disaster and is likely to result in excessive bubble formation, film shrinkage, coating de-lamination and additional stress on components. The result is poorer protection, rather than an improved overall level of circuit protection. Aiming for a uniform 30–50 microns and focusing on achieving perfect coverage at each application is a much better approach to improving the protection of electronic circuits. Achieving the correct coating thickness is important. Bear in mind that if the coating is too thick it can lead to entrapment of solvents in areas where the coating does not fully cure. Similarly, it can cause the coating to crack as it cures, as the result of changes in temperature, or due to mechanical shock and vibration.

Conformal coatings protect electronic assemblies from harsh environments by sealing off the electronics from contaminants and environmental factors that can lead to reliability issues and failures. For coatings to be effective, they need to uniformly cover the entire component without moisture, fluid, or outside impurities present. While it might be tempting to use shortcuts either to reduce costs or to speed up production, there will inevitably be a price to pay. Know the limitations and/or special properties of the materials you use to coat electronic assemblies and abide by the correct procedures. Still have doubts? There are experts on hand at Electrolube who have seen it all before and who can steer you in the right direction. **DESIGN007**

Phil Kinner is the global business and technical director of conformal coatings at Electrolube. To read past columns or contact Kinner, click here. Download your free copy of Electrolube's book, *The Printed Circuit Assembler's Guide to... Conformal Coatings for Harsh Environments,* and watch the micro webinar series "Coatings Uncoated!"

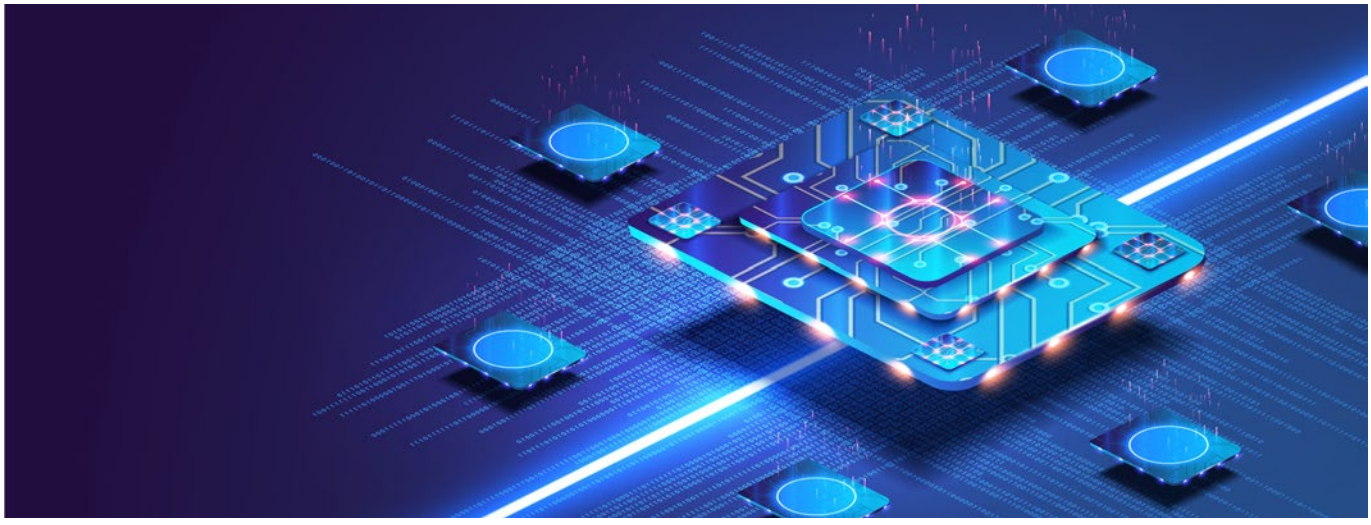
How Unmanned Underwater Vehicles Could Become Easier to Detect

Detecting the presence of an unmanned underwater vehicle (UUV) is usually achieved by intercepting the noise radiated by its propeller. In a noisy harbor, this task is hindered because the acoustic signature of a UUV and the noise in the local environment often present too much signal complexity for current technologies to process.

That may be about to change. Researchers at Draper, Massachusetts Institute of Technology (MIT) and Woods Hole Oceanographic Institute (WHOI) have developed an acoustic remote sensing method for high-precision propeller rotation and speed estimation of UUVs.

A state-of-the-practice technique for identifying the presence of ships is by analyzing passive acoustic data with the Detection of Envelope Modulation on Noise (DEMON). In the study, the authors set out to isolate and characterize motor noise, so they focused on brushless DC (BLDC) motors because of their prevalence in UUV propulsion systems.

In field experiments, the new method outperformed the DEMON algorithm. When boats passed by the UUV, the new method could detect the motor noise, but the DEMON spectrum was dominated by the interfering boats' propeller noise. The new method can also apply to other robotic platforms that are powered by mass-produced BLDC motors. (Source: PRWEB)



Managing Footprints with Integrated EDA Tools

Feature by Matt Walsh
SIEMENS DIGITAL INDUSTRIES SOFTWARE

Electronics companies are always under great pressure to continually grow and innovate. In addition to navigating ever-accelerating design cycles, they must also address and overcome generational complexities associated with their products, the underlying components they use, and the human capital accountable for delivering on time and on budget. Electronics firms can ill afford the time and resource inefficiencies associated with manually correcting design errors, poor library data integrity, or other inconsistencies leading to missed deadlines or even costly re-spins.

The quality of eCAD libraries—or, more specifically, the quality of the underlying logical and physical models—plays a pivotal role in stemming the challenges of delivering a successful electronics product to market. In fact, the eCAD library affects every process from PCB layout to PCB manufacturing and assembly.

The Siemens PartQuest cloud-based application is a gateway to a large collection of component technical content for electronics design. This addresses five critical factors relative to best-in-class PCB library solutions:

1. High-quality eCAD model content.
2. Symbol and footprint creation.
3. Library management.
4. Standards.
5. Integration with Xpedition and PADS Professional.

In October 2020, Siemens released the PartQuest Vault, consisting of eCAD models (symbols and footprints) for over 1 million parts. These pre-made models are entirely created, validated, and maintained by Siemens. A rules engine consisting of validation logic and thousands of checks are run against model content to confirm construction correctness, which provides end-customers with peace-of-mind when using this content. Further, the Vault is parametrically or keyword searchable, which simplifies the identification of the precise part to meet a product design's requirements, and the Vault is expected to contain 100 million parts by the end of 1QCY21.

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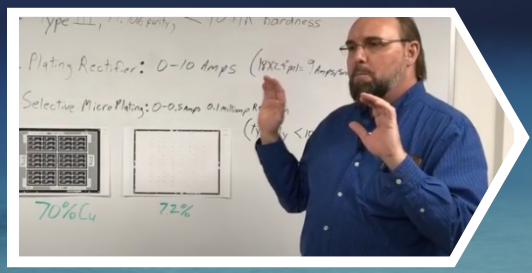

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There are inevitably instances where premade eCAD model content might not be readily available. For these scenarios, users have one of two options. First, users can request model content be constructed; turnaround time is typically less than 24 hours. This is presently a free service. Second, PartQuest has a robust part-builder capability. Whether a simple op amp or significantly more complex flatpack with multiple terminal groups, the "Create Footprint" capability guides users through easy-to-follow wizards and templates (including tool tips) to create content that is correct by construction.

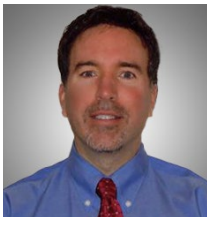
Whereas library content management is traditionally conducted via desktop authoring tools, Siemens has added a new dimension, allowing users to create cloud-based projects to manage library content sourced from the cloud. This valuable functionality is a lightweight library management tool for storing and managing library data. Content stored in projects can be quickly downloaded for use on desktop capture-and-layout tools, either in bulk, or on a single part basis.

We are particularly conscious of industry standards. For example, footprints created in PartQuest are constructed according to the IPC-7351B standard, which establishes requirements for surface mount device (SMD) pad dimensions in PCB footprints. The part builder footprint wizards also support the JESD30I standard (for package outline, terminal types, and terminal position classifications), and the JEP30-P100 JEDEC standard (for shape definitions and the terminal vertical dimensions).

PartQuest is evolving to meet the needs of the PCB design community. In fact, later this year, the solution will add support for multigeneration footprints based on customer-defined custom rules. Here's why this enhancement helps PCB designers: While manufacturing technology has evolved a great deal over the past decade, the IPC-7351B standard has not. For example, the land pattern used for a part deployed within a mobile handheld device with expected life span of about three to five years will need to be miniaturized for future versions featuring smaller form factors. Alternatively, if this exact same part is deployed on a high-end mission-critical type product, the reliability requirement may stretch to 15–20 years. Because it enables rule customization during the footprint creation process, users can achieve low-density footprints with larger pads, thereby supporting longer term reliability requirements.

Although access to high-quality eCAD model content is important, its value is dramatically reduced if the content is incompatible with the authoring tools. For this reason, this solution integrates with the Siemens Xpedition and PADS Professional flows. This integration allows PCB designers to simply search for the component they need, select it by clicking on the part, then drag-and-drop the part to the desktop authoring environment. This task can be completed one part at a time or, by organizing selected parts utilizing projects in bulk, which enables quick drag-and-drop functionality.

In the final analysis, today's PCB design community requires tools that eliminate pain points associated with component data throughout the product creation process. The digital transformation underway in the component ecosystem is still in its infancy. We envision a world where electronic components are represented by standards-based digital twins that encompass physical, electrical, thermal, and assembly data, all sourced by component manufacturers and directly consumable by downstream tools used during each phase of the product creation process. We've made tremendous progress, but much more work lies ahead. **DESIGN007**



Matt Walsh is a product manager for Electronic Board Systems, Siemens Digital Industries Software.

PCB007 Highlights

CES Dispatches: Opening Day at Pepcom ▸

On Monday, January 11, Nolan Johnson attended the launch of the CES 2021. Well, more precisely, he attended the Pepcom program, one of the multitude of ways to connect with CES in the virtual environment. Pepcom is a regular at CES, functioning a bit like a show-within-a-show.

Your Greatest Competition is Yourself ▸

It really doesn't matter who you think your external competitors are, because the only competitor that really matters is you. Of course, you will look externally to stay on top of latest trends, but when it comes to competition, just competing with yourself is a win. When you look at yourself as your greatest competitor you will start with a huge advantage: you already have great intel on how "your competition" thinks. Ask yourself, "What can I do to displace my 'competitor' and create something much better?"

Bruce Mahler Discusses Ohmega Technologies' Acquisition by Arcline Investment Management ▸

I-Connect007's Nolan Johnson catches up with Bruce Mahler, vice president and general manager at Ohmega Technologies, about Thursday's announcement that Ohmega Technologies has been acquired by Arcline Investment Management. Mahler outlines the new opportunities this presents for Ohmega Technologies and discusses how this change in ownership will benefit existing customers and markets as well.

Punching Out! The 'Dream' Business Exit ▸

Almost all business owners have a "dream exit": a well-financed buyer flies in, offers up a suitcase full of cash with no strings over a steak and lobster dinner, and the next day the owner is sitting on a beach with a mai tai. These kinds of dream exits do occur, but they are extremely rare. Tom Kastner explains.

IPC CEO and President John Mitchell Discusses New Membership and Dues Structure ▸

In this video, IPC CEO and President Dr. John Mitchell discusses the organization's move from a site-based and enterprise membership dues structure to a company revenue-based model. Mitchell explains that this change will go into effect upon each member company's renewal in 2021, and he points out that many of the existing member discounts will remain unchanged.

I-Connect007 Editor's Choice: Five Must-Reads for the Week ▸

In this week, we have a variety of news and articles to share, and it's all positive. We have a new president, and he's pledging to help American businesses. December PCB sales were up 4.5% over the same period a year ago. Atotech is just about ready to launch an IPO. Sunstone has tweaked its free CAD tool, PCB123, to make it even easier for designers to receive their Gerber files. And columnist John Watson breaks down what we all learned during the chaos that was 2020.

APEX EXPO IPC 2021

Schedule at a Glance

As of January 2021:

Monday, March 8

8:45–8:50 a.m.	Welcome Message
9 a.m. –Noon	EMS Management Meeting
9 a.m. –Noon	Managers Forum: Managing Challenges in Periods of Transition—*Presented by the Raymond E. Pritchard Hall of Fame Council*
9 a.m. –Noon	Professional Development Courses
12:30–1:30 p.m.	Keynote Presentation *by John Mitchell, President and CEO, IPC*
1:30–5 p.m.	EMS Management Meeting
1:30–5 p.m.	Managers Forum: Managing Challenges in Periods of Transition—*Presented by the Raymond E. Pritchard Hall of Fame Council*
2–5 p.m.	Professional Development Courses

Tuesday, March 9

8:45–8:50 a.m.	Welcome Message
9 a.m.–Noon	Professional Development Courses
9 a.m.–Noon	Exhibitor New Product Presentations
12:30–1:30 p.m.	IPC Annual Meeting and Awards Ceremony
12:30–1:30 p.m.	A Virtual Escape Experience
2–5 p.m.	Professional Development Courses
2–5 p.m.	Exhibitor New Product Presentations

Wednesday, March 10

7:55–8 a.m.	Welcome Message
8–8:45 a.m.	Keynote Presentation *by Travis Hessman, Editor-in-Chief, IndustryWeek*
10 a.m.–Noon	Technical Conference Sessions
11 a.m.–Noon	Forgotten Tribal Knowledge with IPC Hall of Fame and Emerging Engineers
12:30–1:30 p.m.	IPC Emerging Engineers Roundtable
12:30 –1:30 p.m.	Exhibitor New Product Presentations
12:30–1:30 p.m.	Live Q&A with *Travis Hessman, Editor-in-Chief, IndustryWeek*
1:30–3 p.m.	Technical Conference Sessions
1:30–5 p.m.	Exhibitor New Product Presentations
3:30–5 p.m.	Technical Conference Sessions

Thursday, March 11

8:10–8:15 a.m.	Welcome Message
8:15–9 a.m.	Keynote Presentation by *Shawn DuBravac, Chief Economist, IPC*
9 a.m.–Noon	Professional Development Courses
9 a.m.–Noon	Exhibitor New Products Presentations
10–11:30 a.m.	Technical Conference Sessions
12:30–1:15 p.m.	IPC Education Foundation: Looking Ahead
12:30–1:30 p.m.	Trivia Networking and Name That Tune
1:30–3 p.m.	Technical Conference Sessions
1:30–5 p.m.	Exhibitor New Product Presentations
2–5 p.m.	Professional Development Courses
3:30–5 p.m.	Technical Conference Sessions

Friday, March 12

9–9:45 a.m.	IPC at a Glance (Standards, Education, Advocacy, Solutions and Industry Intelligence)
10–10:30 a.m.	Exhibitor New Product Presentations
10:30 a.m.–Noon	Technical Conference Sessions
Noon–12:15 p.m.	Closing Remarks

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Making the Most of a Virtual Event

Feature Interview by Nolan Johnson
I-CONNECT007

Nolan Johnson speaks with Alicia Balonek, senior director of tradeshows and events at IPC, about how both attendees and exhibitors can best prepare for this year's virtual IPC APEX EXPO and breaks down some of the events you can look forward to at this year's show.

Nolan Johnson: Hi, Alicia. IPC APEX EXPO is going to be different for 2021. Those of us who are regulars know how to get around in a physical venue and how to make the most out of being all together in one place. But this won't be exactly the same. Could you walk us through some of the most effective strategies for making the most out of the virtual event for IPC APEX EXPO?

Alicia Balonek: Sure. I'd be glad to help out our future attendees. We're actually working with two different platforms, but from the attendee side and the exhibitor side, it will be seamless. The first platform is the platform that we've been using for years: our agenda planner or online exhibit hall. Once someone registers for the event, they will automatically receive a link to register to this platform to set up their attendee profile. That is the platform they will use to connect with exhibitors and other attendees, as well as setting up their planner and their schedule for the week and which events they'll be attending. There's also a feature for exhibitors which allows them to upload product images, videos, presentations, press releases and company descriptions. They can select what their product categories are, and it also gives them the opportunity to schedule appointments as

well with attendees and even other exhibitors, if they want to.

The most important part of both of these features is to turn on the networking capabilities so other attendees and exhibitors can connect with each other. Since there are so many variables and features with this program, we are actually in the process of creating customized videos—one specific for attendees, and one specific for exhibitors—which will be available on our website weeks before the virtual event, to show people how to use this platform and how to get the most out of it.

Johnson: That is something that, to my knowledge, is unique when it comes to doing virtual events. I don't think I've ever seen anybody give advanced tutorials on how to use the environment.

Balonek: That's the point (laughs)! We want to make sure that people have a successful experience with IPC APEX EXPO. The more that we can do ahead of time to help people with their experience, then that's what we want to do to make sure that everyone comes away with everything possible on how to connect, how to find products and services that they're looking for, and how to find any education that they need, as well.

Johnson: Will there be links to access this information?

Balonek: Yes. In fact, the agenda planner is live now.

Johnson: Great. When will this be turned on for the public?

Balonek: It is turned on right now, but the key is you have to register for the event in order to access the information. If an attendee is not sure whether they want to register for a paid option at this time, they can register for Event Essentials, there's no charge for that, and it will allow access into this platform. Additionally, our eBrochure is due to come out any day now and will be available by the time this interview goes to print.

Johnson: If I register with an Event Essentials package as my choice, what is available to me?

Balonek: The Event Essentials includes three keynote presentations. One will be given by IPC's president and CEO, John Mitchell, and another keynote is by IPC's chief economist, Shawn DuBravac. Our third keynote, Travis Hessman, editor-in-chief of IndustryWeek, will speak about Factory of the Future. All three keynotes are included in the Event Essentials package, as well as exhibitor product demonstrations and other presentations that are focused on IPC. These presentations include IPC-at-a-Glance, which will cover: Standards, Education, Advocacy, Solutions and Industry Intelligence, Forgotten Tribal Knowledge (featuring IPC's Emerging Engineers and IPC Hall of Fame Recipients), and a presentation on IPC's Education Foundation, just to name a few. These presentations will also be available for 90 days after the event.

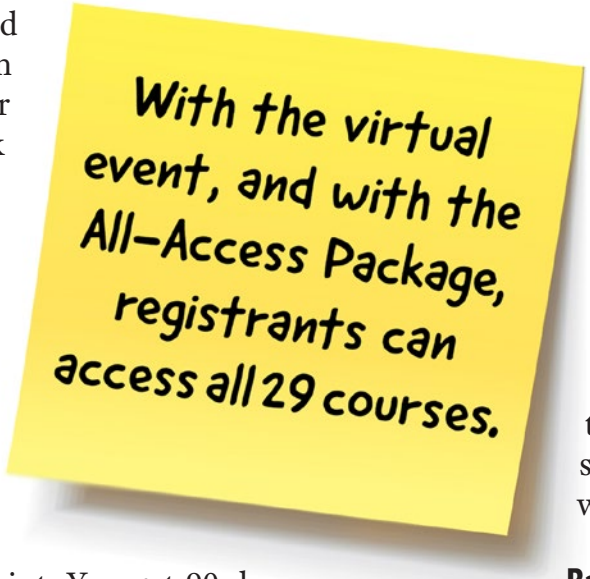
Johnson: If I were to take a step up from Event Essentials, Alicia, what would be in my registration?

Balonek: We have several options available depending on your budget. We're offering a one-day conference package, which offers access to the technical conference sessions for the day of the attendee's choice. There's also the full conference, which will give someone access to all 70 technical conference sessions with on-demand access for 90 days after the event. And then—the cream of the crop package—the All-Access Package, which includes all 70 technical conference sessions, as well as all 29 half-day professional development courses also with access for 90 days after the event. Something new this year, which has

never been done before, for the All-Access Package, all the professional development courses can be accessed for 90 days after the event. Normally for an in-person event, due to scheduling, a person would be limited to attend only five professional development courses. With the virtual event, and with the All-Access Package, registrants can access all 29 courses.

Johnson: That's a huge benefit.

Balonek: We believe so, and especially with in-person events being on hold for most of this year, we think it's very important to be able to provide our members with the training and education that they need in order to succeed. We're very excited about this package and we hope many people take advantage of it.



Johnson: That's a great point. You get 90 days of access to the material which cultivates the potential for a very immersive educational experience. It's a great way to get a lot of value out of this; go deep and wide in the content that's available.

Balonek: Another benefit to this is that people can learn on-demand. It doesn't have to be during normal work hours, because it's all accessible for 90 days; they can learn at their own pace when time permits, in the evenings, on the weekends or whatever works best for them. There's plenty of time to get through all of this content.

As an exclusive benefit for IPC members, we are offering two special, brand new, registration packages. We have a Basic Package which allows up to 100 employees from the same company to gain access to the full conference and 100 professional development courses. Again, that's live and on-demand for the 90 days that it will be accessible. Then we have a Premier Package which allows an unlimited number of employees from the same organization to attend the conference and up to 200 professional development courses. This is a way for some of the larger companies to be able to send quite a few people to the event so we can help train and educate their employees on the latest and greatest technology and solutions that are available.

Johnson: It's going to be exciting to see how all of this works over the course of IPC APEX EXPO, and to learn exactly what the results are from all of this innovation. I have to say, the setup for this event looks to be perhaps the most innovative and thorough that I've seen. I'm really excited to see what your results are.

Balonek: We are too. I mean, we have a very dedicated team and we've been working very hard at this. We want our exhibitors to have a positive experience, and we also want our attendees to have a positive experience and get them information that they desperately need to help them succeed.

Johnson: You mentioned earlier, as people get registered, to make sure that they turn on the right settings so as to be visible for networking.

Balonek: Yes, and that would be for the agenda planner, attendees and exhibitors need to "opt-in" to the appointment calendar which allows exhibitors and attendees to schedule appointments with each other.

Johnson: It sounds like a good idea to make some appointments early on with exhibitors to

cover material. Would you recommend that as a good strategy for this virtual approach?

Balonek: Oh, definitely! And the planner does also have that capability. The planner will also match attendees with exhibitors based on the demographics for each. Even the week of the live event, if an attendee attends a certain technical conference session, it will match exhibitors that have complimentary products and services based on the subject matter and the content of that particular session. The same goes for the Professional Development courses.

Johnson: Now that's interesting! You're helping me focus in on exactly who I should talk to, based on my technical program interests. You're creating a more focused agenda just for me. I may know some of these companies, but other companies may be new to me.

Balonek: Exactly. Also, if you're interested in a product, or looking at launching a new initiative within your company and you're not familiar with what companies offer products and services around that particular topic, with this feature they'll be right in front of you. We'll highlight that for the attendees, which we think is a really cool feature.

Johnson: Interestingly enough, you're driving that exhibitor connection from the technical programs. A great way of connecting attendees with new exhibitors is for the attendees to get very involved in the technical programs.

Balonek: Exactly. Similar to show floor traffic and just the casual passer-by stops by a booth, this is a virtual way of doing that now.

Johnson: That's exactly what I'm picking up on as we talk about this. Networking is an important part of going to a show, what with your peers, vendors, potential customers, IPC staffers, and the like. We always come back from the shows having met somebody new as a colleague or a customer. How do you see that happening in the virtual event?

Balonek: We have a few events planned, which we participated in as a team and we had a lot of fun with them. We are planning on doing a virtual escape room, which attendees can join as a team. We also have a "name that tune" trivia event, and I don't mind saying that, when our team tested the game, I won.

Johnson: I bet that was a lot of fun.

Balonek: Yes. It definitely is a lot of fun! And it's moderated by a DJ. He did a great job engaging people and trying to get the conversation going. All the conversations are done via the chat feature, which was fun as well.

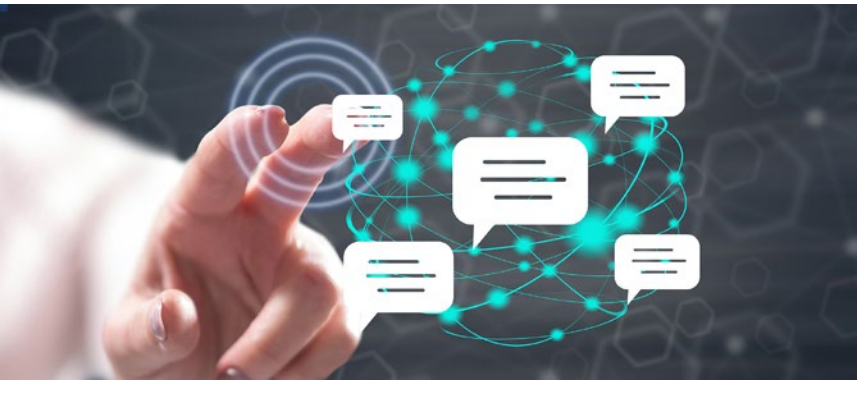
Then, for those who want more of a subject matter type educational format, we are creating an event with IPC's Emerging Engineers and our Hall of Fame members. We're calling this event "Forgotten Tribal Knowledge." We did a smaller version of this at one of our other events last year. There's so much information which we can build on, as far as transferring information from one generation to another, so this session strives to pass along working knowledge that is not found in textbooks or in training materials. We feel that is a great way to get people engaged with the industry and also with different representatives from the industry.

Johnson: Connecting experience to the younger professionals is so important.

Balonek: I think it goes both ways. They can definitely learn from each other. Also, Forgotten Tribal Knowledge is one of the events included in Event Essentials as well. So that event is free and available for everyone to attend.

Johnson: What's your vision for the serendipitous bumping into somebody, having a conversation, waiting in line for snacks in the exhibit hall or in a hallway? Do you see a way to incorporate that sort of very traditional organically occurring networking in the virtual environment?

Balonek: Well, a lot of it is going to be on both the attendees and exhibitors to reach out to one another. That's why it's critical that they work with the online agenda planner to connect with each other. We are trying to, like I said, match people up with each other. All the conference technical sessions will have live Q&A, so there's also an opportunity for people to get to know each other through the Q&A. For our keynote speaker, Travis Hessman, there will be a live one-hour Q&A with event participants later in the day, in addition to his 45-minute keynote presentation. So, it would be nice if they can build upon the questions that are asked and connect with each other after the event. If attendees allow us to share their information with exhibitors, we send the attendee list to the exhibitors so they can reach out to them before and after the event.



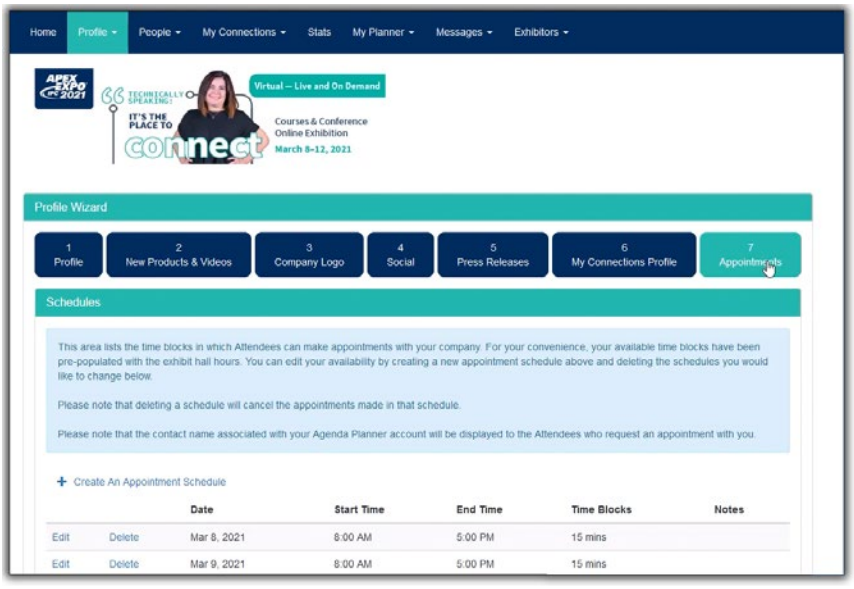
Johnson: I have heard on several occasions people comment that the virtual approach will allow for a much more global reach for IPC APEX EXPO. Do you see that unfolding?

Balonek: Yes, I do. And not only a global reach, but I also see this as a potential for people who aren't normally able to attend the event to participate this year in some capacity. Even though all the events will take place in central time zone, again since everything is on-demand, they are able to access this virtually on-demand wherever they are for 90 days after the event. We often hear from some companies that they can only send so many people to the event, but they would like to send more. This is the opportunity for more people to attend now, because you don't have the travel related expenses of hotel, airfare, meals, etc. And as I mentioned earlier, we have a one-day conference option. We also have a single session pass option if people just want to attend one or two sessions, they have the opportunity to do that as well. I definitely see our reach with the younger engineers who may not have the authorization to travel or the budget to travel as well as expanding our reach around the globe for people to participate.

Johnson: Now, it's tricky to be an exhibitor in a virtual environment, in that all of our normal ways of operating as an exhibitor change, and we interact with our booth visitors in a very different way. You've already alluded to making appointments and scheduling through the planner. As an exhibitor, what sort of support can I expect to receive in this environment?

Balonek: We're working on a video to show them how to make the most out of their exhibitor profile and virtual experience. This is a platform we've been using for years, but some exhibitors don't take full advantage of every feature available, while some do. So,

we're creating a video to show them what they can do to utilize every single feature that's available to them. Talking about the traditional virtual booth, based on my own experience with the events that IPC participated in the last few months, and also feedback from our exhibitors, the current model, in my opinion, is not working. I think a lot of organizations are trying to take that brick-and-mortar exhibit hall and just plop it into a virtual environment.



I don't see people just hopping in a booth to ask, "Oh, what's this company do? What's that company do?" We wanted to provide more value to our exhibitors, for brand recognition. So, we decided, during select times throughout the week, we are giving exhibitors the opportunity to post a commercial. It will be a two- to three-minute commercial on their products and services. And they're strategically placed before certain events throughout the week, to give them the largest audience of viewers and there are several time slots available.

We're also giving exhibitors the opportunity to present a product demonstration. These products demonstrations will be recorded and will also be available on-demand for 90 days after the event. Then already we've talked about the matchmaking tool. In the conversations we've had with exhibitors regarding these features that we're providing, they have been very well received because these opportunities give them the exposure to the attendees they're looking for and provide real ROI. With a virtual booth, exhibitors are waiting for the attendees to come to them whereas with our approach, we're putting exhibitors in front of the audience for them.

Johnson: Yes, I've been attending CES as we have this conversation. CES is a massive show. I think there were 200,000 attendees last year and exhibitors in the thousands. Once you get into a virtual environment it feels like you're looking through a long paper tube. The sensation is very much that of tunnel vision. Go to a very large show like CES, and your vision doesn't expand, doesn't open up. As attendees, we know we're missing 99.5% of what's going on at the show just because it's not immersive. I think what you're doing makes a lot of sense.

Balonek: Yes. I really feel for exhibitors. I know how important trade shows are to them. Every year we survey our attendees and ask for the top three reasons they attend APEX EXPO. Consistently year after year, the number one reason is exposure to new products and services so for our virtual event it's important that we continue to highlight new products and services which is a feature provided through our online platform. Exhibitors have the ability to upload their new products and services along with press releases and video demonstrations. And IPC will continue to highlight and promote exhibitor new products as we do every year.

Johnson: Alicia, what isn't going to happen? If I should be prepared for something to not to be available, what should that be?

Johnson: Yes, that makes a lot of sense. Typically, the committee meetings help drive attendance to the show, and the show drives the opportunity to get involved with the committee meetings. They feed off of each other, but they also compete for the same amount of the very precious three- or four-days' time.

Balonek: Exactly. We always hear there is too much to do and not enough time, which is a good thing. The committee awards will not be taking place either virtually, these individuals work so hard and we feel that they deserve the recognition in front of their peers and it's best to celebrate their accomplishments when we're able to reconvene in person.

Balonek: Obviously, since we're not in person, we will not be having the show floor reception and other various reception type events, like the ice cream social on the show floor, the Women in Electronics Reception or the Newcomers Reception. Those events will not be taking place. Also, the standards committee meetings will not be taking place during the live event. Those meetings will be held in the same capacity as our summer committee meetings, and the IPC committee staff liaisons are communicating with their various groups to schedule those meetings. We'll also have a dedicated website for the committee meetings so the participants know when they will be taking place after the event. We just didn't want to dilute the audience, there's so much content that we're trying to deliver this year. For the committee meetings and the conference to compete for people's time, we thought that this is a year to at least separate them so people can participate in both programs, because they're both very important to IPC.

Johnson: Is there a plan to have awards announced and then do a ceremony later? Is that how that's going to work?

Balonek: For the IPC recognition awards, like the Hall of Fame, the Corporate Recognition, the President's Award, the Dieter Bergman IPC Fellowship Award, and the Rising Star Award, those will be presented during the IPC annual meeting. The committee awards will be presented at a later date, most likely during the fall committee meetings.

Johnson: Great. Thanks for taking the time to speak with us today, Alicia. DESIGN007

Links

- Click here to access the Agenda Planner. A badge number from registration is required to sign in and create a profile.
- Click here to access the IPC APEX EXPO 2021 brochure.

Figure It Out: Closing the Gap Between College and Industry with PCEA

by Dugan Karnazes
VELOCITY RESEARCH

A few months back, I had the opportunity to meet Mike Creeden at the 2020 Altium Live conference. For those who don't know, Mike ran San Diego PCB, a well-regarded PCB design company and is now the technical education director at Insulectro. As someone growing a design company of my own, I knew It would be foolish to miss an opportunity to pick his brain. Between comparing notes and getting to know each other a bit, it was immediately clear to me that Mike was incredibly passionate about education and the PCB industry. He had also encountered and solved many of the business issues I had been running into (but more on that another time).

It's been my (and my intern's) experience that PCB design education is notably lacking from college EE curriculums. Even basic understanding of how to design a PCB and the manufacturing, routing techniques, and test processes involved are completely unaddressed. When I was in school, the first PCB we designed was downright cringe-worthy. We used the free version of Eagle with a former instructor's libraries, and then we were asked to keep rearranging components on the board until the autorouter could solve everything on a two-layer board. The board was made without solder mask or silkscreen. No concepts of return paths, power distribution, decoupling, shielding, manufacturing, or principles beyond the bare minimum of electrical conductivity were covered in the class. This was a college level course I'm still making payments on.

This may have been passable before engineers were expected to know how to design circuit boards, but that's not the case today. I'm a big fan of Eli Hughes's term "full stack hardware engineer," because it really does capture the expectations for what we're required to know today. The full stack engineer understands everything from idea to manufacturing; the PCB is a major part of that process.

It's also clear to me that trying to cram it all into a four-year degree is probably not possible. Our outstanding intern Austin Gilbert also shares this sentiment. So much of what we do here at Velocity Research is not even mentioned in the classes at his university. Colleges still depend on the industry to cover this material, but many companies keep their techniques confidential. **DESIGN007**

To read this entire column, which appeared in the Design007 Week Newsletter, click here.

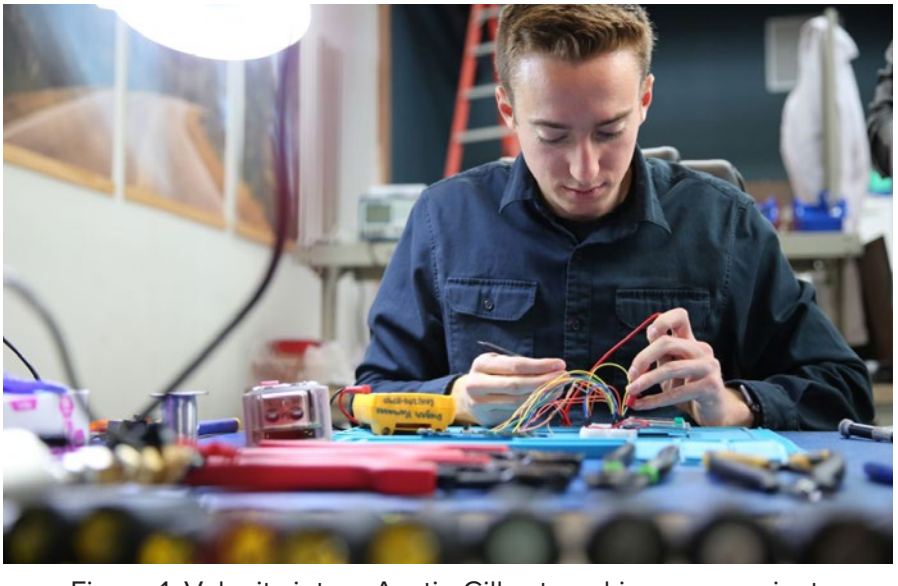
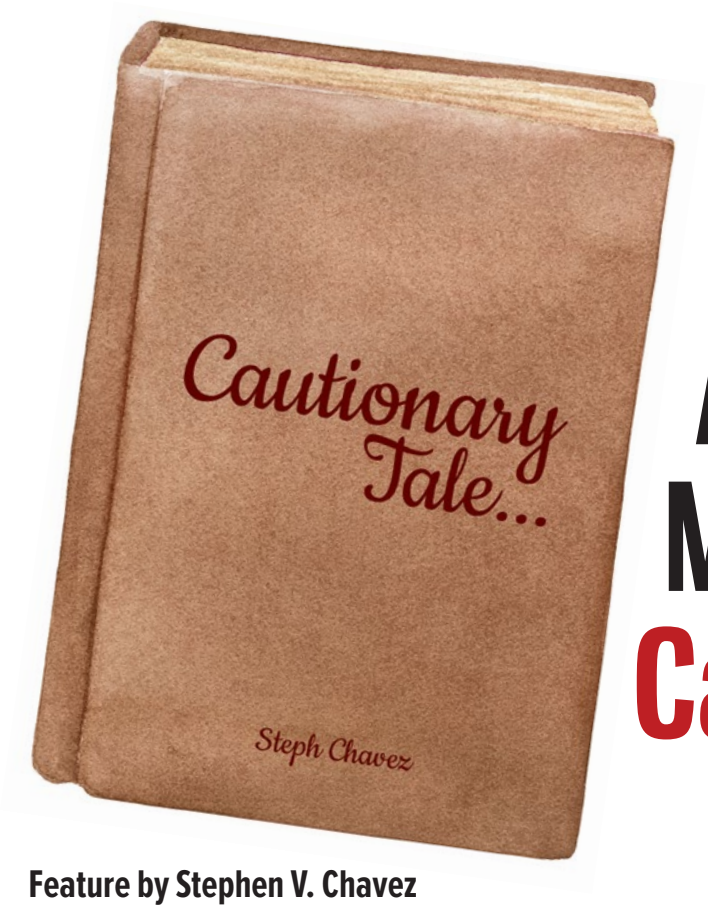


Figure 1: Velocity intern Austin Gilbert working on a project.



A Library Management Cautionary Tale

Feature by Stephen V. Chavez
PCEA

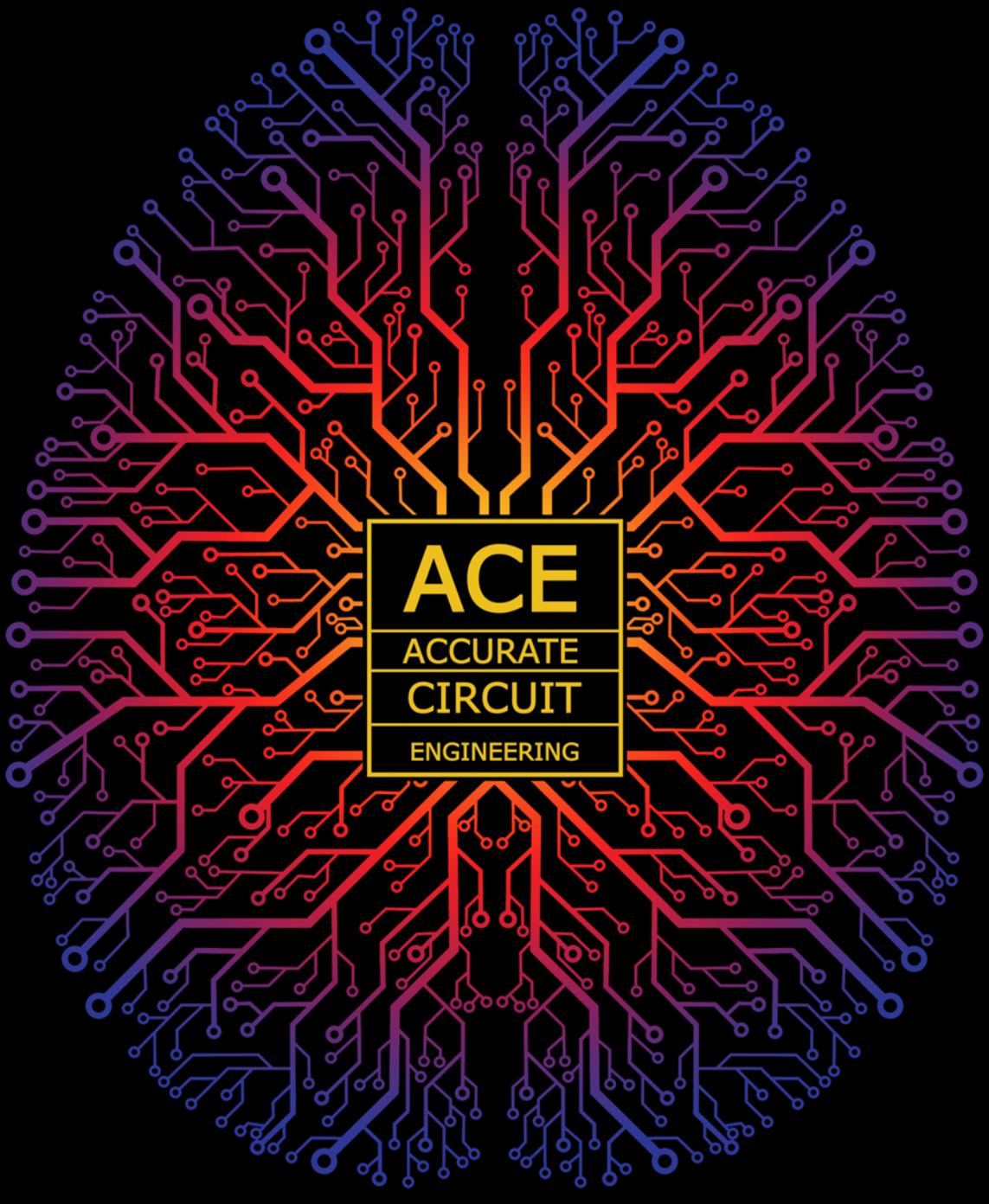
The library management of footprints, land patterns, or cells—however you refer to them in your ecosystem—is one of the most critical items in the foundation of any PCB or CCA design. When I was asked to write an article on this topic, so many thoughts and experiences instantly flooded my mind. After 30+ years of designing PCBs throughout the industry, I have my share of experiences and stories about footprints.

One particular experience stands out—a project that I consulted on several years ago. My friend Vino asked if I could support a project that he was about to kick off. I said sure, as I had worked with him many times before. We discussed the initial PCB layout details, and we noted the extremely tight, aggressive schedule he was up against.

As we were planning our attack, the topic of library part creation came up, as usual. But this time, Vino wanted to farm out the library efforts to a third-party company that was unknown to me. I voiced my concerns about using this resource, and the importance of library parts being accurate and correct. Vino assured me that we'd be okay because this company came with high recommendations from a trusted source. I trust Vino, so a few meetings later, everything was put into motion.

The design at hand was a small, complex backplane card targeted for the end-product to go to a data center customer. The PCB measured 8" x 3." It had 14 layers, 0.062" thick, with about 1,000 parts, and eight cluster modules containing 2 x 2.5 Gbps per link on each of these modules. This is a high-speed digital design, with around 40 Gbps data rates and very fast edge rates. It also featured two additional daughter cards, two network switches and a backplane controller BGA consisting of several hundred pins. The team worked like crazy and hit all the initial targeted phase gates within the project schedule. After lots of analyses done on the design, including a final DFM check, the design went out for fabrication as scheduled, with no apparent issues. Happy ending! Or was it?

Don't Overthink Your Prototype Builds



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About four weeks later, I was at the office when Vino called my cellphone. I answered, expecting to hear some early success of initial testing of the assembly. But I knew something was wrong from the tone of his voice. "Steph, I need your help!"

My heartbeat quickened. Vino proceeded to tell me that upon powering up the CCA, it got extremely hot within a few seconds, especially the backplane controller BGA. He had already powered up two of the five CCAs we had built, and each had this similar issue. We scrambled, discussing possible issues that caused the overheating.

It was difficult to assess this issue, since I was at the office and didn't have my personal laptop that contained the PCB design. (I always use my personal laptop for consulting.) Within a few minutes of our discussion, a bad feeling hit me like a ton of bricks. While Vino was describing what he was checking, I ran back to my desk and grabbed my business laptop. I asked him to provide the part number for that backplane controller. I downloaded a PDF of the manufacturer's datasheet and jumped to the page that contained the BGA footprint details. I asked Vino to tell me where Pin 1 was identified on the actual part that was placed on the CCA, knowing that the part was placed on the secondary side of the design. Then, I asked him to tell me where the Pin 1 markings were located on the PCB itself. He told me where Pin 1 was located on the PCB and that it also aligned with the part alignment markings on BGA, so I asked him to open the design.

That very second, as we compared the footprint in the design to the footprint in the datasheet, we realized that our fate was sealed. We both knew the cause of our overheating: the footprint was designed incorrectly. It was designed as if you were looking through the board: basically backward. You can imagine the amount of F-bombs that were dropped by both of us as we combed through the manufacturer's datasheet while triple-verifying the error, to no avail. We confirmed the worst-case scenario: a catastrophic mistake with no possible chance of salvaging the five CCAs.

What happened? The librarian from the third-party resource created the footprint manually and simply missed the one detail in the manufacturer's datasheet located under the image of the footprint that stated in a large, bold font, "Viewed from Bottom Side of Device." This was also missed by the individual who validated the part for release into the library. This one missed detail caused the footprint to be designed with the entire pin sequence 180° off. Devastating mistake with no potential of recovery? There was no choice in this case but to make the footprint correction in the library, redesign a major portion of the board and re-spin the board.

The ripple effect of such a mistake: Each CCA cost over $5,000 to fabricate and assemble. There were five total assemblies with very little parts remaining due to limited funding and extremely long lead time on some of the ICs and connectors. Figure 1 shows a photo of one of the bad CCAs.

The immediate follow-up meeting with the third-party library team was not pretty, to say the least. We had to deal with a missed scheduled window of marketing opportunity, additional unexpected cost, additional time to redesign and re-spin the board, and a very negative hit on our reputations. The rhetorical question is this: What is the true cost of this mistake?

And what is the lesson from this experience? Attention to detail is paramount in PCB design, especially when it comes to creating library parts. In my opinion, a good librarian is worth their weight in gold. You can do due diligence in circuitry design, design layout, signal analysis, and DFM, but if your library parts are not accurate, your CCA design may have a catastrophic ending.

Can this type of error be prevented? Absolutely. Whether a footprint is created manually or with any of today's third-party automated library creation tools, attention to detail is key. I would even go one step further and suggest

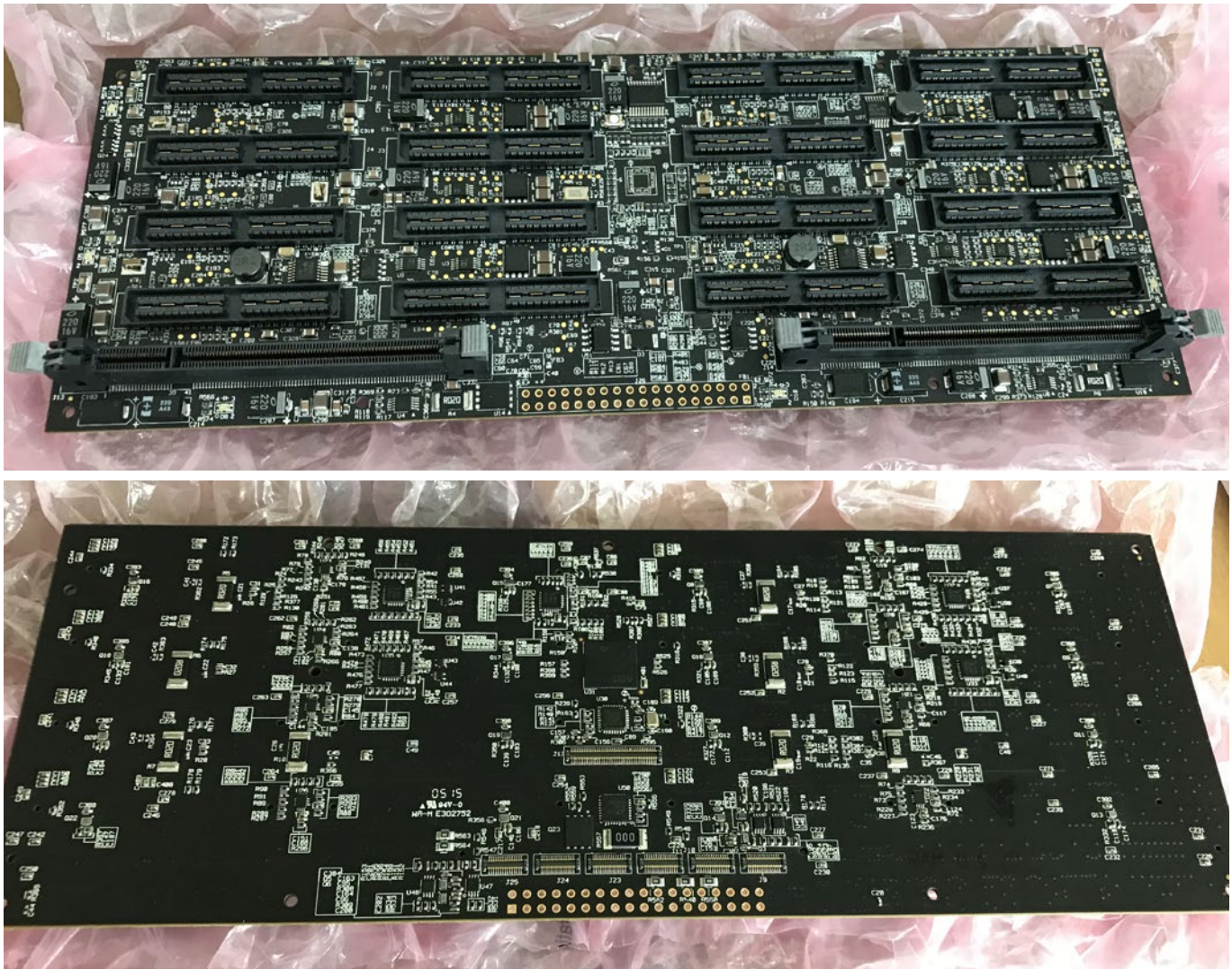

Figure 1: Photos showing the top and bottom of the CCAs that overheated due to a simple footprint error. Note the backplane controller BGA in the center of the bottom side of the board; this one CCA represents $5,000 out the window.

that a DFM check should be done at the library level using any of today's industry tools, such as Siemens' Valor VPL.

A DFM check and verification of a footprint for both fabrication and assembly should be done as early in the design process as possible. When done at an early stage, a design will have a higher percentage of success right out of the blocks, with no potential missed footprint design errors to worry about. A bad pin can easily be identified within seconds utilizing such a tool. A thorough DFM check between the 3D industry model of the component against the designed footprint, along with the appropriate solder fillets and overall assembly concerns, can also be quickly addressed to prevent downstream issues as well. This is what we now refer to as a shift-left approach.

In this design, no assembly DFM verification was ever performed. The board was redesigned successfully. Vino worked out the financial compensation with that third-party library team, but it was the last and only time Vino and I used them. **DESIGN007**

Stephen V. Chavez, MIT, CID+, is chairman of the Printed Circuit Engineering Association.

Stackup Configurations to Mitigate Crosstalk

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Crosstalk arises because of the unintentional coupling of electromagnetic fields. The current trend is toward smaller, faster boards with lower IC core voltages. But, as the supply voltage drops from 3.3V to 1.5V, the allowable noise margin is more than half. Also, the closer parallel trace segments are spaced, due to limited real estate, the greater the chance of coupling. The reflections created by crosstalk erode the noise margin. We cannot eliminate crosstalk, but as PCB designers it is our job to ascertain how to control and manage the predicted interference.

Crosstalk is three dimensional and dependent on the signal trace separation, the trace to plane(s) separation, parallel segment length, the transmission line load, and the technology employed. But crosstalk also varies depending on the physical stackup configuration. In this month's column, I will delve into the properties of microstrip and stripline crosstalk and how to mitigate the concern.

Crosstalk can be induced by the following stackup configurations as illustrated in Figure 1:

1. Microstrip edge coupled
2. Stripline edge coupled
3. Dual stripline broadside coupled
4. Dual stripline broadside-edge coupled

The first two edge coupled configurations are well known—and for good reason—they are also commonly used for differential pairs. Close coupling is good for maintaining impedance, rejecting noise and avoiding slew, but not good for crosstalk. The other two configurations are broadside coupling, which has many disadvantages: the main one being layer-to-layer registration during fabrication. IPC Class 3 specifies ±2 mil registration between any two adjacent layers but it may be more like ±4 mil for a combination of layers nudging the impedance way out. Also, broadside coupling requires a very thick dielectric material

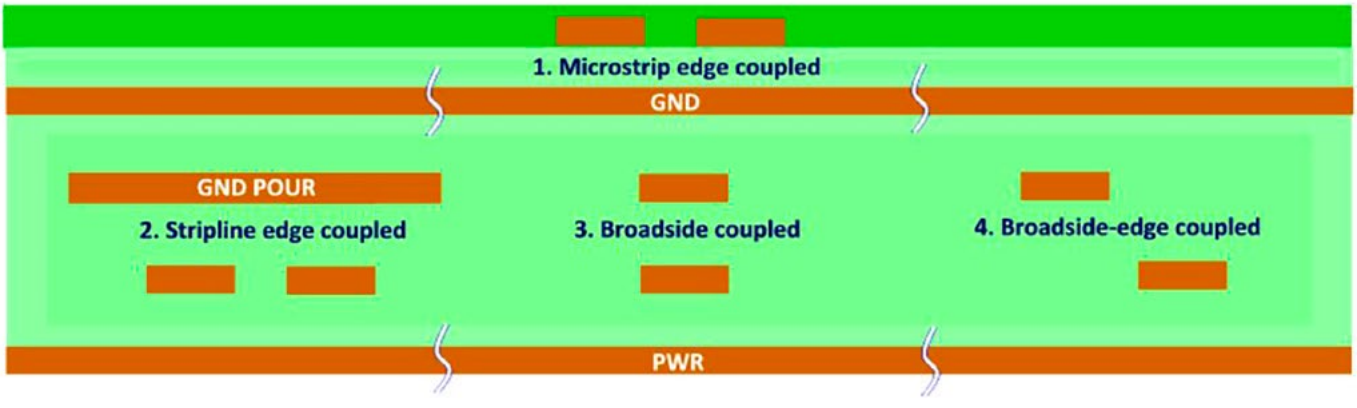

Figure 1: Crosstalk stackup configurations.

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between adjacent signal layers which will generally render the substrate too thick. On the plus side, it can be a good solution for navigating a connector pin array, maintaining impedance with no reference place. Broadside-edge coupling requires less dielectric thickness but is very difficult to predict the impedance due to alignment issues. Impedance aside, any coupling of unrelated signals should be avoided.

There are two types of crosstalk: forward and reverse. These are also termed far-end (FEXT) and near-end (NEXT) crosstalk, which refers to where the crosstalk is measured—at the load or the receiver, respectively.

Interestingly, there is a unique property of the stripline configuration in that the ratio of mutual capacitance (*Cm*) equals that of the mutual inductance (*Lm*) which cancels out the forward crosstalk (*Kf*) component (equation 1). Whereas reverse crosstalk (*Kb* in equation 2) is the addition of the two, consequently it is always present to some degree.

equation 1

Forward crosstalk (FEXT) $$Kf = 0.5\left(\frac{Cm}{Ctotal} - \frac{Lm}{Ltotal}\right)$$

equation 2

Reverse crosstalk (NEXT) $$Kb = 0.25\left(\frac{Cm}{Ctotal} + \frac{Lm}{Ltotal}\right)$$

Figure 2 shows the near- and far-end crosstalk for a microstrip configuration where the victim traces are adjacent to the aggressor trace (1.5V @ 1GHz). In this case, the traces are 4 mils wide, 40 ohms impedance with a 4-mil spacing. Crosstalk falls off rapidly with

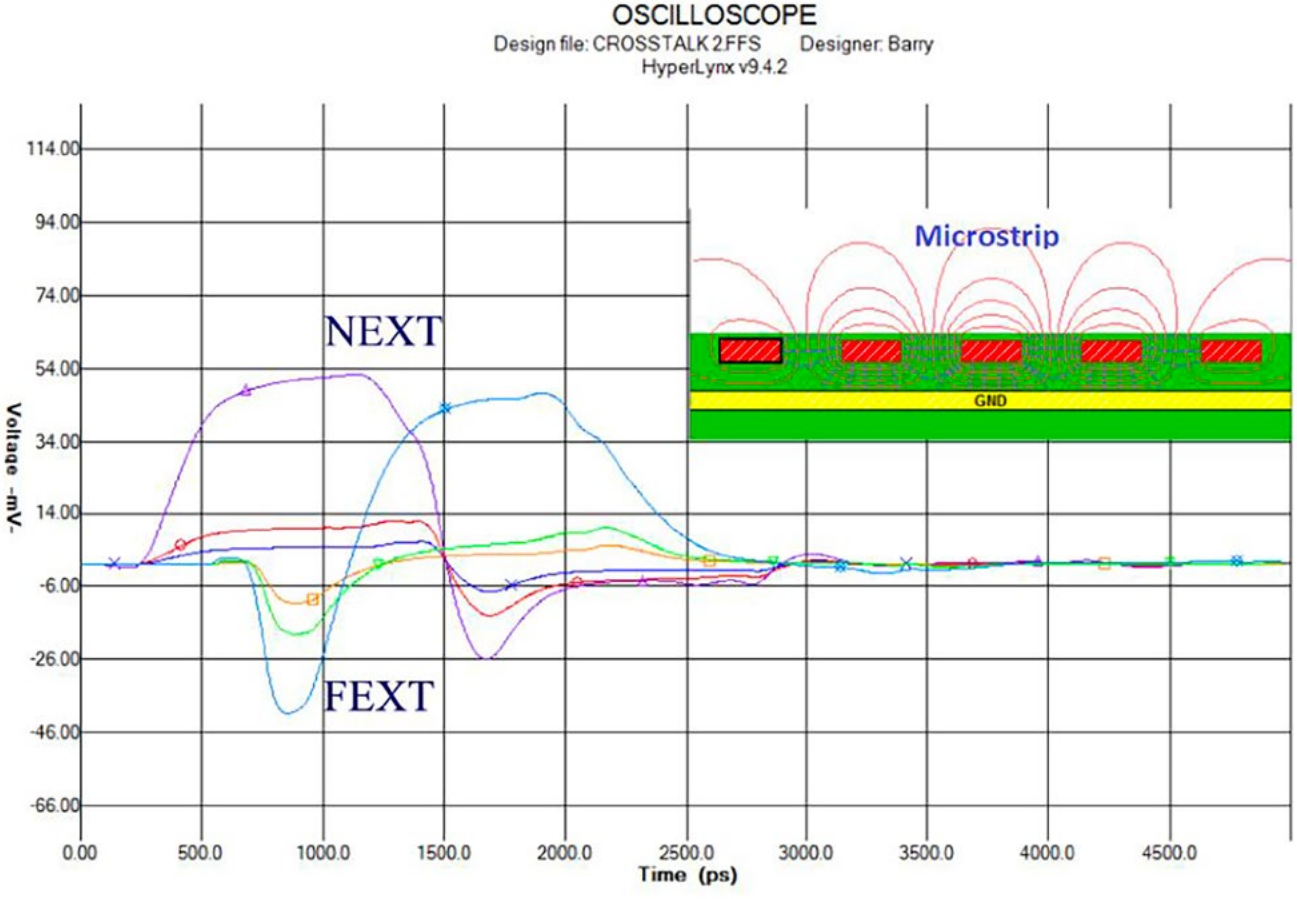


Figure 2: Near- and far-end crosstalk for microstrip with 4/4 mil trace width/clearance.

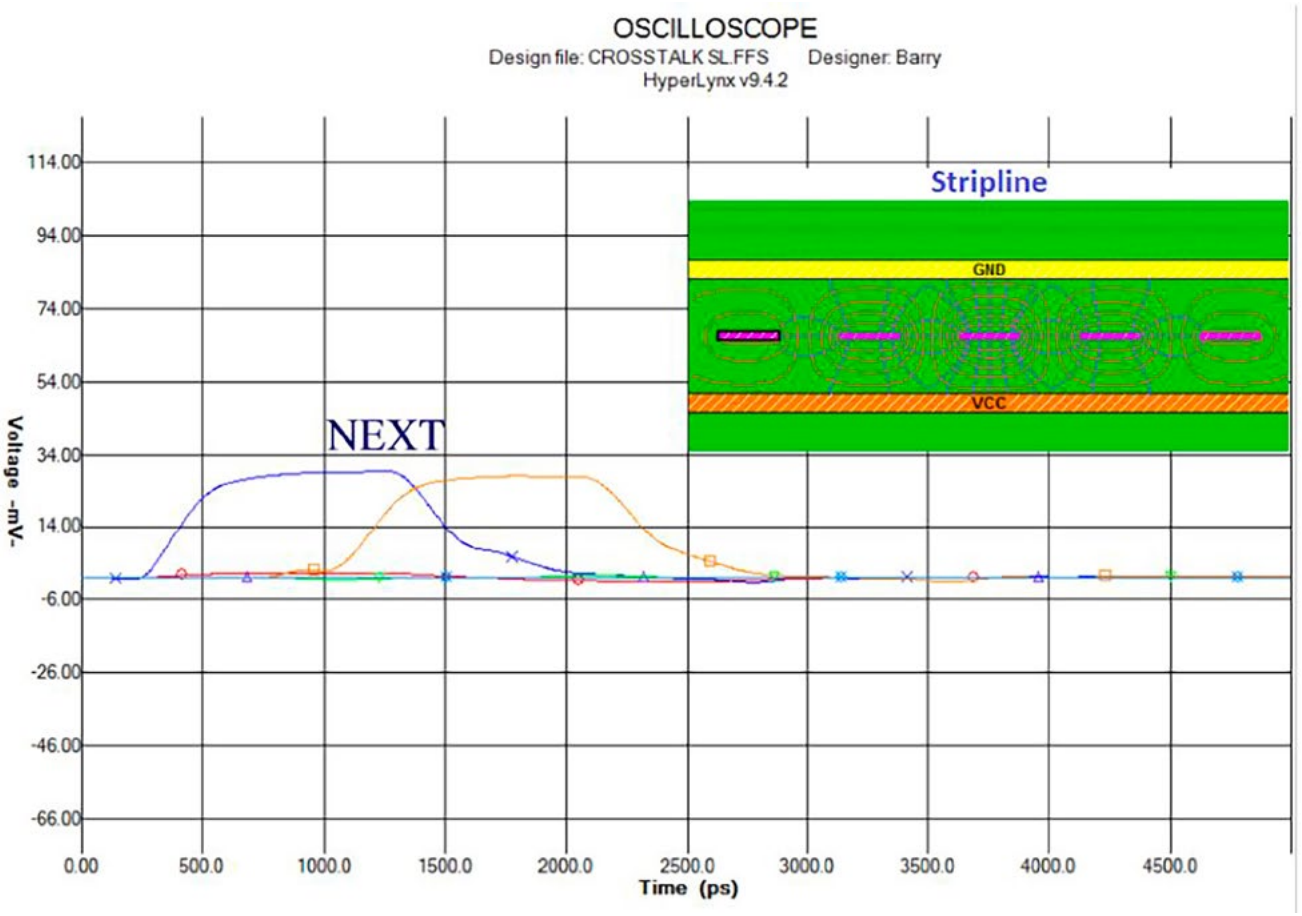


Figure 3: Crosstalk for stripline with 4/4 mil trace width/clearance.

the square of the distance and the degree of impact is related to the aggressor signal voltage, the proximity of trace segments, and proximity to the plane(s).

In an outer layer microstrip configuration, the mutual capacitive coupling between adjacent traces is generally weaker than the mutually inductive coupling, driving the FEXT co-efficient negative, as can be seen in the simulation. However, forward crosstalk does not exist in the stripline configuration. The fine balance between inductive and capacitive coupled crosstalk produces almost no observable forward crosstalk (Figure 3). This shows the near-end crosstalk of a stripline configuration for 4 mil wide, 40 ohms impedance traces with a 4-mil spacing. Notice how there is no FEXT component of the noise. Also, the peak amplitude of the crosstalk has been considerably reduced. All other factors being equal, here is just another good reason why one should always route high-speed signals on the inner layers of a multilayer PCB. Stripline edge coupled signals can also be placed closer to each other compared to the microstrip equivalent leaving more space for routing, which is always welcomed.

The easiest way to reduce crosstalk from a nearby aggressor signal is, of course, by increasing the spacing between the signals in question. Crosstalk falls off very rapidly with distance. Crosstalk plummets roughly quadratically with increased separation. By doubling the spacing, it cuts the crosstalk to roughly a quarter of its original level. A good rule of thumb for this is Gap = 3X trace width. However, in today's complex designs it is not always possible to use up valuable real estate to satisfy the above. Also, different technologies should not be mixed as higher voltages create

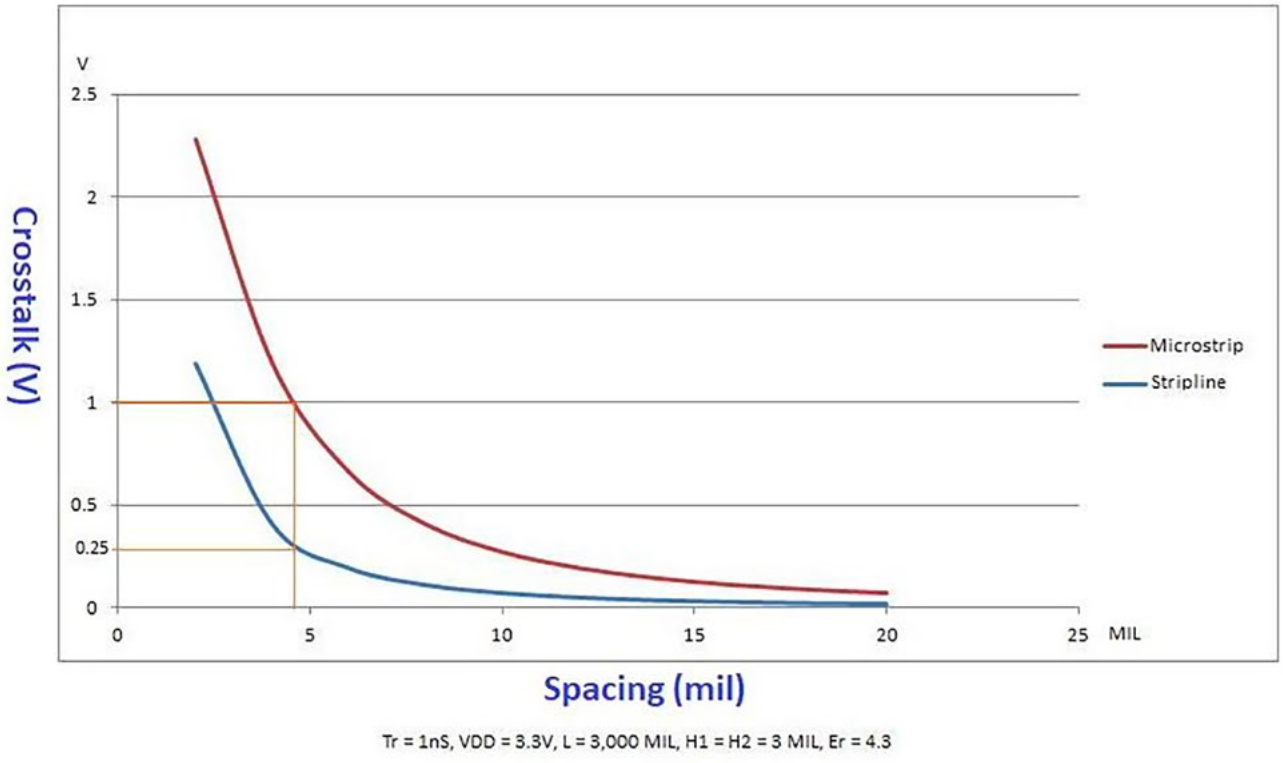


Figure 4: Crosstalk vs. trace spacing (edge coupled).

higher crosstalk. And long parallel trace segments should be avoided.

Figure 4 shows the effect of the edge coupling on the crosstalk for both microstrip (outer layers) and stripline (inner layers). Note that the stripline has about one-quarter the crosstalk of the microstrip. Also, microstrip crosstalk tends to radiate from the outer layers of a multilayer PCB whereas stripline confines the EM fields between the planes.

Crosstalk also depends on the load which may vary considerably when driving banks of memory modules, for example. Keep in mind that the total crosstalk on each victim trace is the total crosstalk from each of several nearby aggressors, all of which sum up to produce the maximum value.

Both forward and reverse crosstalk can be arbitrarily reduced by separating the aggressor(s) from the victim trace(s) or by reducing the height of the dielectric above/below the planes. The latter also requires a reduction in trace width to maintain the impedance. If real estate is a premium, as it generally is on dense, high-speed designs, then routing on the inner layers and avoiding broadside coupling may be good solutions.

Key Points:

- Crosstalk is three dimensional and is dependent on the signal trace separation, the trace to plane(s) separation, parallel segment length, the transmission line load, and the technology employed
- Crosstalk also varies depending on the physical stackup configuration
- Close coupling is good for maintaining impedance, rejecting noise and avoiding slew, but not good for crosstalk
- Far-end (FEXT) and near-end (NEXT) crosstalk refer to where the crosstalk is measured—at the load or the receiver, respectively
- A unique property of the stripline configuration is that the ratio of mutual

capacitance equals that of the mutual inductance, which cancels out the forward crosstalk component
- The peak amplitude of the stripline crosstalk is considerably less than microstrip
- Stripline edge coupled signals can also be placed closer to each other compared to the microstrip equivalent leaving more space for routing
- The easiest way to reduce crosstalk from a nearby aggressor signal is by increasing the spacing between the signals in question; crosstalk falls off very rapidly with distance
- Different technologies should not be mixed as higher voltages create higher crosstalk
- Long parallel trace segments and broadside coupling should be avoided
- The stripline configuration has about one-quarter of the crosstalk of the microstrip for the same spacing **DESIGN007**

Resources

1. Beyond Design: Controlling the Beast, by Barry Olney.
2. *Trace Design for Crosstalk Reduction*, by Scott McMorrow, Samtec.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns or contact Olney, click here.

Brain-to-Brain Communication Demo Receives DARPA Funding

Wireless communication directly between brains is one step closer to reality, thanks to $8 million in Department of Defense follow-up funding for Rice University neuroengineers.

The Defense Advanced Research Projects Agency (DARPA), which funded the team's proof-of-principle research toward a wireless brain link in 2018, has asked for a preclinical demonstration of the technology that could set the stage for human tests as early as 2022.

"We started this in a very exploratory phase," said Rice's Jacob Robinson, lead investigator on the MOANA Project, which ultimately hopes to create a dual-function, wireless headset capable of both "reading" and "writing" brain activity to help restore lost sensory function, all without the need for surgery.

Jacob Robinson

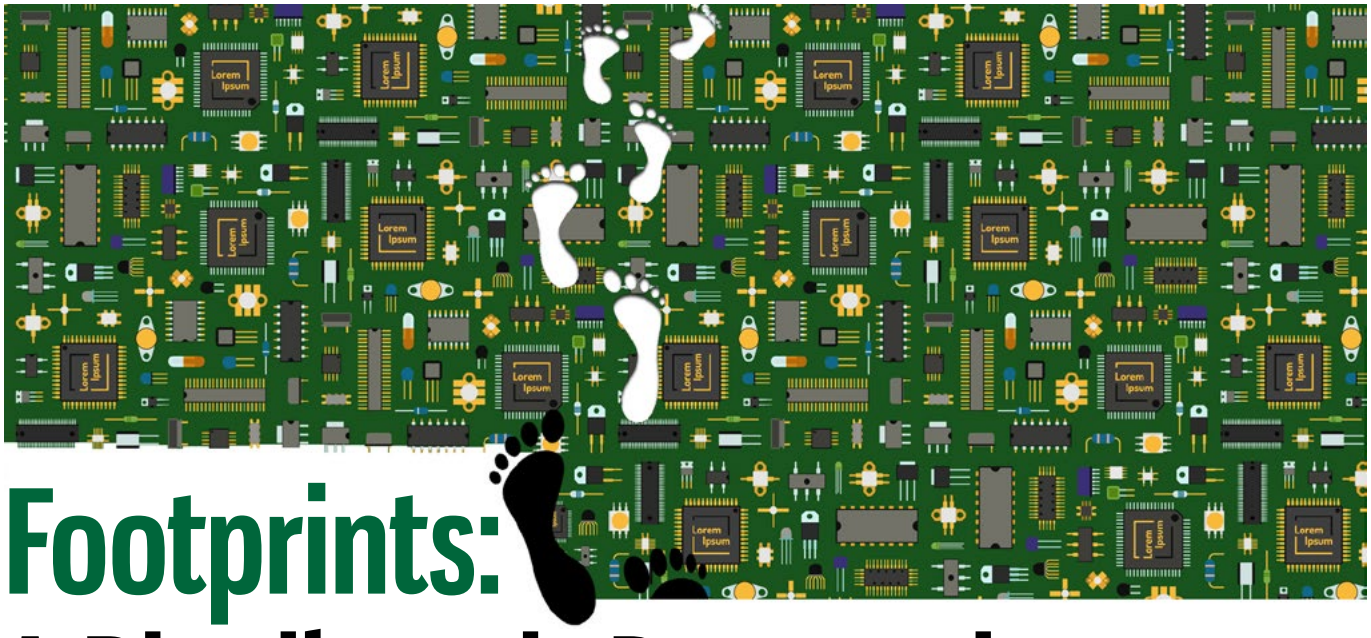
MOANA, which is short for "magnetic, optical and acoustic neural access," will use light to decode neural activity in one brain and magnetic fields to encode that activity in another brain, all in less than one-twentieth of a second.

If the demonstrations are successful, he said the team could begin working with human patients within two years.

"Most immediately, we're thinking about ways we can help patients who are blind," Robinson said. "In individuals who have lost the ability to see, scientists have shown that stimulating parts of the brain associated with vision can give those patients a sense of vision, even though their eyes no longer work."

The project is funded through DARPA's Next-Generation Nonsurgical Neurotechnology (N3) program.

(Source: Rice University)



Footprints: A Distributor's Perspective

Feature Interview by Andy Shaughnessy
I-CONNECT007

No issue on footprints and library management would be complete without input from a component distributor. I recently interviewed Geof Lipman of Octopart; as director of operations for part data, he's one of the brains behind the entire site. Geof explains how Octopart functions and manages millions of component data points, and he also discusses the current landscape of electronic components.

Andy Shaughnessy: Geof, give us a quick background on how Octopart operates.

Geof Lipman: Absolutely. We aggregate and curate data about electronic components from hundreds of distributors and thousands of component manufacturers. We use a combination of approaches to acquire data. Some of our intake is highly automated, which results in us having the most comprehensive and up-to-date marketplace information in the industry.

Other data types need to be evaluated, and classified or normalized. ECAD data like footprints, 3D models and schematic symbols need to be built. We have teams of electrical engineers who ensure the quality and completeness of these types of data. We provide ECAD models for over 1 million parts, supporting multiple popular formats, footprints, schematic symbols, and 3D models.

Shaughnessy: What sort of data do you provide your customers when they search for a component?

Lipman: Broadly speaking, we supply marketplace data, lifecycle status, datasheets and other manufacturers' documents, compliance data, technical specifications, free ECAD models, similar parts, and alternate names and MPNs for about 40 million parts.

For instance, marketplace data provides customers with answers to these questions: How much does it cost? What are the price breaks for quantity? How many are in stock? Who has the stock? What is the current typical lead time? We provide a "freshness indicator" so that our customers can see how long ago this marketplace data was updated.

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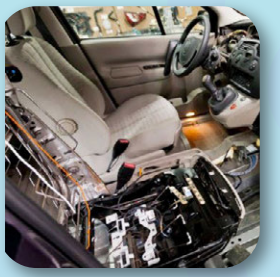
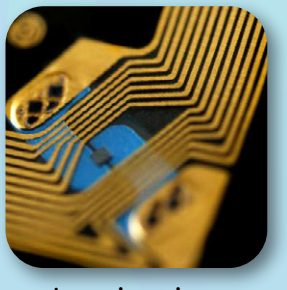


Automotive Electronics



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The lifecycle status information tells you if the part you are specifying is likely to be hard to get or obsolete when you go into production. We provide a "freshness indicator" here too, so that our customers can see how long ago the lifecycle data was updated.

Geof Lipman

We provide two "flavors" of lifecycle status: The "Manufacturer Lifecycle Status" is exactly what the manufacturer says—no more, no less; and the "Lifecycle Status" is a composite spec summarizing all the lifecycle data that we have on a part. This could be from both the manufacturer and several distributors, for example.

Datasheets and other manufacturer documentation are probably the most critical technical documentation on a part, describing its functionality in detail. The compliance data (as provided to us) helps customers determine whether that part can be used in the jurisdictions where they want to sell the product, including RoHS, REACH, and conflict mineral regulation compliance.

Shaughnessy: Since you deal with customers around the globe, why don't you share some of the trends you're seeing in electronic components.

Lipman: There are several ways to talk about the trends that we can measure; it all depends on how you slice the data. As far as demand, in terms of popularity, we've seen increased interest in SMD chip resistors when we look at the total number of views by category in 2020. Compare this to 2019 where ceramic capacitors took the top spot in terms of raw views. Connectors are another category that saw a significant increase in the amount of user interest. We're calling this our "most improved" category for 2020 as we saw a 21% jump in engagement in this category compared to the previous year.

Looking at the types of parts being added to the site by our partners, we see that power products and discrete semiconductors had a big jump in the number of components added to those categories in 2020 vs. 2019. In terms of volume, however, passives continue to have the most components added compared to other categories.

As for what this might mean for the industry more broadly, we like to avoid drawing those kinds of conclusions from our data. While we have a very broad and central view of the component landscape, there are so many factors—political, economic, just to name a few—that can impact behavior on our site, and we never want to put out information we can't confidently validate.

Beyond the activity on Octopart, we continue to see consolidation among component manufacturers, and we expect this trend to continue for a while.

Shaughnessy: What is your typical customer looking for?

Lipman: Purchasers are looking for inventory and pricing for immediate purchase. Our site gives an instantaneous view of the entire industry and provides access to part risk data and BOM tools, which makes it easy to manage orders and optimize purchasing and shipping for cost and schedule.

Engineers are researching parts to include in their BOMs. Engineers know that electronic components need to be optimized in more ways than simply for performance. This includes market availability and pricing research, as well as possible alternate parts to make their designs more resilient to supply chain variations. Engineers are also leveraging our ECAD

models (schematic symbol, footprint, and 3D model) to speed up their design process.

Makers come to Octopart to find ideas for projects, conduct research, compare parts, and find the most economical way to acquire parts in small quantities. This includes using our BOM tool, which makes it easy to consolidate your BOM into your preferred distributors, thus reducing shipping costs. Hackers like our API because you can use it on projects for free. Makers also use our ECAD models a lot to save time and effort.

Shaughnessy: What are your customers' biggest issues related to footprints and ECAD?

Lipman: Although there are a number of companies that promise high-quality ECAD models in their marketing materials, engineers with money and careers on the line cannot trust the majority of free ECAD models. Engineers understand that symbols must be of high quality. Schematic diagrams exist to transmit understanding, and so engineers have devised symbols that have been in use for nearly 100 years to convey this understanding. ECAD symbols need to comply with this tradition, and with sensible standards in the field.

Footprints should follow the manufacturer's recommendations. For standard package type parts, IPC-7351 standard footprints should also be provided. 3D models should follow a simple rule. They should look like—and be the same size as—the actual part. And the best 3D part is "photorealistic," or at least has the right colors and shapes.

Every part we build comes with a schematic symbol, PCB footprint, and 3D model. Every schematic symbol looks like it should, following the guidelines of IEEE 315-1975 and IEC 60617. We provide footprints that follow the manufacturer's guidelines, and when standard packages are used, we also supply three IPC-7351-compliant footprints for different PCB densities. Every part is checked three times by electrical engineers before we release it as a "verified" model. And we do not release unverified models.

Shaughnessy: Do you have any advice for designers who are having trouble with footprints?

Lipman: Sure. Your best resources for help with footprints are:

1. The manufacturer's datasheet or land pattern drawing.

In most cases, a manufacturer will have tested their parts with the land patterns in their technical documentation. That makes this a primary starting point for any footprint design. If you have a specialized use that involves tight geometries, close component spacings, or challenging thermal aspects, check with the manufacturer for literature or other advice about how to optimize your footprint for your application.

2. IPC-7351B.

This IPC standard lays out equations for land pattern geometries that are optimized for manufacturing. This can be especially helpful if you cannot find any documentation for a part. In most cases, the manufacturer's recommendations and the IPC recommended footprint are very similar.

3. Your PCBA assembly provider.

Your PCBA assembly professionals are experts in their machines and processes. It is common to submit designs to the assembly house before production so that they can discover any issues and recommend remediations. Similarly, during design, you should be able to reach out to them to get recommendations for particular parts.

Shaughnessy: Sounds good, Geof. Thanks for your time.

Lipman: Thank you, Andy. **DESIGN007**

Circuit Material Library Considerations

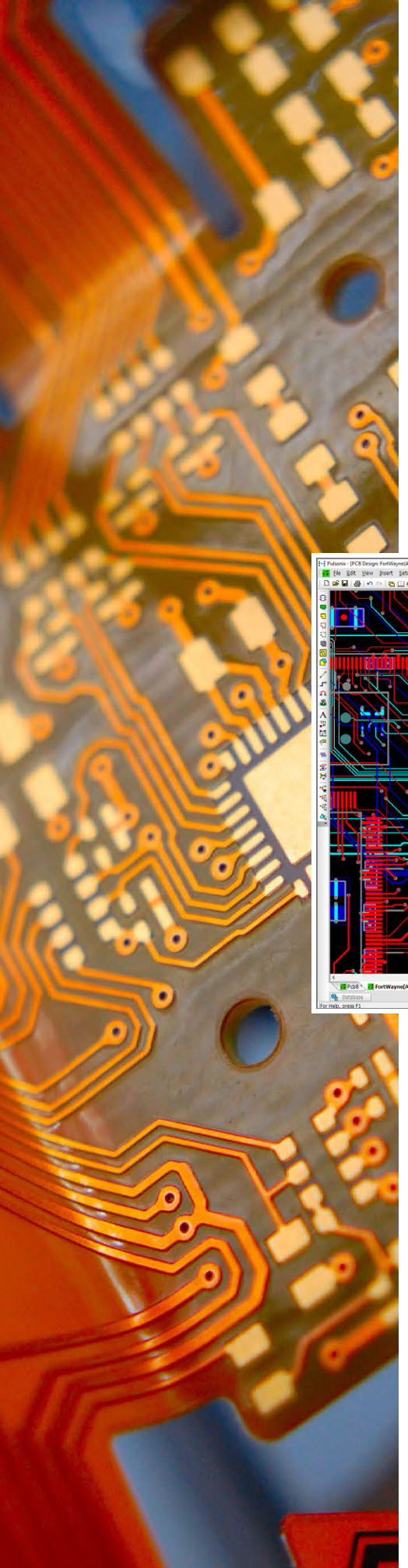
Lightning Speed Laminates

Feature Column by John Coonrod, ROGERS CORPORATION

There are multiple libraries of information nowadays for a PCB fabricator. A circuit material library for the fabricator can be advantageous for multiple reasons. Sometimes these libraries are intended to be used for electrical predictions, such as impedance, insertion loss or other issues. Other times the information found in the circuit material libraries are used to assist with thermal issues, potential reliability concerns, circuit construction stackups, and some processing issues.

When a PCB manufacturer is creating and building a circuit materials library, there are some property values which should be defined by the circuit fabricator while other property values should be obtained from the circuit material supplier. As general statements, the circuit material property values which can be affected by the PCB fabricator should have data that was collected by the fabricator using their specific processes. The circuit material properties which are unaffected by circuit fabrication can be obtained from the circuit material supplier.

The common circuit material properties which can be affected by the fabricator are related to some of the electrical evaluations which the circuit manufacturer performs. It is common for a PCB supplier to perform impedance testing on the final circuit, as a "go/no-go" test for shipping the product. The material properties which relate to impedance are dielectric constant (Dk), substrate thickness, and copper thickness. Most PCBs today are using plated through-hole (PTH) technology, which means the final and overall copper



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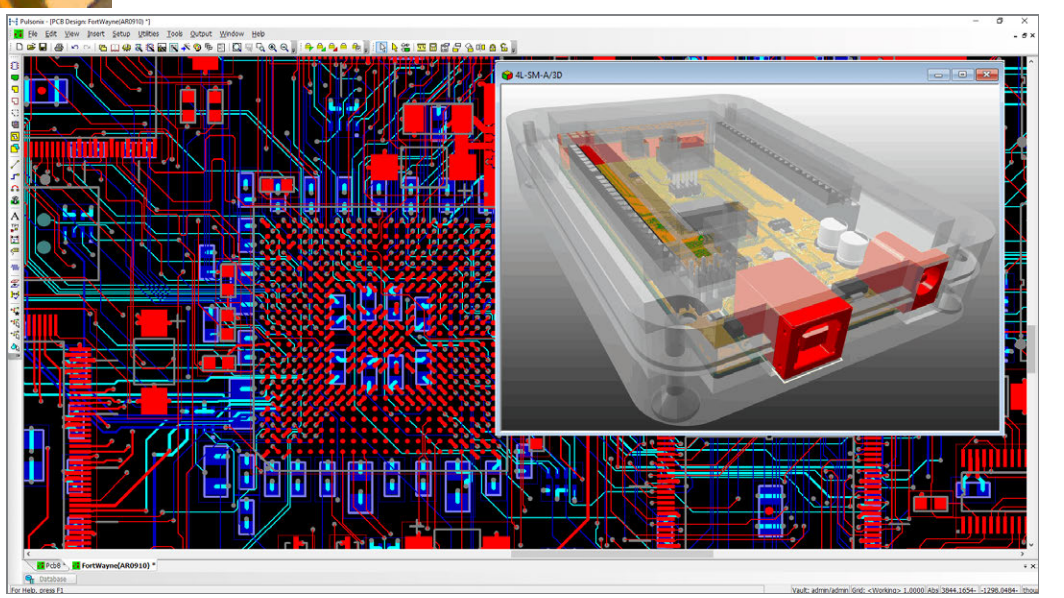

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thickness of the circuit can be influenced by the PCB fabrication process. The substrate thickness issue depends on the circuit construction, and in the cases of a foil lam construction, the thickness control is influenced somewhat by the PCB fabricator.

The Dk of the material is relatively fixed by the material supplier, however for some materials there can be a slight alteration of the Dk value due to material interaction with certain PCB processes. With these considerations in mind, the PCB fabricator should do studies with these variables, using a circuit material of choice, to define data which can be used in the material library for impedance modeling. The circuit material library will have data that is tailored to the circuit material being processed at that specific PCB fabricator.

The circuit material supplier can certainly assist by giving the fabricator more detailed information for the material properties, as the material is tested at the supplier using the material supplier's test method. Many of the high frequency circuit material suppliers use the IPC-TM-650 2.5.5.5c test method to report Dk at 10 GHz. This test method is a raw material test and is not affected by circuit fabrication. As an example, the IPC test method uses a clamped fixture and there is some amount of entrapped air to be expected. The entrapped air has a very small effect, but air does have a Dk of about 1. The reported Dk with the clamped test method will often be lower than if the material is tested in circuit form without entrapped air.

Another reason for the PCB fabricator to build their database based on their process is the fabricator will often have a choice of what copper foil to use in a foil lam construction. The bond surface of the copper foil, and specifically the roughness of that surface, can impact the "circuit perceived Dk" or as Rogers Corporation calls it, design Dk. Again, with the PCB fabricator having the ability to alter the circuit performance due to the choice of copper foil, they should be defining the Dk values used per their process and with the copper they use.

The properties which the circuit material library should use from the material supplier are typically things like CTE, T_g, peel strength, moisture absorption, thermal conductivity, etc. These properties are innate to the material and they are typically not affected by the PCB fabrication process. Peel strength could be the exception on this list, where certain PCB processes can cause this property value to change. Peel strength (or bond strength) may be a good property value for the fabricator to gather information from the material supplier and then perform their own study and compare results with the material supplier.

When using data from a material supplier, the PCB fabricator should be very familiar with the test methods used by the supplier. A noteworthy example would be the material property of thermal conductivity. Thermal conductivity can be determined by several different test methods and the results may or may not be appropriate for how the circuit fabricator will apply the data. One test method for thermal conductivity used for laminate evaluations will include the effects of copper. A different test method will not include the effects of the copper. Since copper has a very high thermal conductivity, the influence of copper can make the results significantly different when comparing these two test methods for an evaluation of the same laminate. Depending on how the PCB fabricator will use the thermal conductivity information, they may or may not want to have the copper effects included.

It is always good advice for the PCB fabricator to work closely with the material supplier and that is especially true when the fabricator is developing a material database. **DESIGN007**

John Coonrod is technical marketing manager at Rogers Corporation. To read past columns or contact Coonrod, click here.

MilAero007 Highlights

Defense Speak Interpreted: Your Best Friend is a Skyborg? ▸

Suddenly the term "Skyborg" is popping up in Air Force publications, and if you are an Air Force pilot, your future best friend may be a Skyborg. To understand the concept behind the term Skyborg, we need a bit of weapons strategy for the Air Force.

Book Excerpt: Thermal Management with Insulated Metal Substrates, Part 5 ▸

The following is an excerpt from Chapter 5 of "The Printed Circuit Designer's Guide to... Thermal Management with Insulated Metal Substrates," written by Ventec International Group's Didier Mauve and Ian Mayoh. In this free eBook, the authors provide PCB designers with the essential information required to understand the thermal, electrical, and mechanical characteristics of insulated metal substrate laminates.

TT Electronics, Thales Join Forces to Enable Future Development of Cybersecurity ▸

TT Electronics, a global provider of engineered electronics for performance critical applications, has announced a collaboration agreement with Thales to enable future development of operational technology (OT) based cyber security initiatives and research.

IPC Praises U.S. Government Actions to Bolster Security and Resiliency of Defense Electronics Supply Chain ▸

This is a statement by Chris Mitchell, vice president of global government relations at IPC, the global electronics manufacturing association, on recent actions by the U.S. government to bolster the security and resiliency of the U.S. defense electronics supply chain.

Arcline Investment Management Acquires Ohmega Technologies ▸

Arcline Investment Management, a growth-oriented private equity firm with $1.5 billion of committed capital, announced that it has expanded its specialty electronic components platform with the acquisition of Ohmega Technologies, a leading manufacturer of advanced embedded thin-film resistive materials.

Ventec Strengthens Canada OEM Activities with Appointment of Sigma Component Design ▸

Ventec International Group Co., Ltd. has announced the appointment of Sigma Component Design (Sigma) to provide sales and support to OEM customers in Canada. The two companies have signed a contractual agreement under which Sigma will help drive new OEM business for Ventec in Canada and represent all product lines from 1st January 2021.

Elbit Systems Awarded $24M Contract to Supply Tactical Computers for Royal Netherlands Army ▸

Elbit Systems Ltd. was awarded an approximately $24 million contract from the Dutch Ministry of Defence (Dutch MOD) to supply the Royal Netherlands Army (RNLA) with new vehicular tactical computers. The contract will be performed over a 30-months period.

The Case for Expansive Parts Libraries

Connect the Dots

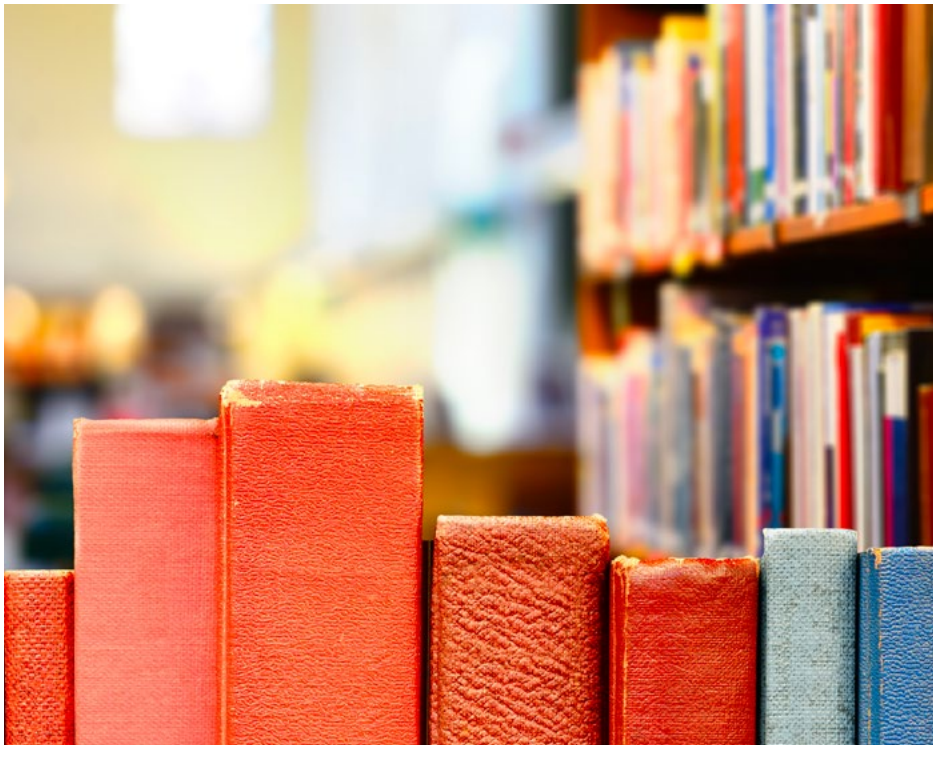
Feature Column by Bob Tise, SUNSTONE CIRCUITS

A large, reliable library of parts shortens design time and can eliminate costly errors.

My colleagues and I spend our days helping customers with their PCB designs. Much of our effort is directed at making functional improvements, speeding the prototyping process, or finding cost savings in a design. But we do a lot of problem solving, too: "Why did this blow up? How come nothing happens when I press the 'on' button?" Issues with specialized components are a common culprit.

PCBs are the foundation of every electronic device, the home for the components that make up your assembly. Those integrated circuits, connectors, headers, and passives are what make it function. How it needs to function determines whether standard components alone can make it work.

Specialized parts are often needed to make innovative electronic devices and that can create time-consuming challenges for the designer. Even though there are millions of parts available for your designs, custom or hard-to-find parts are sometimes needed. Finding the right one is a stubborn challenge for PCB designers. The average design team maintains a parts library with thousands of parts, but even the largest of those contain less than one percent of what's out there. That's why designers can spend as much as 35% of their design time on the laborious and error prone process of researching and creating specialized parts.



Larger organizations have librarians on staff who locate or fabricate components that reliably meet designer specs. Absent that resource, PCB designers are left to search for what they need or create custom components themselves.

Small Mistakes Can Lead to Big Problems

Your datasheet will usually provide what you need to locate the right part in a library, but those datasheets can be complex to the point of ridiculousness. Each part has a

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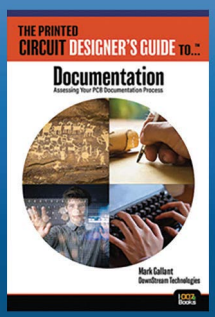

This book, written by Mark Gallant of DownStream Technologies, explains how an automated documentation solution like BluePrint-PCB® can eliminate post-processing errors and speed up time to market.

This book is a must-read for any PCB designers or design engineers who would like to adopt 21st-century PCB documentation processes.

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lot of information that describes it—things like pin functional names, pin numbers, manufacturer part number, and tolerances. That creates a lot of opportunity for error. There can be discrepancies between the component footprints and the datasheet—tiny things like pin spacing not carried out to the furthest necessary decimal point (on a 200-pin connector, this can add up!) or the symbol on the datasheet not specifying part orientation.

Since the process of researching a part and making sure it will not turn your board into ash is a laborious and unpredictable process, designers often choose to invest a few hours and just design a custom part themselves. They will have to navigate all the same landmines that come in the form of funky shapes, a unique size for desired functionality, or an inventive footprint. It is painstaking. You must translate every design element from the datasheet perfectly and it is hard not to miss something that will create problems.

Frying a board full of expensive components makes mistakes at this stage costly. So, if there is an easy way to avoid this risk and hassle, it makes sense to take advantage of it.

Keep Accurate, Pre-defined Parts at Your Fingertips

Expansive component databases will shorten PCB design time, reduce the need for rework, and avoid costly board failures. The more complete and accurate your parts library is, the better. We believe SnapEDA is the best solution to the custom parts challenge.

It's also one of, if not the easiest to use. With the ability to integrate the search and download functionality within the software, product manager Michael Hebda highlights the ease of use and simplicity of SnapEDA.

SnapEDA offers designers a massive, cloud-based electrical components database that includes a collection of specialized parts from many different manufacturers. With close to a million parts at the designer's fingertips, SnapEDA makes it much easier to locate a tested, proven component that meets your specs. SnapEDA's database is maintained by professionals dedicated to interfacing with component manufacturers, meticulously breaking down every detail of each technical datasheet and double-checking every piece of information made available.

Most of the CAD tools preferred by PCB designers—including Sunstone's free PCB123® design software—have third party plugins that allow you to quickly search SnapEDA and import parts you can rely on from their component database. This makes finding and integrating specialized parts into your design easier than ever.

Specialized parts don't have to be a challenge. Resources like the one illustrated here really can eliminate a lot of headaches for those of us who don't have a parts librarian on staff. Whether you choose SnapEDA or another parts library database, we encourage you to leverage cost-effective resources that will save time in the design phase and eliminate issues with specialized components during production. **DESIGN007**

Bob Tise is an engineer in PCB technical support at Sunstone Circuits. To read past columns by Sunstone or contact Tise, click here.

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Footprints—Small Steps with a Giant Impact

The Digital Layout
Feature Column by Kelly Dack, CIT, CID+, PCEA

Introduction

In this month's column, I celebrate the importance of the humble PCB component footprint. I suggest that creating and leaving positive professional footprints on all we do in the Printed Circuit Engineering Association is imperative to the success of the PCB industry. Next, I hand it off to PCEA Chairman Stephen Chavez to give us some inspiring words from PCEA as we tread into the new year. And as always, I'll provide our readers with a list of upcoming events.

PCEA Updates

Not a day goes by that I don't come across hundreds of footprints. They are not all related to electronic components used in PCB design. As you might imagine, around a cattle ranch, some are left on the property by turkeys, deer, cattle, and other outdoor critters as they go about their daily business of foraging for food in the snow. Some footprints are my own, which I make as I go about my daily business of taking care of outside chores. Sometimes I make "bad" footprints, tracking them into the kitchen if I fail to shed my muck boots in the mudroom before entering. I'd like to point out that these are hardly lasting footprints. They are made without much thought and quickly fade with the next snowfall or the wipe of a mop across the floor.

Lasting footprints are quite different.

Over 50 years have passed since Neil Armstrong made the first footprint on the moon, July 20, 1969. As he climbed down the ladder from the lunar landing module Eagle, and prepared to hop down onto terra Luna, he made the profound statement: "That's one small step for man, one giant leap for mankind." He took that step and made a footprint.

That iconic image of a footprint on the moon (Figure 1) represents so much more than someone going about their daily business. The footprints made by Neil Armstrong and Buzz Aldrin on the dusty surface of the moon at Tranquility Base represent millions of actions and pieces of information—data, people, machinery, and processes. They also represent their mission-critical project stakeholder, Michael Collins, who stayed back to pilot Apollo 11's spacecraft Columbia, and all those

Figure 1: Neil Armstrong's footprint on the moon.

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working behind the scenes at Mission Control. All aspects of the mission had to fit together perfectly to achieve a common goal of putting human footprints on the moon and returning to Earth safely.

Those of us working in printed circuit engineering know the importance of information and accuracy as it pertains to the footprints which are made to be placed—and forever remain—on the surface of our printed circuit boards. Component footprints must represent current, accurate information and feedback from all the PCBA's project stakeholders. Representatives from circuit engineering, mechanical engineering, supplier management, component manufacturers, suppliers of solder paste, solder stencils and all the personnel who are in the business of looking at, considering, or having to place and inspect a part of the component footprint must be represented within its geometric imprint on the surface of the PCB.

The Printed Circuit Engineering Association recognizes that people from all the realms of electronics must come together for printed circuit assemblies to work properly. We consider this our mission. Our goal is to make significant, lasting footprints on the face of the electronics industry through meaningful collaboration between our membership and the electronics industry overall. We seek to make giant leaps in educating our membership over the next few years to "dock" with new technologies coming from beyond the horizons. We hope our actions will leave lasting footprints on the surface of the entire industry, and which will serve to inspire those who come after us.

Message From the Chairman

by Stephen Chavez, MIT, CID+

January 2021 came and went. I feel it's a month that always seems to fly by very quickly. Most or all of us in the industry hit the ground running at the beginning of each year. With new aspirations or continued focus on attaining our respective short- and long-term goals, we come off the holiday break eager to get in the mindset and attack the new year with refreshed and rejuvenated minds. Each of us approaches January in our own individual way. Some start off with an aggressive attitude and game plan for success, others may be a bit hesitant or cautious in their approach to the new year, and some simply take it one day at a time as they let the new year unfold. Whichever way you start your new year, my advice is to go after it with passion and a positive attitude for success. I believe by doing this, we set the tone for the entire year. PCEA is doing just that.


Stephen Chavez

PCEA hit the ground running in January and by the time the month ended, we were in full stride; I feel we had set the tone for the new year. As we headed into February, we continued to accelerate our momentum of success. We are doing it with great passion and with the most positive attitude as possible. I see this by the great activity within PCEA: Our individual members, existing regional chapters and newly formed chapters, new chapters in their infancy stages, newly added sponsors (Polar, American Standard Circuits, and NCAB Group) with others in the works, and finally our internal PCEA Executive Board members all continue to have lots of excitement; the PCEA buzz is in the air.

Coming off a successful dual San Diego Chapter and Phoenix Chapter virtual event at the end of 2020, I was extremely excited to participate in our second multi-chapter virtual event in late January. The newly formed Minneapolis St. Paul Chapter, the Ontario, California Chapter, and the Greater Michigan Chapter held a successful tri-chapter virtual event, which was sponsored by American Standard Circuits. I highly recommend to any individuals in those respective local areas to get connected and involved with these local PCEA collectives.

As PCEA continues our core mission to Collaborate, Inspire, and Educate within the

industry, we are continuing to do our part to collaborate virtually with many in the industry while inspiring both industry veterans and the new generation of printed circuit engineers, and by adding valuable industry educational content and professional development in support of the evolution of today's printed circuit engineer. When I think about all the industry educational content, both free and fee based, being offered through so many virtual events, it's hard to open my inbox and not find a single virtual event or two being offered by one company or another, by an industry subject-matter expert (SME) here and there, or from one industry source or another offering up industry educational content.

Because of how 2020 unfolded, since mid-year last year our inboxes have been filled with many educational content events being offered virtually. It's hard enough to find time to attend at least one of these virtual events in each of our respective busy schedules. It's even harder to know which event will provide the best or most valuable content. The challenge then becomes filtering out what is considered "good content" or "not so good content," or what is considered just industry "noise." Which virtual event is right for you to squeeze into your already busy schedule and attend? That's the million-dollar question. I know this because it's a daily dilemma as I go through my email inbox every day. Personally, if I had the time, I'd attend everything I could get my hands on related to printed circuit engineering. You never know where that golden nugget of knowledge will be found or perhaps an opportunity to sync up with an individual who will add positive value or inspiration for you.

With PCEA, we definitely do our very best professionally and with passionate due diligence to make sure our educational content and our virtual events are on point so that true industry collaboration is taking place. We aim to offer the latest, relevant industry educational content that is directly related to what's going on within today's ever evolving industry technology. Finally, with lots of passion and excitement, we continue to offer inspiration for growth, professional development, and success to every individual taking advantage of what PCEA has to offer. So, the next time you open your inbox and happen to come across that PCEA email, I highly recommend you open and read it so that you can take advantage of all PCEA opportunities we offer. Don't just "swipe left." From one printed circuit engineer to another—you won't be disappointed. I'm sure of this!

Refer to our column and the PCEA website to stay up to date with the up-and-coming industry events. There are many free webinars, so take advantage of these opportunities as much as you can. If you have not yet joined the PCEA collective, I highly encourage you to do so by visiting pce-a.org and becoming a PCEA member.

I wish all of you health and safety. Best of success to all as 2021 unfolds.

Warmest Regards,
—Steph

Next Month

We've got more PCEA Chapter meetings coming up to report on, with some exciting new chapters forming and I will be touching base with some of our international chapters to see what they are up to.

Upcoming Events

Below is a list of upcoming events which may lead you to mutate your thought process or at least provide you with antibodies to help ward off career stagnation.

- March 6–11: **IPC APEX EXPO** *(Virtual)*
- May 11–13, 2021: **IPC High-Reliability Forum 2021** *(Baltimore, Maryland)*
- August 16–18, 2021: **DesignCon** *(San Jose, California)*
- November 10, 2021: **PCB Carolina** *(Raleigh, North Carolina)*

Spread the word. If you have a significant electronics industry event that you would like to announce, please send me the details at kelly.dack.pcea@gmail.com, and we will consider adding it to the list.

Refer to our column and the PCEA website to stay up to date with the up-and-coming industry events. If you have not yet joined the PCEA collective, please visit pce-a.org and find out how to become a PCEA member.

Conclusion

Whether we realize it or not, we leave footprints on every activity we take part in. We leave physical footprints from our walk into the office. We leave digital footprints on the internet while searching for data used to create component footprints for our PCB design libraries. Hopefully, the professional footprints we leave throughout our careers will not only show that we collected data to achieve our own personal goals, but our footprints will show interwoven paths to people we helped in order to achieve their goals along the way. Lasting footprints not only reflect two surfaces which happen to have met with one another. They reflect all the brilliance of the people and ideas above and below their contact surfaces.

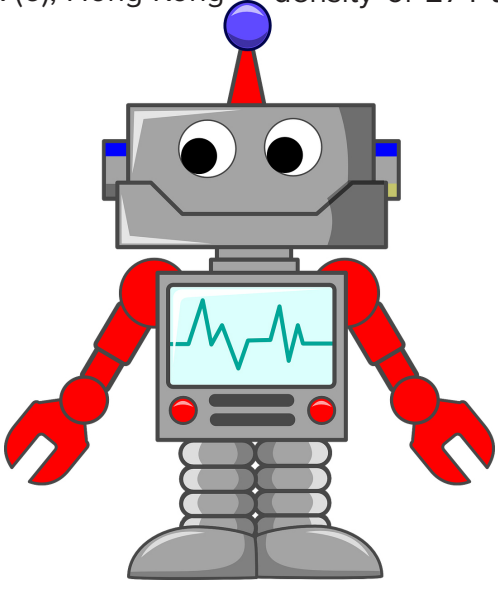
See you next month or sooner! DESIGN007

Kelly Dack, CIT, CID+, is the communication officer for the Printed Circuit Engineering Association (PCEA). To read past columns or contact Dack, click here.

Robot Race: The World´s Top 10 Automated Countries

The average robot density in the manufacturing industry hit a new global record of 113 units per 10,000 employees. By regions, Western Europe (225 units) and the Nordic European countries (204 units) have the most automated production, followed by North America (153 units) and South East Asia (119 units). The world´s top 10 most automated countries are: Singapore (1), South Korea (2), Japan (3), Germany (4), Sweden (5), Denmark (6), Hong Kong (7), Taiwan (8), USA (9) and Belgium and Luxemburg (10). This is according to the latest World Robotics statistics, issued by the International Federation of Robotics (IFR).

The country with the highest robot density by far remains Singapore with 918 units per 10,000 employees in 2019. South Korea comes second with 868 units per 10,000 employees in 2019. Japan (364 robots per 10,000 employees) and Germany (346 units), rank third and fourth respectively. Japan is the world´s predominant robot manufacturing country—where even robots assemble robots: 47% of the global robot production are made in Nippon. Germany is by far the largest robot market in Europe with 38% of Europe's industrial robots operating in factories here.

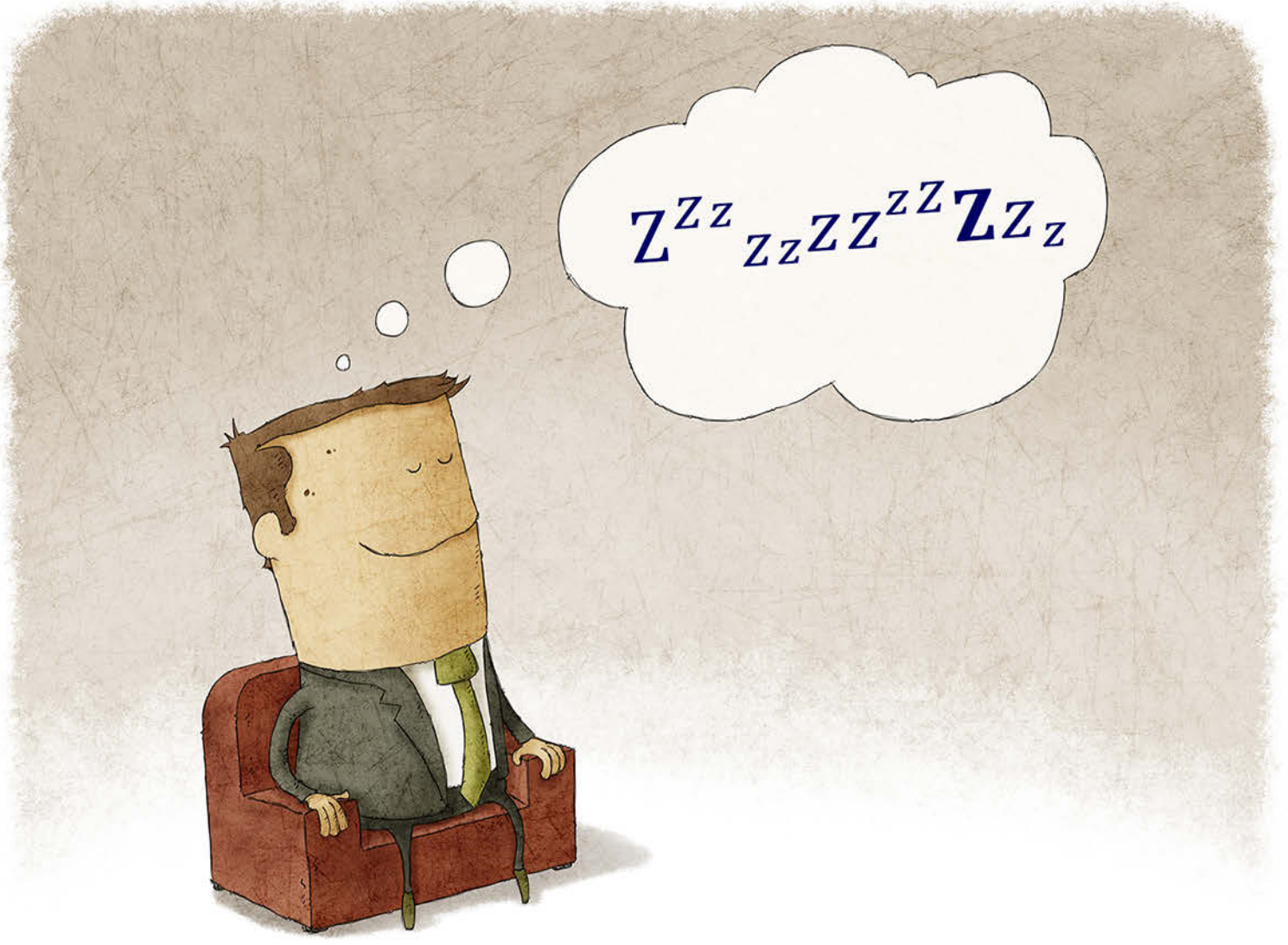


Sweden remains in fifth position with a robot density of 274 units operating with a share of 35% in the metal industry and another 35% in the automotive industry.

The development of robot density in China continues dynamically: Today, China's robot density in the manufacturing industry ranks 15th worldwide. Next to car production, China is also a major producer of electronic devices, batteries, semiconductors, and microchips.

(Source: IFR)

We DREAM Impedance!



Did you know that two seemingly unrelated concepts are the foundation of a product's performance and reliability?

- Transmission line impedance and
- Power Distribution Network impedance

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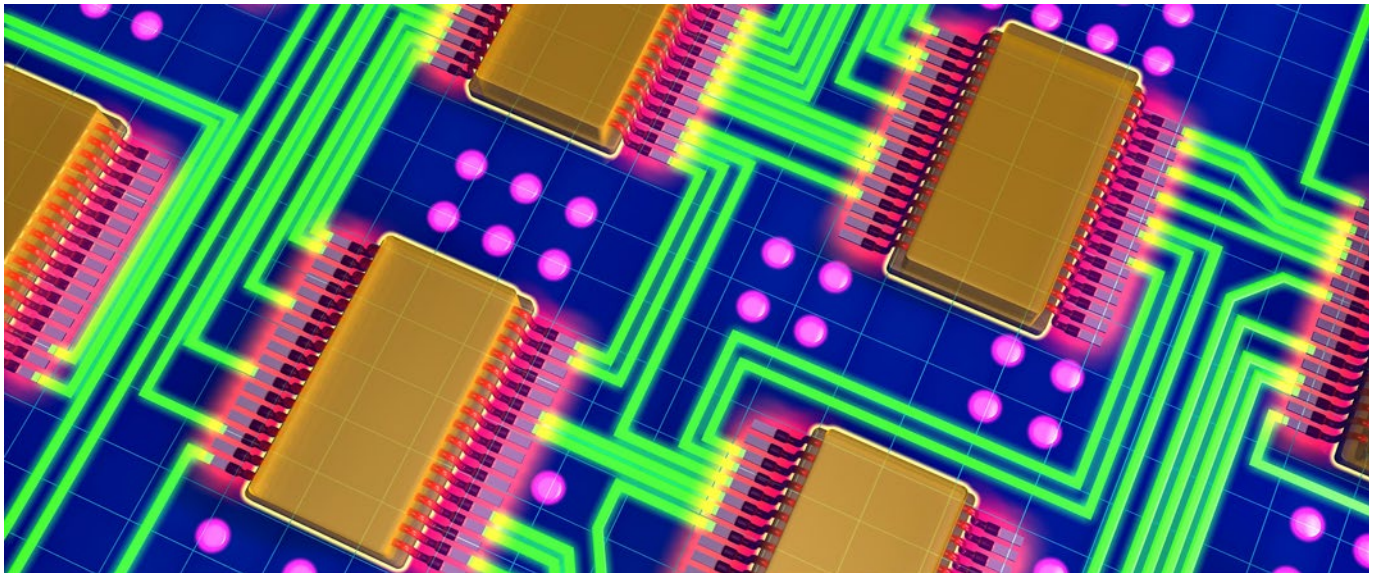
FLEX007
A SPECIAL DESIGN007 MAGAZINE SECTION

IC Package Footprints:
Why So Many and How Many Is Enough?

Flexible Thinking
FLEX007 Feature Column by Joe Fjelstad, VERDANT ELECTRONICS

The integrated circuit is credited to both Jack Kilby and Robert Noyce. Kilby was an experimentalist who had worked at CentraLab in Milwaukee, and a purveyor of ceramic insulators with printed conductors (true printed circuits, if you will). He was evidently inspired by his work in ceramic printed circuits and saw how the technology could be used to integrate discrete transistors to make a functional circuit block; thus, he was the first to reduce the concept and demonstrate it in his first few months at his new employer, Texas Instruments. Noyce had a similar vision at Fairchild Semiconductor, a company he co-founded, but he used a more thought-out engineering approach to develop ICs.

The challenge for both approaches upon completion of the IC was how to protect it and make it more useful; thus, the IC package was born. TI was again first out of the gate, delivering ICs in ceramic packages with flat peripheral leads on two sides. These were used on NASA's Apollo computers and the ICs were surface mounted. Fairchild had a different and



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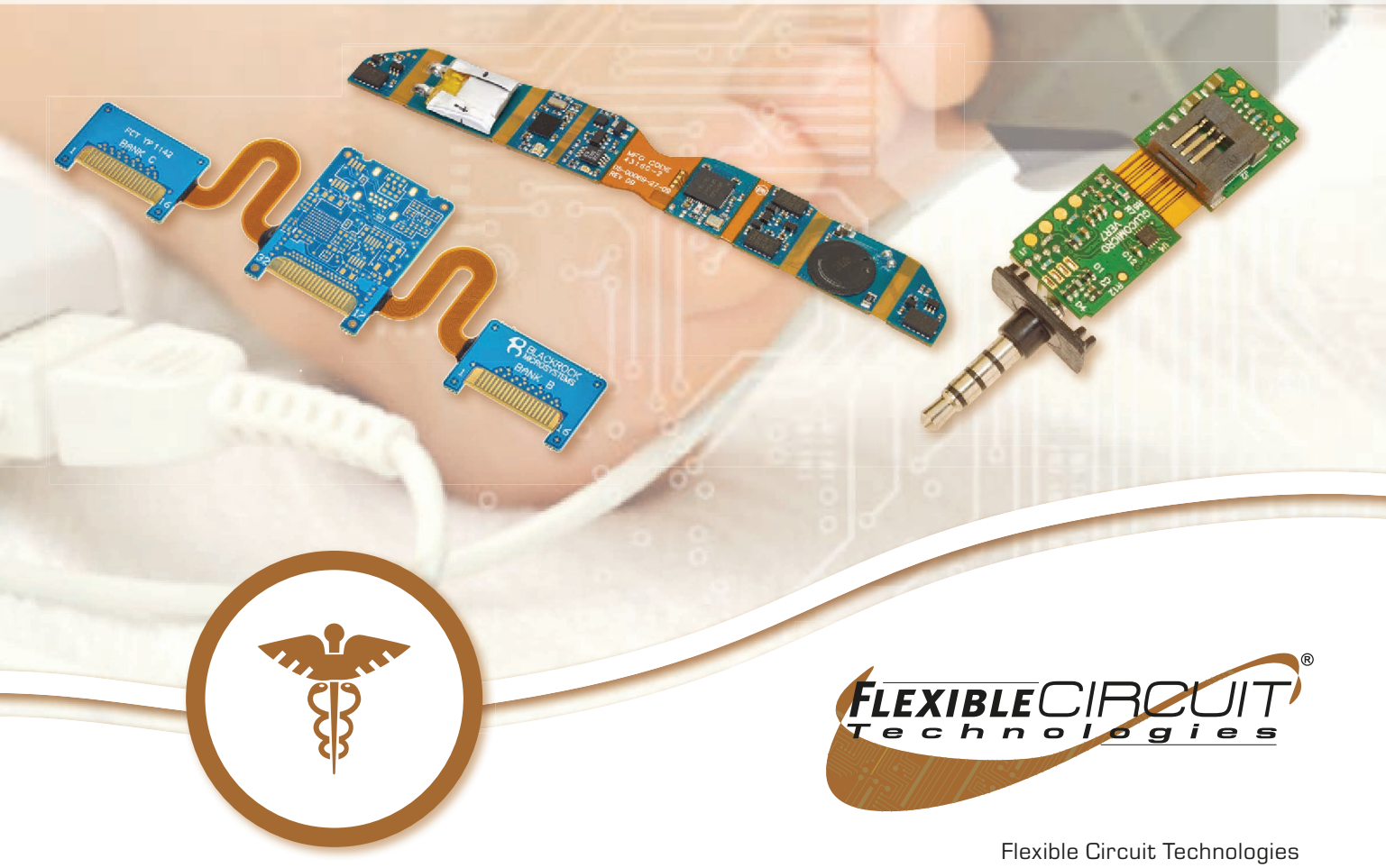

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less expensive idea—the dual in-line package (DIP) with the die attached and interconnected to a lead frame, then protected with an epoxy. Its leads were formed in a manner that allowed them to be soldered into through-holes of a PCB.

The DIP package became the preferred format and dominated for most of the early years. It is still in use today, though it would likely be much cheaper to use a more modern format of the era and integrate advancements to bonding such as tab bonding, double bonding, and varying wire diameter.

The DIP package became the preferred format and dominated for most of the early years.

However, from a performance perspective, skew, clock speed and frequency requirements soon exceeded the limitations of signal through wire, through DIP pin, down to the plated holes and through the PCB, to keep up with electronic performance demands. In the 1980s, surface mount technology was identified as the best way to achieve what had become the prime objectives of electronic product developers (i.e., faster, smaller, cheaper, lighter, and better). Surface mount technology offered all these benefits. However, little attention was given to basic geometry and the arithmetic relationships between the package dimensions and the trace and via routing implicit in the deployment of these newer package types into a PCBA.

To plan for the future, a planning convention was required. This resulted in the arguably arbitrary "80% rule" of generational package lead pitch reduction. By its very definition, the "rule" combined both legacy Imperial measurements and metric measurements. The resulting conversion issues triggered an explosion in package types: pin grid arrays (PGA), small outline packages (SOP), thin small outline packages (TSOP), quad flat packages (QFP), land grid arrays (LGA), and ball grid arrays, to name but a few. These packages had many different lead shapes: flat, straight, gull wing, J-lead, and truncated, among others.

Thus the 80% rule also resulted in an explosion in lead pitches, which assured the end of easily designed routing layers with multiple lead pitches employed in a common design. For the reader's consideration, ponder this: During the era dominated by through-hole devices there was fundamentally one lead pitch of 0.1" or 100 mils. If one has ever visited an electronic hobbyist's store, one may have noticed what appeared to be blank epoxy boards with hundreds of holes drilled in them in a gridded fashion. They are commonly referred to as "bread boards" and they allow hobbyists to more easily assemble their circuit designs using through-hole components such as DIPs, TO cans, and axial leaded discrete devices.

The causes for the explosion were pretty much two-fold. First, the global electronic community, including the U.S., agreed to use the metric system for all measurements related to electronic production. This included outlines and lead pitches. The second was an agreement to follow the 80% rule, which held that every subsequent generation of lead pitches should be 80% of the previous lead pitch (or as close as practical). Thus, legacy pitches such as 100 mil became 2.54 mm, and 50 mil became 1.27 mm. Other finer pitches beginning with 1.25 mm were 1.0 mm. 0.8 mm, 0.65 mm, 0.5 mm, 0.4 mm, 0.3 mm, 0.25 mm, and 0.2 mm. The result is that today, there is a mind-numbing number of package options.

Earlier generation designers demanded that planning and math come first. In the tape and rubylith era (horse and buggy days, I know), math ruled. The completed schematic was

BENDING THE POSSIBILITIES

FLEXFINER

BY TAIYO

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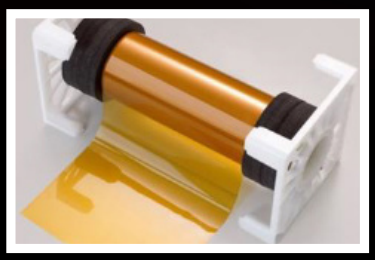
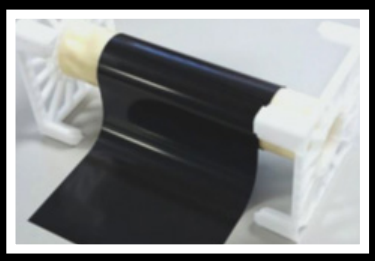


AMBER



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bedrock, and finally the BOM served to provide quick reference. When CAD became stable and made it easier to integrate the "hard math" of the EE to a reasonable degree, the math began getting kicked to the curb. Today, fewer and fewer designers have the "scar tissue" of the earlier veterans and thus have the ability to fully appreciate the fundamental importance of planning.

Today, fewer and fewer designers have the "scar tissue" of the earlier veterans and thus have the ability to fully appreciate the fundamental importance of planning.

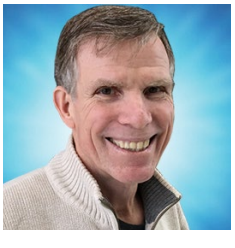
The 80% rule was not optimum but satisfactory for the early SMT industry. Where it missed opportunity was when it was applied to area array packages such as BGAs and CSPs. Area array land patterns have an intrinsic advantage: If all devices conform to the use of a common base grid such as 0.5 mm or 0.1 mm, trace, via, and plane artwork creation is streamlined because the component count options drop dramatically and layer counts can be significantly reduced. The lesson is this: When lead pitches are fewer in number, vias fall on larger grids, and the routing lanes (trace + gap) align, thus creating less "hypotenuse diagonal" trace length across the circuit layout.

This is graphically illustrated in a design comparison done by PCB design master Darren Smith of Athena Tech and published in Solderless Assembly For Electronics: The SAFE Approach, available for free download in the I-Connect007 eBook library.

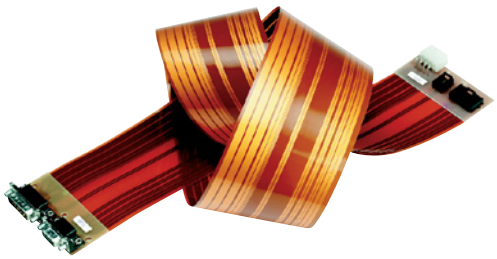
The sage CEO of a consulting company I worked for in the late 1990s was often heard to say, "Too soon old, too late smart," when seeing that simple solutions were often overlooked or unrecognized in our problem-solving efforts. However, I have attached to that thought another time-worn aphorism: "Better late than never." We are learning beings if we allow ourselves permission to do so and think beyond the pale. As Mark Twain said, "It's not what you don't know that gets you into trouble; it's what you know for sure that just ain't so."

So, I believe the fundamental answer to the question posed in the title of this column is that there are far too many options. JEDEC allows virtually any package outline and pitch configuration to be registered and we are overloaded with options. I personally believe that fewer options, especially when all components share a common lead pitch for IC package terminations (my suggestion is 0.5 mm, the pitch below which soldering becomes progressively more difficult) is both simpler and better for design and manufacturing. However, one of the strange ironies of achieving simplicity is that it generally takes more forethought and discipline to execute a simple design than it does for more complex ones. So it goes. **FLEX007**

Note: Thanks are extended to design expert Darren Smith for his reviewing skills and valuable comments.



Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185 patents issued or pending. To read past columns or contact Fjelstad, click here. Download your free copy of Fjelstad's book *Flexible Circuit Technology, 4th Edition,* and watch his in-depth workshop series "Flexible Circuit Technology."



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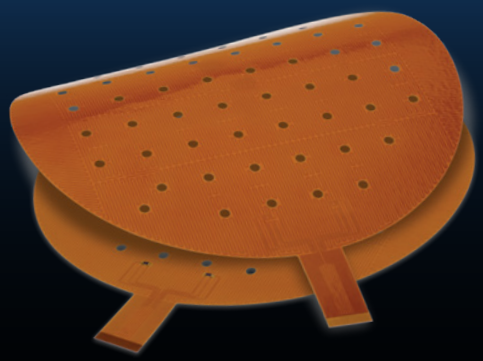

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Flex007 Highlights

Consider This: Advancements in Printed Circuit Manufacturing Equipment ▸

Computers, lasers, and artificial intelligence are infiltrating every area of the PCB manufacturing facility. The interconnecting intelligence allows for quicker file processing, higher accuracy, and vastly improved yields.

Flex Talk: Demystify Flexible Stack-ups ▸

The sheer number of flexible laminate materials and constructions can be a bit daunting for those new to flex and rigid flex design. Tara Dunn sits down with Jeff Martin from Omni PCB to hear his insight into flexible laminates and his advice when working on a flex stack up.

Nano Dimension Strengthening its Leadership Position in 3D Printed Electronics with AME Design Methodology ▸

Nano Dimension Ltd., a leading additively manufactured electronics/printed electronics) provider, offers quick solutions and easy access to complex PCBs and 3D printed electronics. Its unique and novel technology allows for rapid prototyping and production of high-performance electronic devices (Hi-PEDs™).

Flex CCL Supplier Taiflex Posts Strong Results in December ▸

Taiflex Scientific Co. Ltd, a Taiwanese manufacturer of flexible copper clad laminate (CCL) material for flex PCBs, has reported consolidated revenue of NT$782 million ($27.9 million at $1:NT$28.02) for December 2020, up by 18.5% from December 2019 figures.

Liquid Wire Delivers Best-in-Class Performance in NextFlex Study of Printed Stretchable Conductor Systems ▸

Liquid Wire Inc. announced that it has joined the NextFlex community, whose mission it is to advance U.S. manufacturing of flexible hybrid electronics (FHE) by fostering technology innovation and commercialization.

Lenthor Engineering Renews Registration of ITAR, SAM ▸

Lenthor Engineering, Inc., a California based designer, manufacturer and assembler of rigid-flex and flex printed circuit boards, has recently received notice of compliance with and renewed registrations for both ITAR and SAM.

Flexible Thinking: Flexible Circuits Vs. Flexible Hybrid Electronics—Where's the Line? ▸

The line separating polymer thick film flexible circuit assemblies from flexible hybrid electronics, exists but it is not hard and bright. The introduction of new flexible circuit manufacturing technologies and materials including stretchable substrates has created a surge of interest in their use.

North American PCB Industry Sales up 4.5% in December ▸

IPC announced the December 2020 findings from its North American Printed Circuit Board (PCB) Statistical Program. The book-to-bill ratio stands at 1.05. Total North American PCB shipments in December 2020 were up 4.5% compared to the same month last year.

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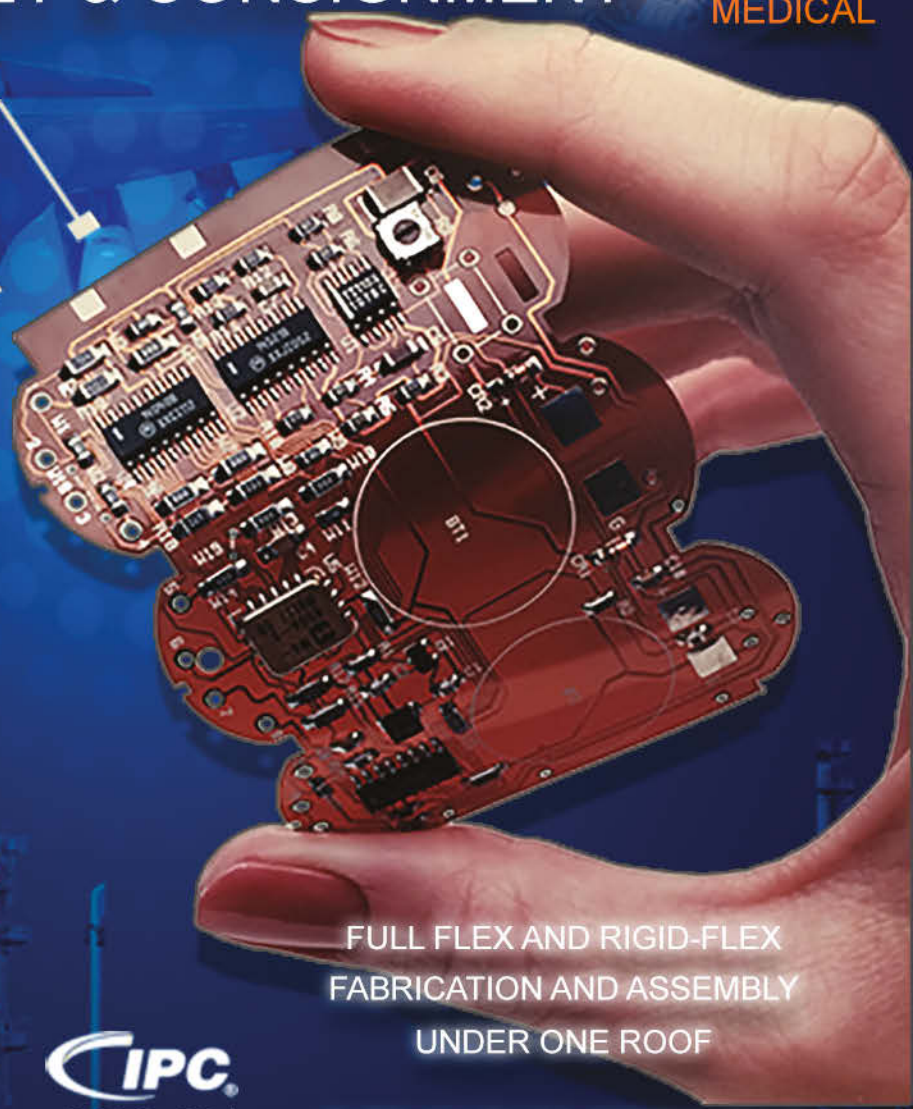

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PCB Technologies We Need Now and Later

Consider This

by John Talbot, TRAMONTO CIRCUITS

RF high-frequency circuits are in almost every vehicle being produced today, with side, front, and rear radar to warn of potential collisions. Specialized RF technology high-frequency PCBs are in high demand.

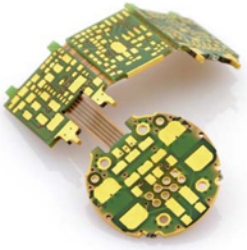
Newer flex designs for automobiles are used in many areas: seat wiring, dash, and even replacing hard wiring within the car. Flex lays flatter, takes up less room, and weighs less than hard wires.

Thermal insulated metal substrates (IMS) are experiencing rapid growth in LED lighting, cars and homes, and even streetlights. Power circuits are utilizing IMS to shrink the size and control heat. IMS allows for more current through smaller track widths and eliminates some heavy copper traces.

Higher-frequency laminate with lower Dk and very low-loss Df will be used for 5G. The new 5G system will be the go-to technology for controlling communications and even machine control, offering wider band width, higher speed signals and more computing power in a smaller package. The PCBs which will be used will need to be able to handle 5 GHz frequencies, requiring new types of laminates.

Artificial intelligence is here, from autonomous cars to automated factories. It is potentially the biggest thing to change your life and our PCB business. Smart computers need not only fast, high frequency PCBs, but they need all the sensors to send the signals to the AI computer which they need to understand and

Focused on Flex



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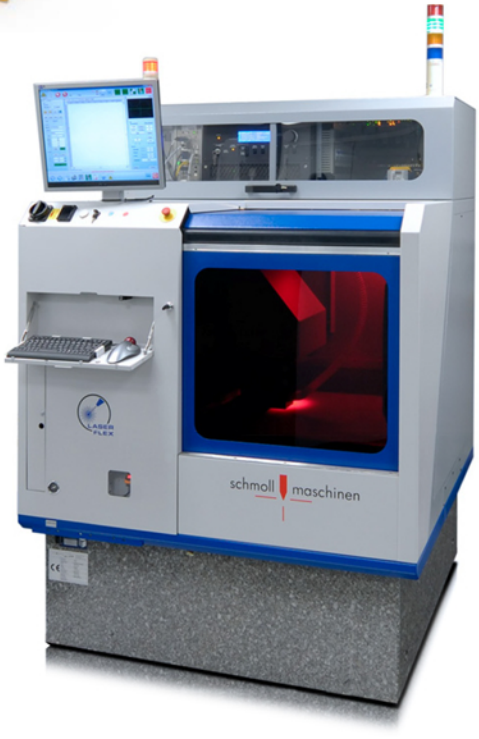

Typical applications:

- Polymer cover foil
- Covered polymer laminates
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- Micro-via and through-hole drilling

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to know the world which they control. It is all here and ready to explode.

As a side note, I used an AI feature to properly spell "autonomous." Now my computer is sending data because I used Word's Smart Look-up feature to find the word "autonomous" and my Google pages will be filled with ads for AI. It's pinpoint sniper advertising, only aimed at me. All the advanced AI electronics on PCBs allows them to identify my inquiries and target only me with those ads. I found this out a few weeks ago. I checked Word to get the correct capitalization for a Raspberry Pi computer. The same day, I was suddenly getting four to six ads per page on Google for Raspberry Pi computers. Coincidence? I think not. I was specifically targeted. The ads were sent to only me out of billions of internet users, and this part scares me the most.

I was specifically targeted. The ads were sent to only me out of billions of internet users, and this part scares me the most.

The point is that a huge number of PCBs were involved in allowing them to target an ad to only me. From my home PC and the internet router box, to a box outside my home and the 20 or more routing computers on the internet, all that information is sent back to some advertising company. Then, the data goes through a computer that "knows" to send me the ads they wanted me to see. It took a few hundred PCBs with powerful computers to achieve the feat. Our industry is only too happy to sell all the PCBs needed to make this targeted ad propaganda work.

The average size of a PCB has decreased greatly. A few years ago, a small PCB was 50 square inches. Today, most PCBs measure only a few square inches, and many are much smaller. In one reality, we are using much more laminate, but we are making many smaller PCBs.

These small PCBs are in smart watches, small RF radar units for your car, and every one of the billions of LED light bulbs; if you look carefully enough, you will find the tiny PCBs everywhere. However, many PCB shops are not specifically set up to manufacture very small PCBs with large spaces between individual PCB parts to allow for router bits to cut them. A smart move would be to design your shop panels to use every little bit of space and use laser or die cutters to increase the number of PCBs that you can squeeze onto a panel.

Conductive silver or tin on glass is a specialty market. With every one of the billions of phones utilizing this technology, it is a massive market all to itself. It utilizes specific plating baths and special imaging and etching equipment. Many of the tiny, overlapping traces are actually screen-printed silver and clear insulative inks. It is expensive to set up, however, the volumes are tremendous.

Ultra-thin multilayer is a quickly growing technology, utilizing thin glue sheets and very thin laminates to produce eight layers, under 20 mils thick. The thin circuits are in cellphones, computers, and a lot of other very small devices. A surprising amount of technology fits on these little circuits, such as hearing aids controlled by your smartphone.

3D printing will be the big disrupter to change the PCB business. They are now quickly printing stainless steel, titanium, copper, and other metals as well as dielectric bases. The 3D printers are already making FR-4 type laminates. Once the technology is sorted out, 3D printing of a PCB will be upon us quickly. Recent changes in the technology have improved speed by 20 times and lowered cost by 10 times. Soon we will see real 3D-printed circuit boards.

Two other technologies that are quickly growing are heavy copper and high voltage

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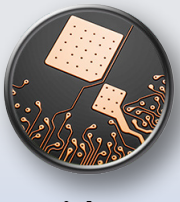

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PCBs. Spurred on by the electric car and transportation gold rush, both types of PCBs are needed in large quantities. The high voltages of the batteries at 300–600 volts, and the massive currents to drive the motor, require significant thick copper traces on the driver PCB and superior laminates with high voltage dielectric properties.

Embedded components are a newer technology that allows more components to be placed on and inside a PCB. Having resistors and capacitors inside allows for more chips and larger components on the two outer layers. It is even possible to insert physical resistors and capacitors in very small sizes. The alternative is to print the components inside, using resistive or capacitive laminates.

There are so many new technologies within the encompassing dome of PCB manufacturing that for any one single PCB shop to know everything about each specialty technology is getting harder and more difficult to manage. **FLEX007**

John Talbot is president of Tramonto Circuits. To read past columns or contact Talbot, click here.

Siemens, MaRS to Accelerate Innovation for Startups in Development of Autonomous, Connected Vehicles

Siemens Digital Industries Software and MaRS Discovery District, a Toronto-based innovation hub, have partnered to provide over 1,400 Canadian science and technology companies with access to Siemens' Xcelerator portfolio of software and services to support and accelerate the development of autonomous and connected vehicle technologies. The design and simulation software can help companies in the MaRS ecosystem conduct early design development and advanced verification of autonomous function and performance systems.

Startup companies are at the forefront of engineering and product innovation and they encounter similar complex design challenges as their larger counterparts, so it's vital that they build a foundation of digital technology that enable expansion and growth as company needs evolve. Most startups begin with core CAD and CAE technologies but evolving product complexity, for example the quantity of parts and design complexity, often require additional capabilities such as data management, advanced simulation, and manufacturing software. MaRS understands these needs and challenges and strives to provide foundational services to their startup community that enable development and growth.

MayaHTT, a long-time Siemens partner with unique expertise in addressing complex technical challenges from chip design to full vehicle system validation will support MaRS companies with software deployment and training services.

"The rise of autonomous and connected vehicles is changing the way the vehicles are designed, manufactured and tested. This emphasis on agile development cycles requires new partnerships and collaboration across the supply chain," said Jamie Dinsmore, Vice President and Country Manager, Canada at Siemens Digital Industries Software. "We are proud to partner with MaRS to empower Canadian startups by providing data management and simulation tools they can use from the beginning of their journeys, which can enable traceability, collaboration and early design validation that can improve product delivery and success." (Source: Siemens)

Design + Fabrication + Assembly =

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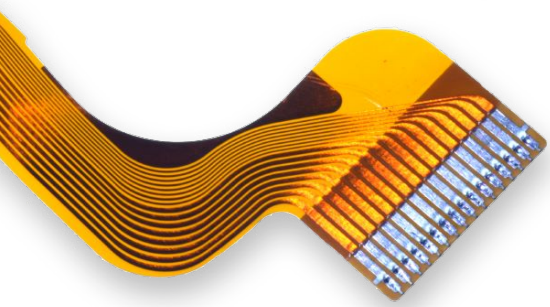

It all adds up to one complete PCB solution.

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Check out John Talbot's column *Consider This*

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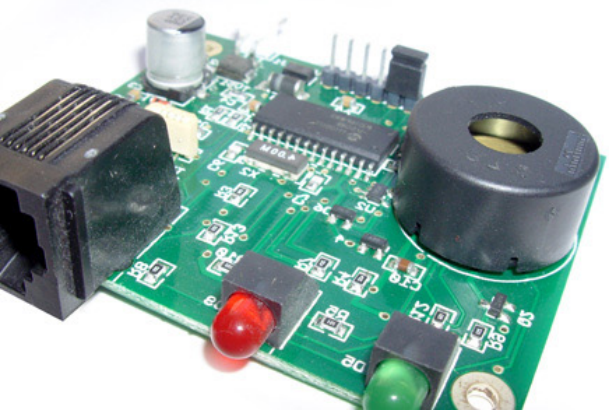

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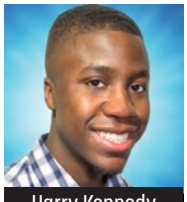
1 Fresh PCB Concepts: RF PCB Designs–Challenges, Solutions and Tips ▸


Harry Kennedy

Today, RF circuitry is crammed into a large variety of commercial products. Most of these are handheld wireless devices for medical, industrial, and communications applications. There are also applications in a variety of fields that are migrating from desktop models to become portable communications units.

2 Elementary, Mr. Watson: 2020—The Year that Taught Us Resilience ▸

Yes, 2020 was a challenge. It's during those times that we can learn some significant lessons if we allow them.

3 Dana on Data: Factory 4.0 NPI Data Transfer Improvements ▸


Dana Korf

The recently released IPC Connected Factory Initiative scope is similar to other Factory 4.0 models with the same glaring omission: They all seem to assume that the incoming design data can't be used as-is and must be reviewed and potentially manually modified prior to manufacturing release.

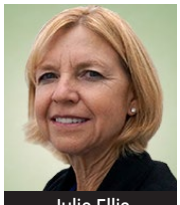
4 The Digital Layout: Now, Where Were We? ▸

In this month's column, Kelly Dack shares a few terms he's been contemplating lately, and which he have been trying to put in context regarding the role of the PCEA within the electronics industry. Then, PCEA Chairman Stephen Chavez to inspire us for a fresh start in the new year. Finally, he provides us with a list of events which are coming up.

5 Design Circuit: 2021 Updates to IPC Design ▸

A year of COVID-19 has taught the world how to operate more efficiently in the virtual amphitheater, and IPC is no different. While standards development meetings have historically occurred via teleconference, and most internal IPC business is conducted remotely, our larger programs—training and educational activities, full-day development meetings, hand-soldering competitions, etc.—have always relied on face-to-face collaboration.

6 TTM's Approach to Stackup Design: Train the Customer ▸


Julie Ellis

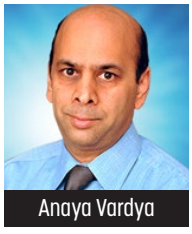
TTM's Julie Ellis and Richard Dang drill down into stackup design, detailing some of the common stackup challenges that their customers face when designing for both prototype and volume levels, and offering advice to designers or engineers who are struggling with stackup issues.

7 Cutting Respins: Journey to the Single-spin PCB ▸


Chris Young

As an engineer/business owner, I find respins frustrating because I would rather spend my time and money applying scientific principles inventing, improving technology, and solving problems. I am not an advocate for perfectionism, but rather I focus on becoming a better adventurer.

8 Standard of Excellence: The Importance of Supplier Retention ▸


Anaya Vardya

We spend a great deal of time and money on attaining low customer turnover rates, making sure that we keep those good customers we worked so hard to attain. But what about holding onto our good PCB vendor/partners? We need to be sure that we are retaining our good suppliers with the same diligence that we hold on to our customers.

9 Just Ask Heidi Barnes: The Exclusive Compilation ▸


Heidi Barnes

We asked for your questions for Keysight Technologies' Heidi Barnes, and you took us up on it! We know you all enjoyed reading these questions and answers, so we've compiled all of them into one article for easy reference. We hope you enjoy having another bite at the apple.

10 Maxed Out: Component Search Engine is a Total Game Changer ▸


Clive "Max" Maxfield

The Component Search Engine provides designers with free access to hundreds of thousands of ECAD and MCAD models in the form of schematic symbols, PCB footprints, and 3D models.

PCBDesign007.com for the latest circuit design news and information.

Flex007.com focuses on the rapidly growing flexible and rigid-flex circuit market.

Career Opportunities

How Do Your Team Members Stack Up?

Find industry-experienced candidates at I-Connect007.

For just $750, your 200-word, full-column ad will appear in the "career opportunities" section of all three of our monthly magazines, reaching circuit board designers, fabricators, assemblers, OEMs, and suppliers.

In addition, your ad will be featured in at least one of our newsletters, and your posting will appear on our **jobConnect007.com** board, which is also promoted in every newsletter.

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Career Opportunities

EAGLE electronics Inc.
MANUFACTURERS OF QUALITY PRINTED CIRCUIT BOARDS

Pre-CAM Engineer

Illinois-based PCB fabricator Eagle Electronics is seeking a pre-CAM engineer specific to the printed circuit board manufacturing industry. The pre-CAM Engineer will facilitate creation of the job shop travelers used in the manufacturing process. Candidate will have a minimum of two years of pre-CAM experience and have a minimum education level of an associate degree. This is a first shift position at our Schaumburg, Illinois, facility. This is not a remote or offsite position.

If interested, please submit your resume to HR@eagle-elec.com indicating 'Pre-CAM Engineer' in the subject line.

Process Engineer

We are also seeking a process engineer with experience specific to the printed circuit board manufacturing industry. The process engineer will be assigned to specific processes within the manufacturing plant and be given ownership of those processes. The expectation is to make improvements, track and quantify process data, and add new capabilities where applicable. The right candidate will have a minimum of two years of process engineering experience, and a minimum education of bachelor's degree in an engineering field (chemical engineering preferred but not required). This is a first shift position at our Schaumburg, Illinois, facility. This is not a remote or offsite position.

If interested, please submit your resume to HR@eagle-elec.com indicating 'Process Engineer' in the subject line.

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INTERNATIONAL GROUP
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Sales Desk & Supply Chain Manager, Leamington Spa, UK

Want to advance your career by joining a globally successful and growing world class CCL manufacturing company and help drive that success? As sales desk & supply chain manager you will work towards maximizing the efficiency and effectiveness of controlling stock levels and sales interactions with the customers and ensuring that the requirement of the business for fast turn delivery of quality products is met in the most cost effective and efficient way. Your tasks will include sales desk & stock management, implementing performance improvement measures, procuring materials and resources and assuring compliance. You will be a mentor to your team members and implement best practices across all levels.

Skills and abilities required:

- Proven commercial experience in similar role for minimum 5 years
- Knowledge of organizational effectiveness and operations management
- Experience with ISO9001 or similar QMS required
- Experience with Lean Six Sigma a plus
- Excellent leadership ability and communication skills (English)
- Computer literate (Microsoft Suite)
- Experience with ERP-systems

What's on offer:

- Excellent salary and benefits commensurate with experience

This is a fantastic opportunity to become part of a successful brand and leading team.

Please apply in the strictest confidence, enclosing your CV to humanresource@ventec-europe.com.

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Career Opportunities

ventec INTERNATIONAL GROUP 騰輝電子

Operations Manager, Elk Grove Village IL, USA

Want to advance your career by joining a globally successful and growing world class CCL manufacturing company and help drive that success? As operations manager at Ventec USA LLC, a wholly owned subsidiary of Ventec International Group, you will coordinate and oversee our organization's operations in Elk Grove Village, IL, and Fullerton, CA. Your tasks will include formulating strategy, implementing performance improvement measures, procuring materials and resources and assuring compliance. You will be a mentor to your team members, find ways to maintain and improve the highest quality of customer service and implement best practices across all levels.

Skills and abilities required for the role:

- Proven commercial experience as operations manager or similar role for minimum 5 years
- Knowledge of organizational effectiveness and operations management
- Experience with ISO9001 or similar QMS required
- Experience in budgeting and forecasting & familiarity with business and financial principles
- Excellent leadership ability and communication skills (English)
- Outstanding organizational skills
- Degree in Business, Operations Management, or related field preferred but not required

What's on offer:

- Excellent salary and benefits commensurate with experience

This is a fantastic opportunity to become part of a successful brand and leading team with excellent benefits.

Please forward your resume to jpattie@ventec-usa.com and mention "Operations Manager—Elk Grove Village" in the subject line.

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SUMMIT INTERCONNECT

Our Summit Anaheim, CA, division currently has multiple open positions for planning engineers.

The planner is responsible for creating and verifying manufacturing documentation, including work instructions and shop floor travelers. Review lay-ups, details, and designs according to engineering and customer specifications through the use of computer and applications software. May specify required manufacturing machinery and test equipment based on manufacturing and/or customer requirements. Guides manufacturing process development for all products.

Responsibilities:

1. Accurately plan jobs and create shop floor travelers.
2. Create documentation packages.
3. Use company software for planning and issuing jobs.
4. Contact customers to resolve open issues.
5. Create TDR calculations.
6. Assist in the training of new planning engineers.
7. Review prints and purchase orders.
8. Create stackups and order materials per print/spec.
9. Plan jobs manufacturing process.
10. Institute new manufacturing processes and or changes.

Education/Experience:

1. High school diploma or equivalent
2. Minimum five (5) years' experience in the printed circuit board industry with three (3) years as a planning engineer.
3. Must be able to cooperate and communicate effectively with customers, management, and supervisory staff.
4. Must be proficient in rigid, flex, rigid/flex, and sequential lam designs.

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Career Opportunities

Now Hiring

Director of Process Engineering

A successful and growing printed circuit board manufacturer in Orange County, CA, has an opening for a director of process engineering.

Job Summary:

The director of process engineering leads all engineering activities to produce quality products and meet cost objectives. Responsible for the overall management, direction, and coordination of the engineering processes within the plant.

Duties and Responsibilities:

- Ensures that process engineering meets the business needs of the company as they relate to capabilities, processes, technologies, and capacity.
- Stays current with related manufacturing trends. Develops and enforces a culture of strong engineering discipline, including robust process definition, testing prior to production implementation, change management processes, clear manufacturing instructions, statistical process monitoring and control, proactive error proofing, etc.
- Provides guidance to process engineers in the development of process control plans and the application of advanced quality tools.
- Ensures metrics are in place to monitor performance against the goals and takes appropriate corrective actions as required. Ensures that structured problem-solving techniques are used and that adequate validation is performed for any issues being address or changes being made. Develops and validates new processes prior to incorporating them into the manufacturing operations.
- Strong communication skills to establish priorities, work schedules, allocate resources, complete required information to customers, support quality system, enforce company policies and procedures, and utilize resources to provide the greatest efficiency to meet production objectives.

Education and Experience:

- Master's degree in chemical engineering or engineering is preferred.
- 10+ years process engineering experience in an electronics manufacturing environment, including 5 years in the PCB or similar manufacturing environment.
- 7+ years of process engineering management experience, including 5 years of experience with direct responsibility for meeting production throughput and quality goals.

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Now Hiring

Process Engineering Manager

A successful and growing printed circuit board manufacturer in Orange County, CA, has an opening for a process engineering manager.

Job Summary:

The process engineering manager coordinates all engineering activities to produce quality products and meet cost objectives. Responsible for the overall management, direction, and coordination of the engineering team and leading this team to meet product requirements in support of the production plan.

Duties and Responsibilities:

- Ensures that process engineering meets the business needs of the company as they relate to capabilities, processes, technologies, and capacity.
- Stays current with related manufacturing trends. Develops and enforces a culture of strong engineering discipline, including robust process definition, testing prior to production implementation, change management processes, clear manufacturing instructions, statistical process monitoring and control, proactive error proofing, etc.
- Ensures metrics are in place to monitor performance against the goals and takes appropriate corrective actions as required. Ensures that structured problem-solving techniques are used and that adequate validation is performed for any issues being address or changes being made. Develops and validates new processes prior to incorporating into the manufacturing operations

Education and Experience:

- Bachelor's degree in chemical engineering or engineering is preferred.
- 7+ years process engineering experience in an electronics manufacturing environment, including 3 years in the PCB or similar manufacturing environment.
- 5+ years of process engineering management experience, including 3 years of experience with direct responsibility for meeting production throughput and quality goals.

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Career Opportunities

MacDermid Alpha ELECTRONICS SOLUTIONS

We're Hiring!
Connecticut Locations

Senior Research Chemist:
Waterbury, CT, USA

Research, develop, and formulate new surface treatment products for the printed circuit board, molded interconnect, IC substrate, and LED manufacturing industries. Identify, develop, and execute strategic research project activities as delegated to them by the senior research projects manager. Observe, analyze, and interpret the results from these activities and make recommendations for the direction and preferred route forward for research projects.

Quality Engineer:
West Haven, CT, USA

Support the West Haven facility in ensuring that the quality management system is properly utilized and maintained while working to fulfill customer-specific requirements and fostering continuous improvement.

For a complete listing of career opportunities or to apply for one of the positions listed above, please visit us here.

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MacDermid Alpha ELECTRONICS SOLUTIONS

We're Hiring!
Illinois / New Jersey

Technical Service Rep:
Chicago, IL, USA

The technical service rep will be responsible for day-to-day engineering support for fabricators using our chemical products. The successful candidate will help our customer base take full advantage of the benefits that are available through the proper application of our chemistries.

Applications Engineer:
South Plainfield, NJ, USA

As a key member of the Flexible, Formable, and Printed Electronics (FFPE) Team, the applications engineer will be responsible for developing applications know-how for product evaluation, material testing and characterization, and prototyping. In addition, this applications engineer will provide applications and technical support to global customers for the FFPE Segment.

For a complete listing of career opportunities or to apply for one of the positions listed above, please visit us here.

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Career Opportunities

Manncorp™

SMT Operator
Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for a **surface-mount technology (SMT) operator** to join their growing team in Hatboro, PA!

The **SMT operator** will be part of a collaborative team and operate the latest Manncorp equipment in our brand-new demonstration center.

Duties and Responsibilities:

- Set up and operate automated SMT assembly equipment
- Prepare component kits for manufacturing
- Perform visual inspection of SMT assembly
- Participate in directing the expansion and further development of our SMT capabilities
- Some mechanical assembly of lighting fixtures
- Assist Manncorp sales with customer demos

Requirements and Qualifications:

- Prior experience with SMT equipment or equivalent technical degree preferred; will consider recent graduates or those new to the industry
- Windows computer knowledge required
- Strong mechanical and electrical troubleshooting skills
- Experience programming machinery or demonstrated willingness to learn
- Positive self-starter attitude with a good work ethic
- Ability to work with minimal supervision
- Ability to lift up to 50 lbs. repetitively

We Offer:

- Competitive pay
- Medical and dental insurance
- Retirement fund matching
- Continued training as the industry develops

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Manncorp™

SMT Field Technician
Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:

- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:

- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Travel and overnight stays
- Ability to arrange and schedule service trips

We Offer:

- Health and dental insurance
- Retirement fund matching
- Continuing training as the industry develops

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Career Opportunities

LENTHOR ENGINEERING
MAKING THINGS FLEXIBLE IN A RIGID WORLD®

Sales Account Manager

Sales Account Management at Lenthor Engineering is a direct sales position responsible for creating and growing a base of customers that purchase flexible and rigid flexible printed circuits. The account manager is in charge of finding customers, qualifying the customer to Lenthor Engineering and promoting Lenthor Engineering's capabilities to the customer. Leads are sometimes referred to the account manager from marketing resources including trade shows, advertising, industry referrals and website hits. Experience with military printed circuit boards (PCBs) is a definite plus.

Responsibilities

- Marketing research to identify target customers
- Identifying the person(s) responsible for purchasing flexible circuits
- Exploring the customer's needs that fit our capabilities in terms of:
  - Market and product
  - Circuit types used
  - Competitive influences
  - Philosophies and finance
  - Quoting and closing orders
  - Providing ongoing service to the customer
  - Develop long-term customer strategies to increase business

Qualifications

- 5-10 years of proven work experience
- Excellent technical skills

Salary negotiable and dependent on experience. Full range of benefits.

Lenthor Engineering, Inc. is a leader in flex and rigid-flex PWB design, fabrication and assembly with over 30 years of experience meeting and exceeding our customers' expectations.

Contact Oscar Akbar at: hr@lenthor.com

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LENTHOR ENGINEERING
MAKING THINGS FLEXIBLE IN A RIGID WORLD®

Senior Process Engineer

Job Description

Responsible for developing and optimizing Lenthor's manufacturing processes from start up to implementation, reducing cost, improving sustainability and continuous improvement.

Position Duties

- Senior process engineer's role is to monitor process performance through tracking and enhance through continuous improvement initiatives. Process engineer implements continuous improvement programs to drive up yields.
- Participate in the evaluation of processes, new equipment, facility improvements and procedures.
- Improve process capability, yields, costs and production volume while maintaining safety and improving quality standards.
- Work with customers in developing cost-effective production processes.
- Engage suppliers in quality improvements and process control issues as required.
- Generate process control plan for manufacturing processes, and identify opportunities for capability or process improvement.
- Participate in FMEA activities as required.
- Create detailed plans for IQ, OQ, PQ and maintain validated status as required.
- Participate in existing change control mechanisms such as ECOs and PCRs.
- Perform defect reduction analysis and activities.

Qualifications

- BS degree in engineering
- 5-10 years of proven work experience
- Excellent technical skills

Salary negotiable and dependent on experience. Full range of benefits.

Lenthor Engineering, Inc. is the leader in Flex and Rigid-Flex PWB design, fabrication and assembly with over 30 years of experience meeting and exceeding our customers' expectations.

Contact Oscar Akbar at: hr@lenthor.com

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Career Opportunities

BLACKFOX
Premier Training & Certification

IPC Instructor

Longmont, CO; Phoenix, AZ; U.S.-based remote

Independent contractor, possible full-time employment

Job Description

This position is responsible for delivering effective electronics manufacturing training, including IPC Certification, to students from the electronics manufacturing industry. IPC instructors primarily train and certify operators, inspectors, engineers, and other trainers to one of six IPC Certification Programs: IPC-A-600, IPC-A-610, IPC/WHMA-A-620, IPC J-STD-001, IPC 7711/7721, and IPC-6012.

IPC instructors will conduct training at one of our public training centers or will travel directly to the customer's facility. A candidate's close proximity to Longmont, CO, or Phoenix, AZ, is a plus. Several IPC Certification Courses can be taught remotely and require no travel.

Qualifications

Candidates must have a minimum of five years of electronics manufacturing experience. This experience can include printed circuit board fabrication, circuit board assembly, and/or wire and cable harness assembly. Soldering experience of through-hole and/or surface-mount components is highly preferred.

Candidate must have IPC training experience, either currently or in the past. A current and valid certified IPC trainer certificate holder is highly preferred.

Applicants must have the ability to work with little to no supervision and make appropriate and professional decisions.

Send resumes to Sharon Montana-Beard at sharonm@blackfox.com.

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MivaTek Global

MivaTek Global: We Are Growing!

MivaTek Global is adding sales, technical support and application engineers.

Join a team that brings new imaging technologies to circuit fabrication and microelectronics. Applicants should have direct experience in direct imaging applications, complex machine repair and/or customer support for the printed circuit board or microelectronic markets.

Positions typically require regional and/or air travel. Full time and/or contractor positions are available.

Contact HR@MivaTek.Global for additional information.

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Career Opportunities

eptac

TRAIN. WORK SMARTER. SUCCEED.

Become a Certified IPC Master Instructor

Opportunities are available in Canada, New England, California, and Chicago. If you love teaching people, choosing the classes and times you want to work, and basically being your own boss, this may be the career for you. EPTAC Corporation is the leading provider of electronics training and IPC certification and we are looking for instructors that have a passion for working with people to develop their skills and knowledge. If you have a background in electronics manufacturing and enthusiasm for education, drop us a line or send us your resume. We would love to chat with you. Ability to travel required. IPC-7711/7721 or IPC-A-620 CIT certification a big plus.

Qualifications and skills

- A love of teaching and enthusiasm to help others learn
- Background in electronics manufacturing
- Soldering and/or electronics/cable assembly experience
- IPC certification a plus, but will certify the right candidate

Benefits

- Ability to operate from home. No required in-office schedule
- Flexible schedule. Control your own schedule
- IRA retirement matching contributions after one year of service
- Training and certifications provided and maintained by EPTAC

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APCT

Passion | Commitment | Trust

APCT, Printed Circuit Board Solutions: Opportunities Await

APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

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Career Opportunities

U.S. CIRCUIT

Sales Representatives (Specific Territories)

Escondido-based printed circuit fabricator U.S. Circuit is looking to hire sales representatives in the following territories:

- Florida
- Denver
- Washington
- Los Angeles

Experience:

- Candidates must have previous PCB sales experience.

Compensation:

- 7% commission

Contact Mike Fariba for more information.

mfariba@uscircuit.com

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YOUR JOB AD HERE

For information, please contact:
BARB HOCKADAY
barb@iconnect007.com
+1 916.365.1727 (PACIFIC)

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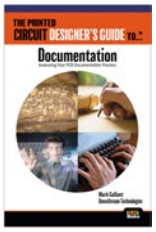
I-007e EDUCATIONAL RESOURCE CENTER

Learn from the Experts in Our On-demand Video Series

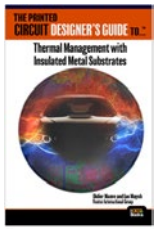
NOW AVAILABLE:
***Implementing "Digital Twin" Best Practices From Design Through Manufacturing with Expert Jay Gorajia*, a 12-part micro webinar series.**

I-007eBooks The Printed Circuit Designer's Guide to...

Thermal Management: A Fabricator's Perspective, by Anaya Vardya, American Standard Circuits
Beat the heat in your designs through thermal management design processes. This book serves as a desk reference on the most current techniques and methods from a PCB fabricator's perspective.

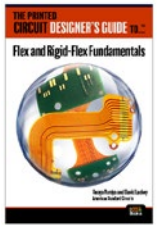


Documentation, by Mark Gallant, Downstream Technologies
When the PCB layout is finished, the designer is still not quite done. The designer's intent must still be communicated to the fabricator through accurate PCB documentation.



Thermal Management with Insulated Metal Substrates, by Didier Mauve and Ian Mayoh, Ventec International Group
Considering thermal issues in the earliest stages of the design process is critical. This book highlights the need to dissipate heat from electronic devices.

Fundamentals of RF/Microwave PCBs, by John Bushie and Anaya Vardya, American Standard Circuits
Today's designers are challenged more than ever with the task of finding the optimal balance between cost and performance when designing radio frequency/microwave PCBs. This micro eBook provides information needed to understand the unique challenges of RF PCBs.



Flex and Rigid-Flex Fundamentals, by Anaya Vardya and David Lackey, American Standard Circuits
Flexible circuits are rapidly becoming a preferred interconnection technology for electronic products. By their intrinsic nature, FPCBs require a good deal more understanding and planning than their rigid PCB counterparts to be assured of first-pass success.

Our library is open 24/7/365. Visit us at: I-007eBooks.com

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