I-Connect007

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DESIGN007 MAGAZINE

THERMAL MANAGEMENT

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Thermal Management

For much of the history of the printed circuit board, thermal management hasn't exactly been top of mind for designers and design engineers. But with the growth of electric and autonomous vehicles, along with telecom and mil-aero applications, thermal management and thermal design processes are becoming mainstream. So, in this issue, our expert contributors share their thoughts on the best methods to "beat the heat."

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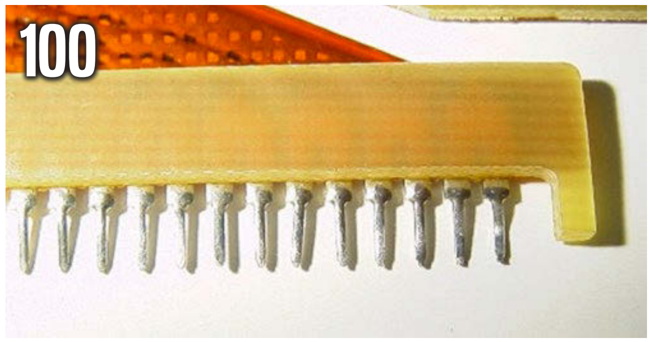
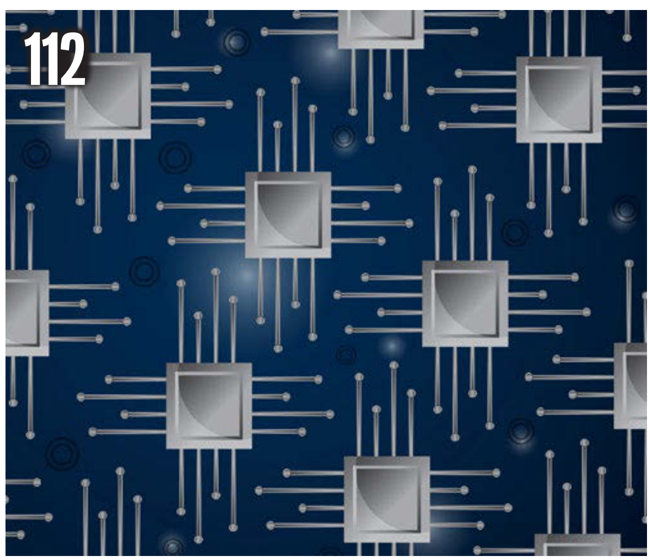




Thermal Management Is a Multi-Pronged Effort

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

Like many of our magazine topics, this month's theme came about as a result of an I-Connect007 survey. We recently asked PCB designers to discuss the challenges they're facing, and quite a few nominated thermal management.

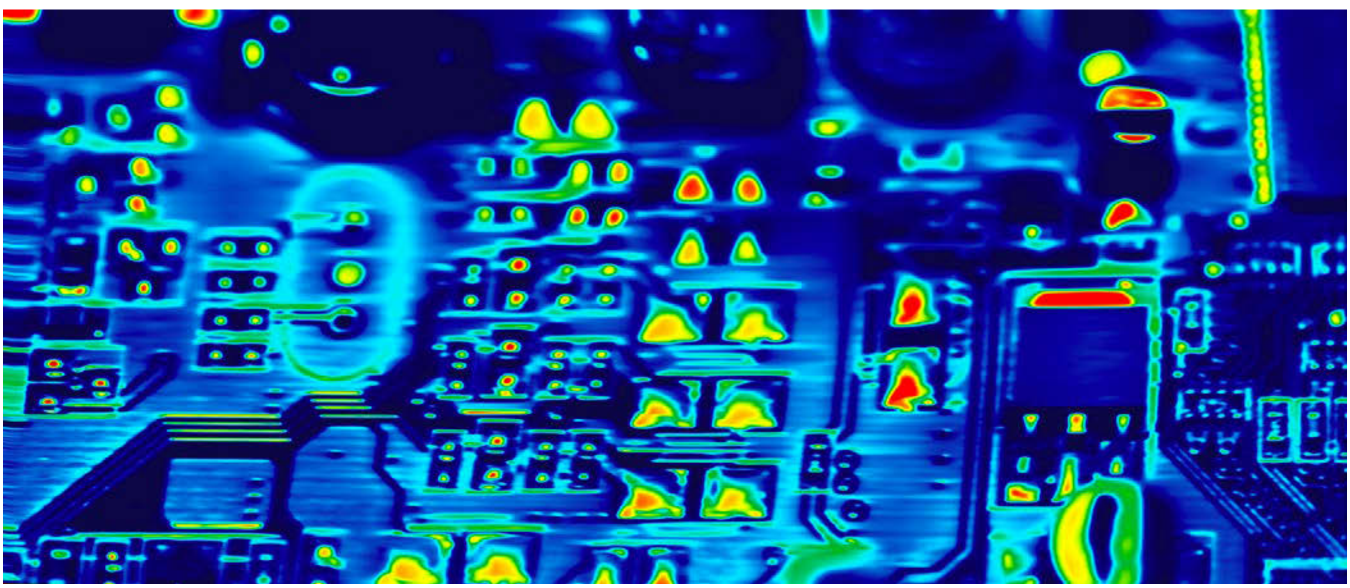
Veteran PCB designers with no experience in thermal matters now find themselves trying to "beat the heat." Unfortunately, there are fewer educational and training resources dedicated to thermal design processes than for, say, signal integrity.

This isn't surprising, given the history of thermal management. For much of the history of the PCB, thermal management hasn't exactly been top of mind for designers and design engineers. There were always more pressing issues that needed to be addressed, such as signal integrity and DFM. The percentage of boards with thermal issues was fairly low; if your company's boards had potential hot spots, you probably had a "thermal person" on your team already.

But with the growth of electric and autonomous vehicles—along with telecom, military, and aerospace, not to mention the explosion of LEDs—thermal management and thermal design processes are becoming mainstream. Are you going to be the "thermal person" on your team?

As we learned from conversations with this month's contributors, there's no simple approach; battling the heat is a multi-pronged effort. Fortunately, technologists now have access to computational fluid dynamics software tools that can eliminate some of the guesswork, and specially formulated thermal laminates that are designed to dissipate heat evenly. Heat sinks and cooling fans are no longer automatic go-to responses to thermal issues.

Technology is catching up with the industry's thermal requirements. But, as Dr. Johannes Adam explains this month, "There is no panacea." There is still no substitute for understanding the fundamentals of heat dissipa-



tion. For instance, is the temperature of a via related to the current going through it? You'll find out in this issue.

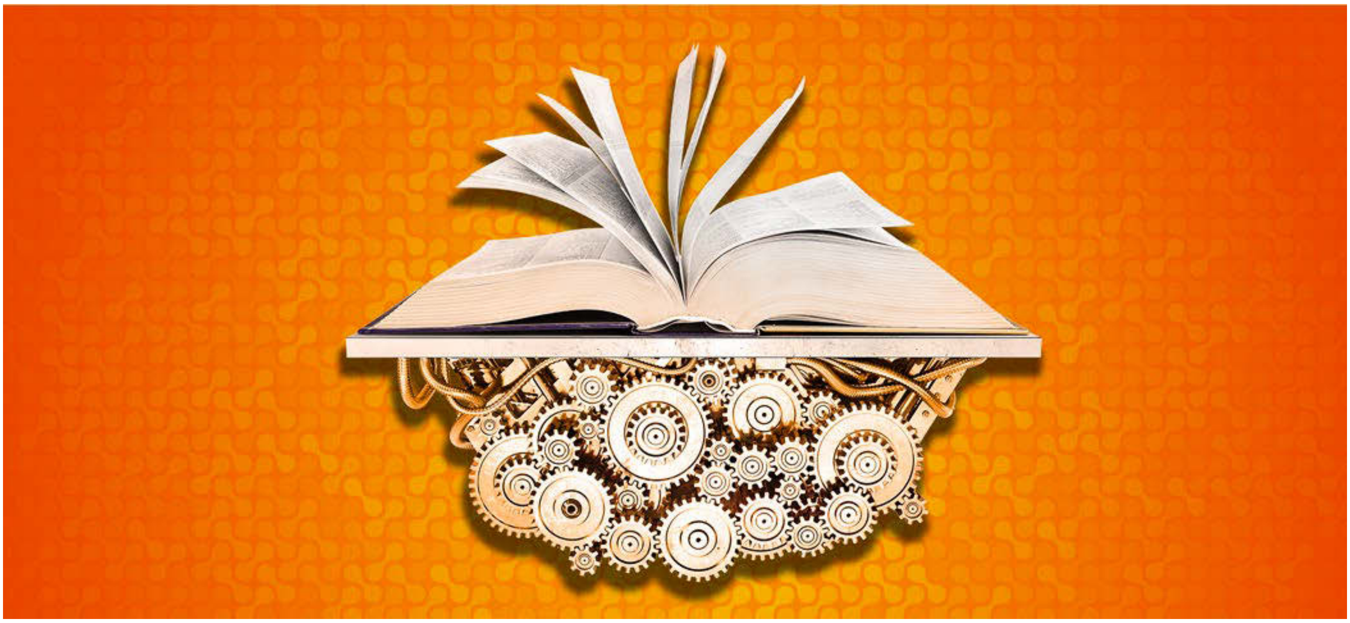
This month, we start by interviewing Mike Jouppi, a pioneer in PCB thermal management. Mike was the champion behind the update of the old IPC current-carrying tables, which lead to IPC-2152. We also have a conversation with Johannes Adam and Doug Brooks, co-authors of *PCB Trace and Via Currents and Temperatures: The Complete Analysis,* who discuss the principles of thermal design and Johannes' new TRM software tool. Doug also brings us an article explaining why trace temperature should not be equated with current density, and Johannes has a feature discussing why thermal engineers should not trust datasheets. Mark Thompson answers five common questions about improving thermal management.

Ventec's Alun Morgan discusses the company's IMS laminates and how they can help mitigate many thermal concerns. Tim Haag shares some advice about how designers can "stay out of the fire." We have a conversation with Jeff Brandman of Aismalibar North America, who discusses the heat dissipation properties of the company's thermal laminates. John Parry of Mentor, a Siemens Business, shares some insight into the FloTHERM CFD software tool and how it can save thermal engineers time and effort. Joe Fjelstad explains why, until recently, thermal issues had been the Rodney Dangerfield of PCB issues. And we have an excerpt from the newest release in *The Printed Circuit Designer's Guide to...* book series, *Thermal Management: A Fabricator's Perspective* by Anaya Vardya of American Standard Circuits.

We also bring you columns from our regular contributors Barry Olney, Alistair Little, Kelly Dack, John Talbot, Patrick Crawford, Dominique Numakura, and Bob Tise and Matt Stevenson. And we have the second half of our fab notes conversation with Jen Kolar and Dan Warren of Monsoon Solutions.

I wrap up most of my September columns by mentioning which trade shows and conferences I'll be attending. But for now, I'm much more likely to see you all in a chat room for a webinar. Speaking of webinars, if you haven't already signed up for Joe Fjelstad's nine-part Flexible Circuit Technology Workshop, now is the time to do so! See you next month. **DESIGN007**

Andy Shaughnessy is managing editor of *Design007 Magazine.* He has been covering PCB design for 20 years. He can be reached by clicking here.



Thermal Fundamentals With Mike Jouppi

Feature Interview by the I-Connect007 Editorial Team

The I-Connect007 team recently interviewed Mike Jouppi, one of the champions of thermal management in PCBs. Mike spent decades working on updating the old IPC current-carrying data, which dated back to the 1950s, and he is the primary architect behind IPC-2152—the standard for determining current-carrying capacity in printed board design. As Mike explained in this wide-ranging interview, even if you're using the latest thermal design software, you still need to have a firm understanding of the fundamentals.

Andy Shaughnessy: Why don't you start off by giving us a little bit of your background in thermal management?

Mike Jouppi: I had an internship when I was a junior in college at Hughes Aircraft Company. They gave me a stack of books and told me to start reading and asking questions, and that's where I started. I was in a thermal analysis group at Hughes, and they used thermal analysis of electronics as a starting point for the new, young engineers who were working in the thermal area.

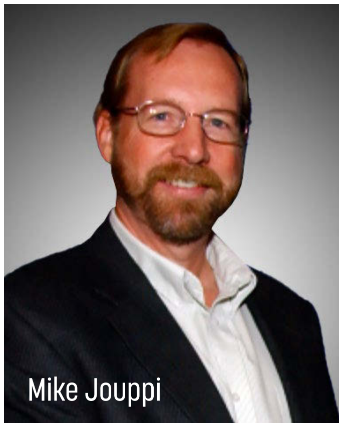
The nice thing about electronics is that you use all the fundamentals of heat transfer. They brought me up thinking about control volumes, which is a fundamental part of thermodynamics, and looking at all the energy coming into a system, all the energy going out, and how that energy gets stuck.

At the time, Hughes Aircraft was a nonprofit corporation, and we had really nice labs with a machine shop just for engineers. We were using a program called CINDA, the Chrysler-improved numerical differencing analyzer, which was a finite difference thermal analysis tool. Typically, our teams would be a mechanical designer, an electrical engineer, a circuit board layout person, and then myself as the thermal analyst. What I would do early is to get the best estimate of the power dissipation for all the components from the electrical engineer and do an early layout showing the power and resulting temperature distribution.

We would look at our worst-case environments, which was often flight or a lab environment that the electronics had to operate in, and we would work with the engineers early in the design to learn where our hotspots were, and then design around that. Getting the fundamentals down really well is what carried

me through, and I use those even now to then. Fundamentals don't go away.

Shaughnessy: What do you see when you look at the industry now? It seems like there's a lot more focus on thermal. Do you see that happening?


Mike Jouppi

Jouppi: The focus on thermal has always been there for the industries in which I worked. The mechanical engineering thermal side worked for a long time on getting a component database that was universal. There were thermal models, a number of different modeling structures for components that people tried to get as a standard structure to work from, and a lot of work was done there, but I didn't see everyone buying into it to where it became a commonly used method for all companies. It would have been nice to have that standardized in such a way that it would address both earth and space environments.

The problem that falls out of that is a lack of understanding of what the thermal resistance values really mean. There are a lot of the thermal resistance values defined in the JEDEC standards. They've done a really good job, and those people realized the importance of each specific thermal resistance associated with the component, such as the component junction-to-case, junction-to-board, junction-to-ambient, etc. They realized that, depending on how you were mounting a component to the board—as well as how many copper planes were in the board—you'd get a different temperature response for the heat transfer. They came up with these different models for looking at different board constructions, which was the same kind of concept that I was trying to introduce with IPC-2152 released in 2009.

That leads to something else that I really would like people to pay attention to—trace heating. I wanted to concentrate on the power that's dissipated in the conductors. A lot of people do not account for the power losses in the electrical conductors, and I've been pushing that everyone should know the conductor losses. There are a couple of reasons why managing power dissipation in traces is important. There's a design rule that deals with parallel conductors. When you have a bunch of traces laying up next to each other—they can be side-by-side or through the stackup—and you have multiple traces that are conducting current, there's a rule for summing the currents and summing the cross-sectional areas to size the traces properly. That rule is very difficult to assess in most designs, and the result is under-sizing traces.

The point is that the charts—both IPC-2152 and the old charts, meaning IPC-2221 and its predecessors—the trace temperatures in those charts represent a single trace being powered up all by itself. When you have parallel conductors, if you look at a really dense board and you have a lot of current running, you have traces running all over the place, and it's next to impossible to employ the design rule of sizing parallel conductors properly. To avoid that problem, you can manage the power losses in the traces and map that power into the board for thermal analysis. You have the best of all worlds. You also begin to further understand if more detailed thermal modeling is needed in certain areas of the design.

Shaughnessy: Are the EDA tools companies starting to pay more attention to thermal? We see FloTHERM from Mentor, Johannes Adam has an Altium interface for his TRM thermal management tool, and there are a few others.

Jouppi: Thermal has evolved a lot over the years. Attention to thermal issues has always been there; it just takes time to develop the tools with a set of resources. The cool thing about this kind of design tool, especially for the big companies, is that they can put the resources wherever they want, and they can get the tools out relatively fast. The key is to have a community that is asking for it.

I've worked directly with some big and small companies, asking them to develop certain tools, and I was always able to get some advancement on those things for the tools that I was using. They're out there to make a profit, and they will change wherever enough people are asking them to go. The push needs to be back on the design teams to ask for their specific needs.

Johannes Adam and I have been friends since about 2002, and I've used a lot of tools for solving various thermal problems. His tool is one of the best I've used for trace heating. However, it is just focused on the circuit boards, whereas a lot of the bigger tools are focused more on the system level, and then they may or may not have features that will address the board level. It takes those larger companies time, and pressure from the people buying their tools, to incorporate the different features that are needed to solve the various thermal issues that come up in designs. Overall, the EDA industry has some awesome tools. I envision fully automated artificial intelligence features in the future EDA tools.

Shaughnessy: Other than using the completely manual way, putting down heat sinks and fans, what advice would you give somebody who is new to doing thermal design?

Jouppi: Understand your design from the fundamental side. I use a control volume and spend time defining all of the sources of power into the board and the heat transfer paths into and out of the board. Model those powers as accurately as possible to represent the physical design. I talked to some people who account for the power losses from their traces and asked how they model those losses. They would smear it over the entire board in their thermal model, and that's at least one step closer, but you could possibly be missing a hotspot.

It's important to understand the component thermal resistances and associate those numbers to your hardware. There's so much to gain from looking at the hardware and how it's mounted, as well as knowing what the lead materials are, the thermal resistance through those leads, how it is mounted to the board, and what the gap between the component and the board might be. Do all your homework by reading papers that people have written, fully understanding every aspect of the design. Then perform thermal testing to validate your models. There is a lot to learn from testing. That is a topic in itself.

Shaughnessy: As always, communication is king. If you have any thermal problems, then your designers should talk to the CAM person.

Jouppi: We're always coordinating with the CAM person, but the problem is that the whole team is under a time crunch. Early temperature predictions help to minimize changes to the layout and keep the design team on schedule.

Shaughnessy: IPC-2152 is pretty central to all of that.

Jouppi: The idea is central to it, but IPC-2152 isn't used the way I hoped it would be used. I wanted to see people use IPC-2152 as a baseline configuration and used to create trace heating charts for their own specific design configurations. The nice thing about IPC-2152 is that it's a well-defined set of numbers that were put together through testing and documentation. There's a large appendix that has a lot of information about the testing we did, as well as the history of the previous charts that were last published in IPC-2221.

When IPC-2152 was put together, we had a long list of items to investigate. We prioritized that list and worked through what we could. The appendix was developed so that we could add to the document over time. The main area was trace heating for internal and external traces, based on temperature measurements following IPC-TM-650 2.5.4.1a.

We also wanted to look at the impact of copper planes on trace temperatures and illustrate the temperature change that occurs when you introduce a copper plane and how the distance from the trace to the copper plane would impact the trace temperature.

In addition, we wanted to address working with vias and how much current you can put through vias and via patterns. Many people still use rules of thumb to say one amp per via or two amps per via, but I wanted to see us do research to define current in vias and microvias. We just didn't get there.

Happy Holden: I'd like you to relate the first time the two of us ever talked when I first met you in Colorado 35 years ago. I reviewed these measurements on a satellite or some kind of space project you were working on, as well as the temperature of these traces, and they didn't match the IPC standards. Eventually, that led to you becoming the chairman of IPC-2152, but I haven't heard the whole story.

Jouppi: I don't think it was quite that long ago, but I was working at Lockheed Martin on a satellite project called Stardust. It was the first time in my career as a thermal analyst that an electrical engineer provided power dissipations for the traces in the design in addition to the component powers. It was a significant amount of power, and it changed the design.

I asked the designer how he calculated the power values, and that took us to trace sizing charts in IPC-D-275, a predecessor to IPC-2221. When I read IPC-D-275, it stated that vacuum environments should be taken into consideration, but it didn't say anything about where the data came from to create the charts or how to take into account the vacuum (space) environment, so I called IPC. I ended up contacting a fairly new IPC employee at the time, John Perry, to ask how the charts were derived.

John told me that he talked to Dieter Bergman. All he could find was a technical paper written by Dr. Charles Jennings from Sandia Labs, and it was published in an IPC technical paper. We were able to get that paper, and I just followed what they had done. I ran some experiments, got some data, and created both internal and external traces on these new boards. The biggest revelation was to see the difference between the internal trace temperatures and what was published in IPC-D-275, and what they're giving you for the internal traces there.

I wrote a paper and submitted that to IPC, and presented the paper at an IPC conference. Back then, Ralph Hersey was the chairman of the task group that dealt with those charts, and he'd also been doing a lot of work trying to figure out where the numbers came from. At this meeting, he stated that the testing that I did validated the old charts and that we should go forward, using them as they were. I raised my hand and said, "No, I don't think that my paper really validates this. It does the opposite." That didn't go over that well with Ralph. He ended up letting go of that leadership role, and I ended up taking over the task group. I also ended up talking to a designer named Jim Yohe in California who had come across an old Navy report that documented the charts in IPC-D-275.

I ended up calling the Navy and asking them, and they said they didn't have it, but they said to contact the National Archives. I did, and I was able to find that old document that had the original data. It was work that was done by the National Bureau of Standards, and it was funded by the Navy in the early 1950s. Printed circuits were a new technology, and a study was needed to assess how much current could be applied to the traces.

There were no multi-layered boards at the time. They collected data on a bunch of different two-sided board configurations, with different board thicknesses, materials, and copper thicknesses; some of the boards had copper planes on one side, and some did not. They took all of those configurations as one data set and drew a line through them to create the external trace sizing chart that was last published in IPC-2221. The problem was that this information didn't get shared with all of the design community. What people don't realize is that those charts represented the external trace design guidelines for the current and cross-sectional area and temperature rise.

To this day, I've never been able to truly track down when the multilayer board internal trace data charts came out. There's no data that went with those. All they did was take half the current from the external ones and say, "That's what the limit will be for the internal ones."

But there were two people at Hughes that did some curve fitting for the external charts and the internal charts, and the difference was a factor of two on the internal ones, so then it suddenly made sense that nobody really did any internal trace testing to come up with the charts. They decided that things would run hotter inside the board than outside, and they took half the current.

Holden: It's crazy. I went through our design manual and relayed some of the numbers back to you, where you gave me the condition. I said, "The data in this chart comes from HP labs, but there's a reference on the bottom from an Air Force ManTech program. Somehow, HP labs had also gone back to the military." But I couldn't help you because they didn't know anything about the IPC standard. We weren't allowed to use IPC standards.

People were running into a fistfight with me because talking about those curves not being correct was totally unacceptable as if they were handed down by God on golden tablets. Nobody knew where they came from, but nonetheless, don't violate them. And it went from one or two pages up to 70–80 in the final IPC-2152.

Jouppi: And that's just touching the surface. I had a long list of all the things that I thought that we should still do. But when you're working with volunteers, it goes extremely slow, and only a few find time to contribute. Everybody was overworked during those years. I teamed with the University of Colorado in Denver, and we wrote a grant proposal to the National Science Foundation (NSF). After being turned down for the NSF grant to fund the work, I ended up creating my own lab, collecting data to validate some previous testing, and developing a software tool to manage the data. Some of the data that was collected went into IPC-2152.

Holden: I was at Mentor when they purchased the software tool Simcenter FLOEFD, so I used it because I was working for the vice president, and everyone were either electrical engineers or software people. The software came from the Soviet Union. They didn't write it, but they adapted it from a Russian worker. They asked, "What can we do with this three-dimensional computational fluid dynamics?"

I was working with it on a Dell computer, and the finite element analysis would give me results within minutes. I said, "Is this software

One of Mike Jouppi's recent pieces of art: a tree stump brought to life as an owl spreading its wings.

for real, or is somebody pulling my leg?" because you can't do three-dimensional fluid dynamics on a Dell computer using an Intel processor. It takes a Cray supercomputer to do that kind of work. And they said, "No, the Russians figured this all out because they didn't have Cray computers." I responded, "This is really something. I've never seen three-dimensional finite element computation like this."

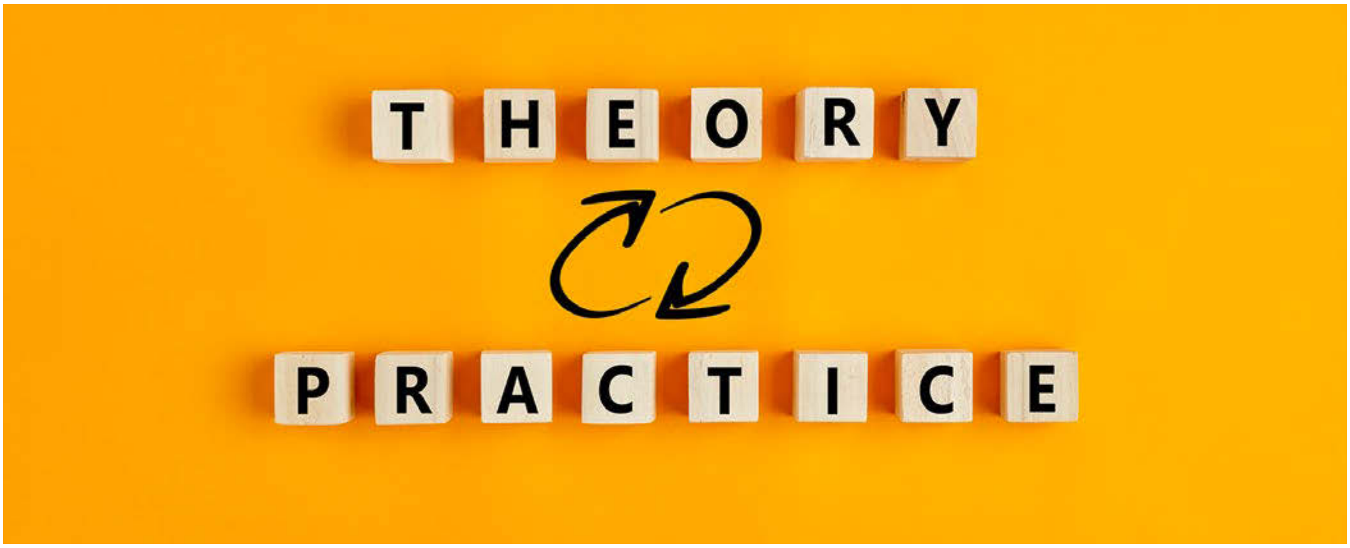
Jouppi: They did a great job. Russian mathematicians are always incredible.

Holden: What are you doing now?

Jouppi: I am semi-retired. I haven't been taking on any work, and I've been doing a lot of artwork. Out of high school, I wanted to be an artist, but I looked at all these great artists who were starving, and I didn't want to have that kind of lifestyle. I chose engineering to provide a lifestyle that would be reasonable, and it has taken until now to really start digging into my artistic side.

Shaughnessy: This has been really good, Mike. We appreciate you taking the time to talk with us. Thank you.

Jouppi: It was fun. Thank you. **DESIGN007**



Thermal Management: Don't Believe the Datasheets

Feature by Dr. Johannes Adam
ADAM RESEARCH

We all know that the temperature of components and materials in a PCB must not exceed a limit between 100°C and 150°C. When the environment is already hot or when heat dissipation is impeded, it is important to be aware of this as early as possible so that appropriate action can be considered and initiated. Compliance with the thermal specifications is not everything, but it is one of the necessary steps in electronics development.

Simple Temperature Predictions: Likely Wrong

What are some methods for predicting the temperature of a PCB? You could take the datasheet of the component and search for temperature information (e.g., for the maximum power dissipation P_{max} or the junction-to-ambient thermal resistance $R_{\Theta J\text{-}A}$). Both are in relation to each other via $T_{max} \approx T_A + P_{max} \times R_{\Theta J\text{-}A}$. The formula is simple but, unfortunately, not to be recommended because "ambient" really includes everything around the component, from the pad to the vias, and the design of the layers up to the air. We can easily imagine that $R_{\Theta J\text{-}A}$ cannot be a "material constant" of the component. On a good thermally conductive copper plate, the same heat source (the component) would have a much lower temperature than on a plate made of FR-4 and thus a different J-A thermal resistance. The PCB on which the datasheet is based plays an important role.

The test environment for the datasheets is usually based on a PCB with a minimalistic design, according to JESD-51 [1]. A review with examples is given by Edwards and Nguyen [2]. Due to the deviation between the real environment and the test environment, $R_{\Theta J\text{-}A}$ must not be used for temperature predictions (Wong [3] p. 4). RΘJ-A is used rather as an indicator for comparing the thermal properties of different components, which are tested under comparable environmental conditions. There is another often misused version of thermal resistance, derived from the Fourier differential equation of heat conduction, namely that for a plate according to R_{th} = thickness / (area x thermal conductivity). This simplification is only valid

for a one-dimensional adiabatic heat transport through (e.g., a thin heat conducting sheet), but it cannot describe the heat spreading in the board (not even in a homogeneous plate). Therefore, it is obvious that there is no panacea for temperature prediction.

Simulation: A Better Way to Predict Temps

A numerical analysis can cover both the big picture and the details for better prediction. What makes a PCB a complex geometry is the sequence of copper layers and prepregs, the stackup, the pattern of the copper tracks in the layers, the artwork or layout, and the placement of the components. Let's look at a few examples. These calculations were performed with Thermal Risk Management (TRM) software, which was developed by my company ADAM Research and can be used by the users of all ECAD systems by importing standard files (e.g., Gerber, drill files, netlists, text and Excel files). There are even export and import wizards for Altium Designer.

It is even possible to use TRM with no layout data at all, for example, for preliminary placement studies or technological studies. The board will be calculated in three dimensions, even if desired as transient and with or without electrical sources (see the article by Doug Brooks in this issue). That will take between one and a few minutes. Much attention is paid to the user interface to have as much as possible in view at once, both in the input and in the results. It is truly easy to use and a teaching and learning tool for the EE (Figure 1).

Examples

In the first three examples, the value of the power dissipation is always 1 watt for the purpose of comparison, the PCB is always in "still air" (i.e., free convection), and the ambient temperature is always 20°C. Using the calculated component temperature, a thermal resistance "case-ambient" $R_{th,C\text{-}A} = (T_{case} - T_{amb})/1W$ can be read off directly. The fact that this value differs from board to board shows that also $R_{th,C\text{-}A}$ values in datasheets are not suitable for individual temperature predictions.

1. Arduino

The two-layer Arduino board is a standard Eagle [4] software installation. Solder mask and silkscreen do not need to be imported into the thermal model and are used here for illustrative reasons only. We only charge the central component IC3. Around the component, there is

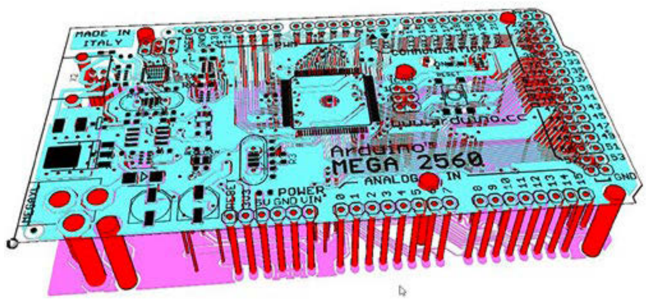


Figure 2: View of the TRM model of the two-layer Arduino board with solder mask and drilled holes. In the vertical direction, the geometry has been expanded by a factor of 10. The size is 100 mm x 53 mm. The components are hidden.

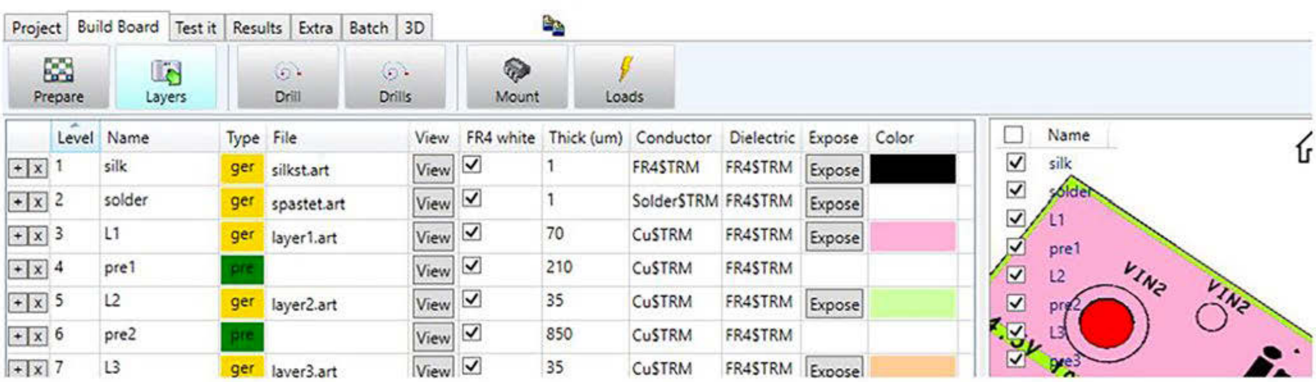


Figure 1: The TRM user interface.

a nearly star-shaped arrangement of traces on top. With respect to the bottom, IC3 lies above a bundle of tracks surrounded by a flooded rest. Nevertheless, the cooling is not very good.

The calculated thermographs of the top and bottom are shown in Figure 2. The shape of the isotherms is very irregular, and the yellow and green sections end abruptly. The heat spreading does not manage to distribute the heat over a larger surface.

The reason can be seen illustratively if the temperatures are superimposed on the layout in the area around the component (Figure 3), the heat spreading ends where the gaps between the traces form an FR-4 barrier for the heat flow. This is not only true for the top layer, but also for the bottom. The overall result is then the superposition of the two structures (Figure 4).

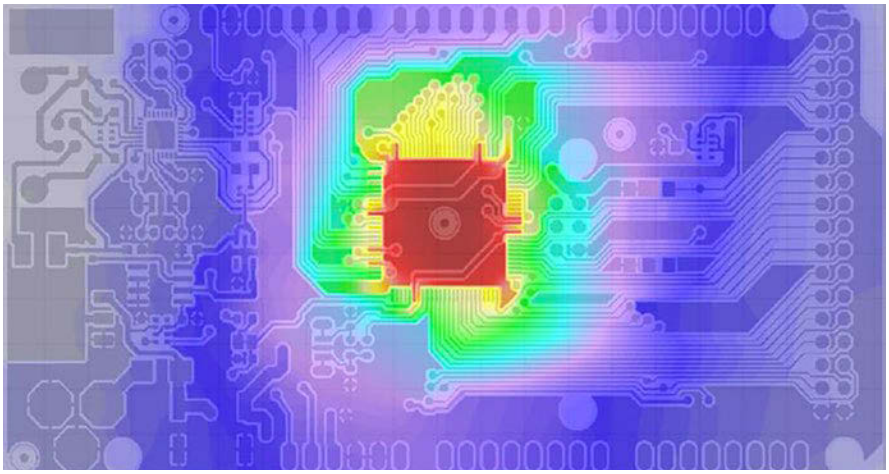


Figure 4: TRM calculated temperature field for the Arduino model with superimposed top-layer artwork. The parallel running traces can obstruct (left) or improve (above) the heat flow.

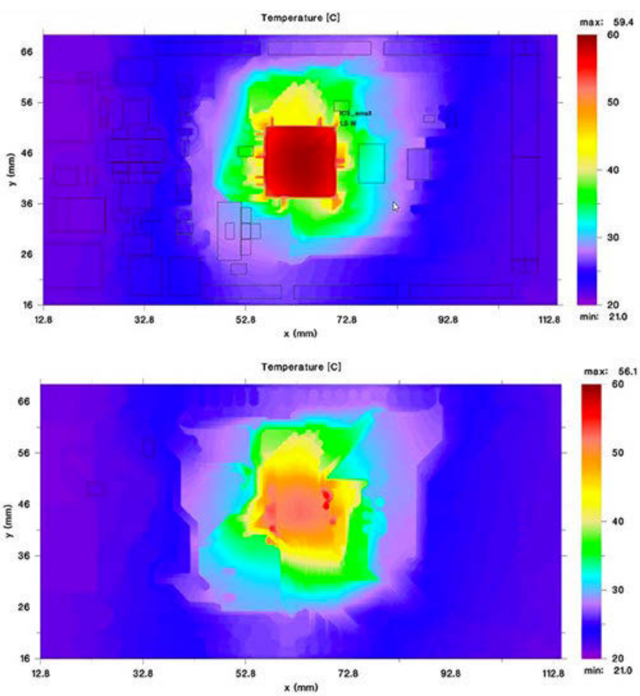


Figure 3: Calculated thermographs of the Arduino board for the top (above) and bottom (below). $R_{th,C\text{-}A}$ would be about 39 K/W.

2. RS-ChipKit Max32

This board is a standard example of a DesignSpark PCB [5] installation. The four-layer board ChipKit Max32 by Digilent is a prototyping platform that demonstrates the power of the Microchip PIC32 microcontroller. The board is the same size as the Arduino board. On top and bottom, around the central microcontroller PIC32MX795F512L (= IC2), the tracks are orthogonally aligned like a woven pattern. Both inner layers are thoroughly flooded (Figure 5).

Because of the two massive inner layers, the shape of the calculated thermographs closely approximates that of circular isotherms from the theory of heat spread. The board is the same size as the Arduino, and even though the

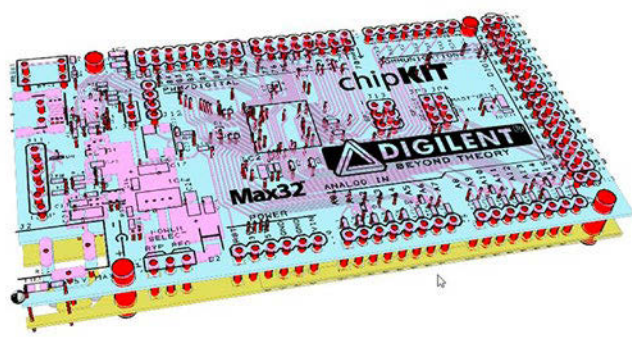


Figure 5: Diligent evaluation board ChipKit Max32. The top layer in pink, first inner layer blue, and second inner layer in brown.

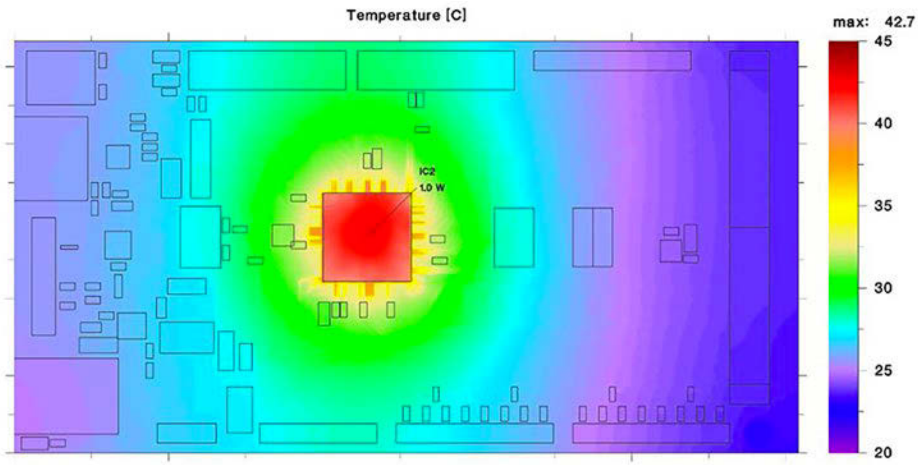


Figure 6: Top layer temperature. Due to the two flooded inner layers, the isotherm is oval-shaped.

component is smaller, the temperature here is 20 K lower. This is the effect of heat spreading in the inner layers. Without the two inner layers, the temperature would climb to 80°C (Figure 6).

3. EVB-USB580x_A

This board is one of the standard examples of an Altium Designer [6] installation. EVB-USB5806 [7] is a demonstration and evaluation platform for the 6-Port SS/HS USB Smart Hub on a four-layer PCB. Below U1, there is a Cu pad that mates with the internal heat slug. The pad is only in contact with GND and can only dissipate heat there. In the Internal2 and Bottom layers, potential separations limit the heat spreading around U1 (Figure 7).

The result of the calculations is given in Figure 8. The circular isotherms on top are the result of the full surface copper in i1 (GND).

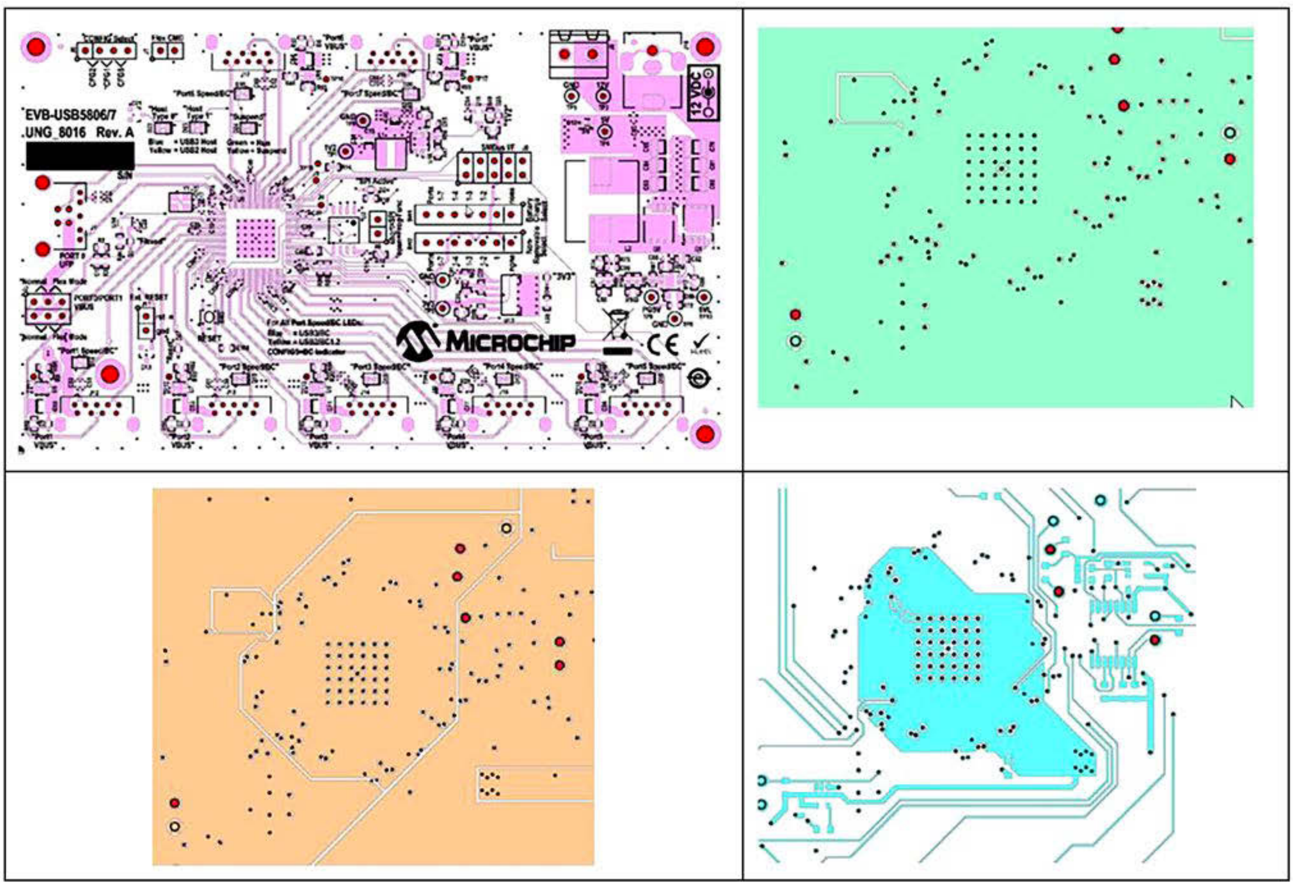


Figure 7: EVB-USB580x_A. General view of the top in pink, detail inner layer 1 (GND) green, detail inner layer 2 in brown, and detail of bottom in blue.

Rogers' Laminates: Paving the way for tomorrow's Autonomous Vehicles

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RO3003G2™ Laminates	Best in class insertion loss / most stable electrical properties for 77 GHz antennas
RO4830™ Laminates	Cost-effective performance for 77 GHz antennas
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ANTENNA	
RO4000 Series Circuit Materials	Low loss, FR-4 processable and UL 94 V-0 rated materials
Kappa™ 438 Laminates	Higher performance alternative to FR-4

To learn more visit:
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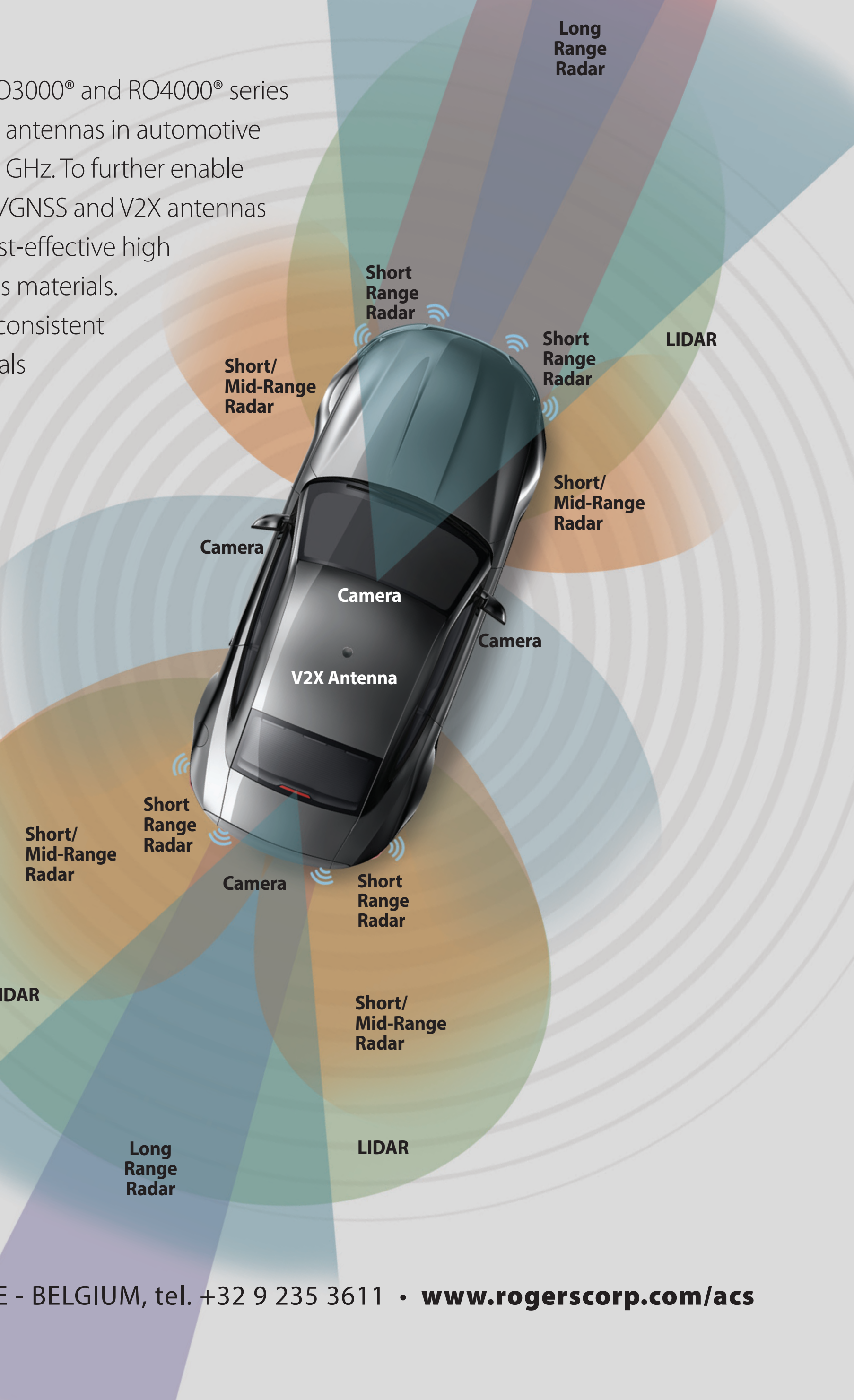

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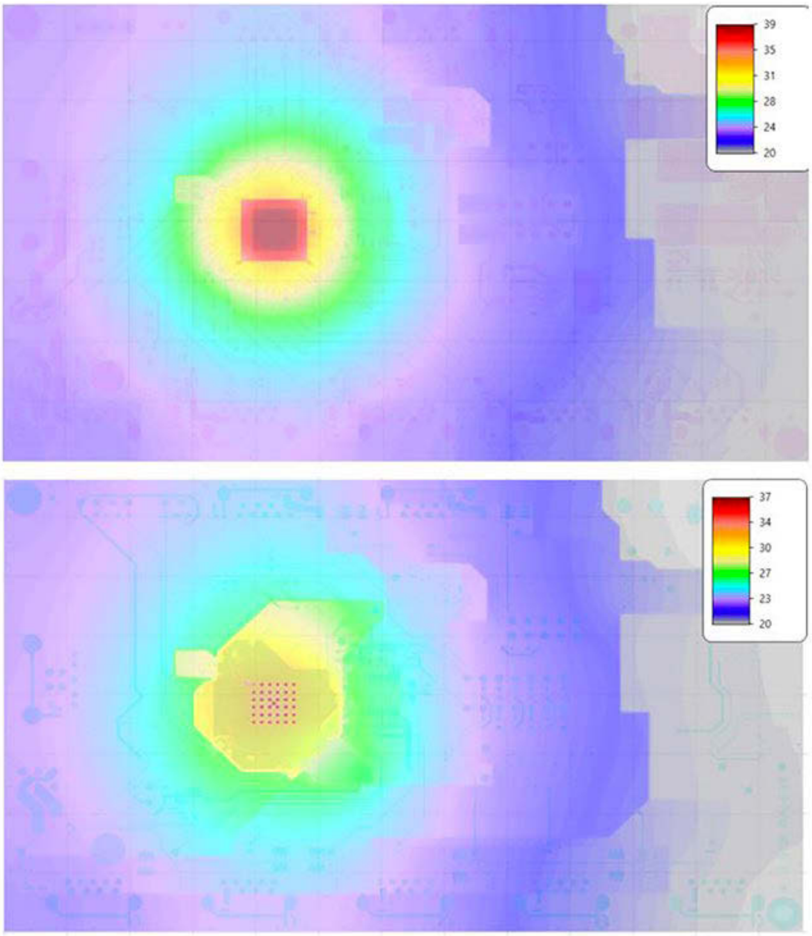

Figure 8. Calculated thermographs from the EVB-USB580X_A model superimposed on the layout images. The top layer (above) and bottom layer (below). The heat dissipation by PTH is poor.

But the geometrically limited heat spread in i2 and bottom impairs the temperature level. The rectangular pattern of red dots below U1 in the bottom layer is the PTH. They roughly show the temperature level of the component, not because they dissipate heat well, but because they dissipate it poorly and because the heat is in a dead-end. If the heat dissipation were good, the outer ring would have to be much colder. The one via in the upper left corner is an exception and is a customized construction on the bottom.

4. ISL8240MEVAL4: Comparison With Observation

Since there are infrared images and an article (Taranovich, 2015) [8] for the ISL8240MEVAL4Z [9] assembly, it is suitable for comparison with the simulation. The layout was created with Cadence Allegro [10]. The comparison of simulation and experiment is very satisfactory (see details of the model [11]). Not only the maximum temperature is properly calculated, but also the edges and ridges caused by the layout of the inner layers are in their correct position. By the way, the "standard" method [12] is the wrong approach here (Figure 9).

Final Thoughts

Temperature also affects the electrical conductivity of the traces and the overall performance of the components ("derating") and the final product. (We intentionally omitted electric heating of traces in this article; see Doug Brooks' article in this issue. High-current applications in high ambient temperature can also be simulated with TRM, also as a mission profile with a time sequence of switching states). Early confidence that the components and traces will meet the temperature limits is one of the hallmarks of serious product development.

As the person responsible for heat dissipation, you can use the resulting graphs and tables (virtual thermographs) to clearly illustrate which actions are to be taken (or not) and why. Do not just believe that it will work out; you just have to want it and realize that good thermal design is cost-free. Even a prototype costs more money than just ordering the PCB sample online, and many bugged prototypes cost too much.

Our plea as a software provider is, of course, that thermal management should be accompanied by numerical simulation and that this should set the parameters for good solutions. But thermal management is also an interdisciplinary task because both the specifications and the solutions come from different directions. There is no panacea, and often, the development department is

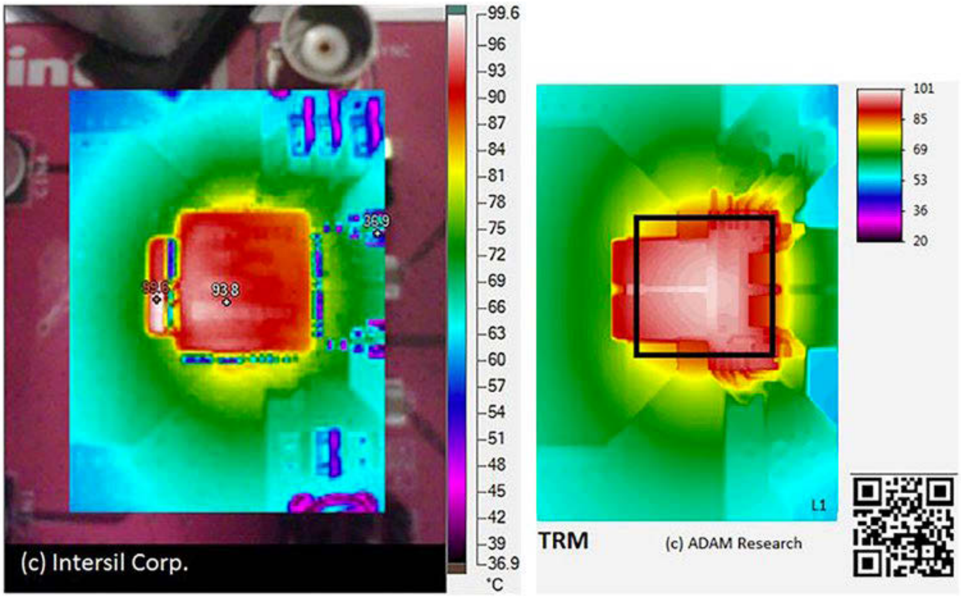

Figure 9: Thermography (left) and the simulation image of the top layer (right).

caught between specifications, costs, design, marketing, reliability, and feasibility.

Think of the heat right from the beginning of development and communicate with internal and external development partners. Also, question any kind of estimate. "We have always done it this way" does not apply. Only reasonable communication can lead to a reasonable solution strategy.

It is impossible to predict when the ROI of a simulation software will be reached. For some users, this is already the case with the first project; usually, it should be the case with 2–3 development projects per year.

Unfortunately, electronics cooling is rarely offered as part of an electronics engineering university curriculum. TRM software can also be an educational tool. Even without importing layout data, you can create, calculate, and adjust a dummy with simple rectangles, circles or digital drawings. That is why TRM is also a prototyping and technology tool. You are free to choose the geometry, the layer structure, the materials, the thermal load by components and currents, and the cooling.

Since time is money, you should also know that the computing time, for example, with the ISL board, is about four minutes on my laptop. The duration of the measurement in the lab would be about 10 minutes until the steady-state is reached. Simulation can also be faster than real-time. **DESIGN007**

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Dr. Johannes Adam is the founder of ADAM Research.

Stackup Planning, Part 6: Impedance Variables

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Interconnect impedance is a trade-off between the variables, including trace width, trace (copper) thickness, dielectric thickness, and dielectric constant. If you need to include differential impedance, trace clearance also comes into play. For minimum crosstalk, the coupling must also be considered. Plus, one needs to bear in mind the exact materials that are stocked by your preferred PCB fabricator. Determining the correct configuration to achieve the desired impedance is not as simple as clicking an impedance goal-seeking button. But rather, one should weigh up all the pros and cons of changing each variable and make an informed decision.

Impedance is the key factor that controls the stability of a design; it is the core issue of the signal integrity methodology. The substrate is the most important component of the assembly and needs to be planned correctly to maintain consistent impedance across layers, avoid unintentional signal coupling, and reduce electromagnetic emissions. In this month's column, I continue with Part 6 of my stackup planning series and look at the correct process of stackup impedance planning and the consequences of bad decisions.

Goal seeking is a function that is used to find an unknown value from a set of known values. If you know the answer, then the algorithm will fix all but one variable and hone in on the desired result. But keep in mind that there is no AI involved here. The software does not take all the possible variables into account as the designer would.

PCB fabricators know their production process extremely well, and their manufacturing

expertise is invaluable to produce a high-performance substrate. However, they are not signal integrity gurus; most know very little about high-speed digital design. Why leave critical impedance selection decisions to them when the product designer has far more knowledge about the requirements of controlled impedance? The people who do not understand impedance control like goal-seeking because they can push a button and get a quick answer, albeit the wrong configuration in most cases.

Let's take a look at the impedance variables and how they interact.

1. Trace Width

There are three main considerations for trace width selection:

a. Minimum manufacturable width, which is generally 4 mils. 3 mils can be achieved, but yields drop, and costs increase.

b. Minimum spacing between BGA balls; in most cases, 4 mils will get you through.

c. Current handling, which is not an issue for digital design. For power distribution, the trace may need to be thick to accommodate the required current.

Trace width increases as impedance decreases (Figure 1). Start with the highest impedance technology first, which is typically 50-ohm single-ended, 100-ohm differential set at 4 mils.

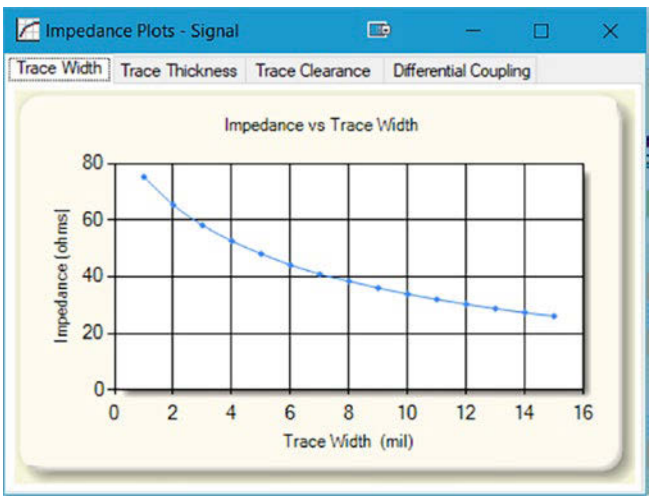


Figure 1: Impedance vs. trace width (iCD Stackup Planner).

2. Trace (Copper) Thickness

The main considerations for trace copper thickness selection (Figure 2) include:

a. Copper on either side of a core material must be the same thickness.

b. Copper plating (typically 1 mil) is added to outer microstrip copper foil hence traces due to the through-hole barrel plating.

c. Current handling capability at low frequencies. High-frequency current flows in the outer skin of the copper.

Typical values are 1 oz (1.4 mils) and ½ oz (0.7 mils). 1.4 mil is a good first choice unless you have a high layer count stackup.

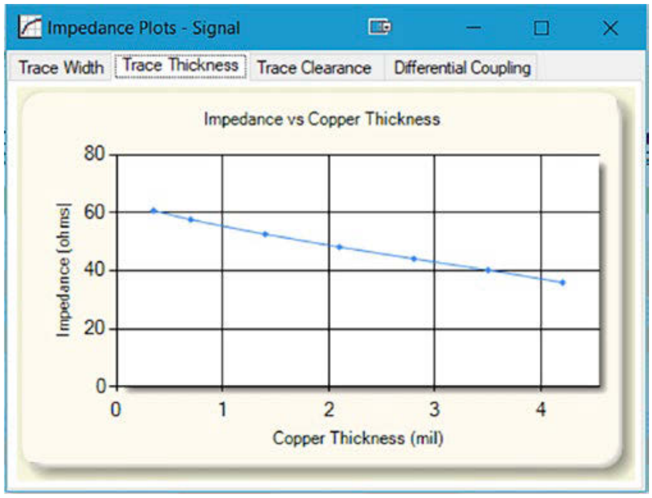


Figure 2: Impedance vs. copper thickness.

3. Trace Clearance (Separation)

Trace clearance determines the differential impedance:

a. Differential signals that are closely coupled will operate mainly in the differential mode with some common-mode radiation from imbalances in the signals.

b. If the two traces are separated enough to prevent coupling then both act as single-ended signals. A 100-ohm differential pair becomes two individual 50-ohm single-ended signals.

Begin with 4-mil clearance and expand this out to where the impedance levels off (10–12

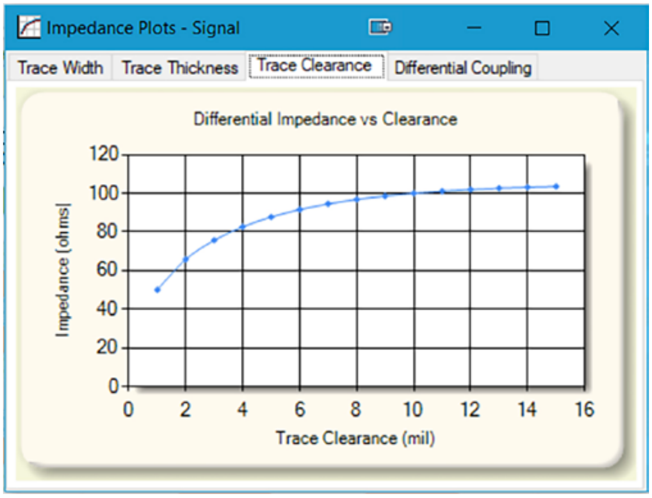


Figure 3: Impedance vs. trace clearance.

mils in Figure 3) if necessary. Close coupling will provide the most routing space.

4. Trace Coupling

Although trace coupling is not strictly speaking an impedance variable, it should be considered during the planning stage. The combination of trace clearance and dielectric thickness provides the point of coupling (12 mils, in the case of Figure 4). At this point, differential pairs are no longer coupled, and individual parallel traces become vulnerable to crosstalk. Use the point of coupling to define the crosstalk trace clearance constraints.

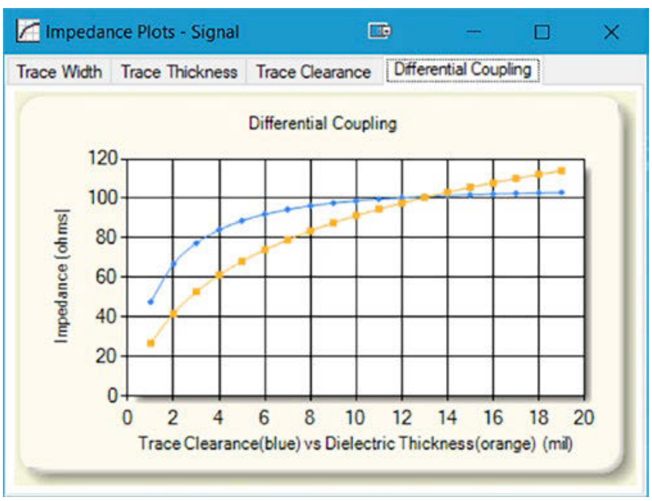


Figure 4: Impedance vs. coupling.

5. Dielectric Thickness

The main considerations for dielectric thickness (Figure 5) include:

a. All signal layers should be adjacent to and closely coupled to an uninterrupted reference plane. This provides the shortest loop area and the lowest inductance for the return current path.

b. The minimum dielectric thickness is determined by the selected material glass style.

c. A wider weave fiberglass may cause skew in differential pairs at high frequency (> 10 GHz), converting differential mode current to common mode—hence radiation.

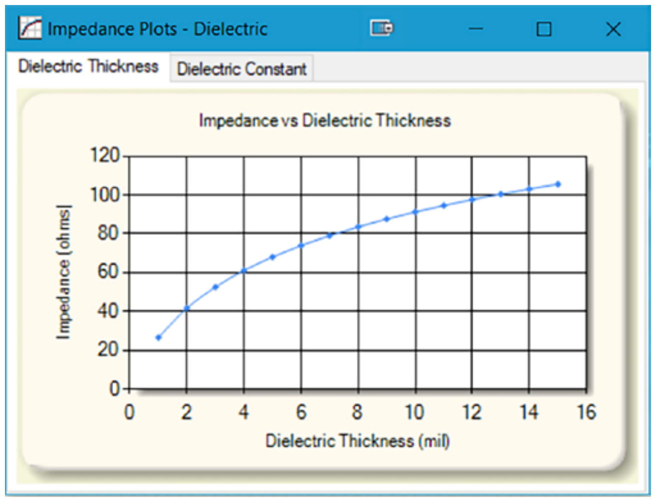


Figure 5: Impedance vs. dielectric thickness.

Glass weave skew and pile unevenness can be prevented by using two plies of 1067 glass prepreg combined. Do not use 106 or other wide gap glass styles. 1067 glass is typically 2.5–3 mils.

With regard to stripline (inner layers), the thinnest dielectric should be closest to the GND plane return path. In a dual stripline configuration, the dielectrics closest to the planes should be thin, and the dielectric between the signal traces should be thickest, which also reduces broadside crosstalk.

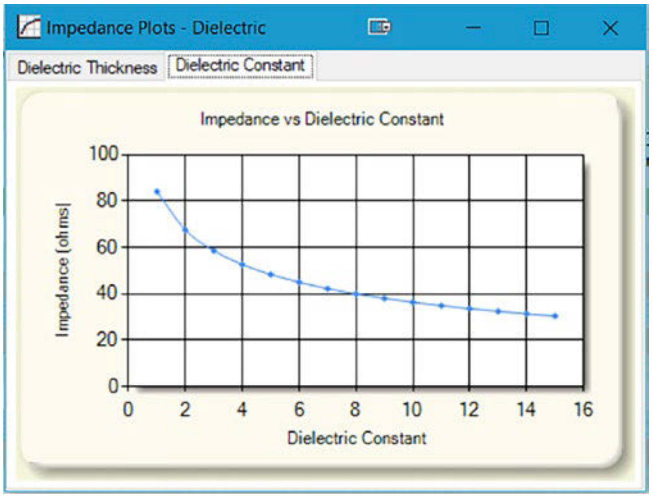


Figure 6: Impedance vs. dielectric constant.

6. Dielectric Constant

The main considerations for dielectric constant, or Dk, (Figure 6) include:

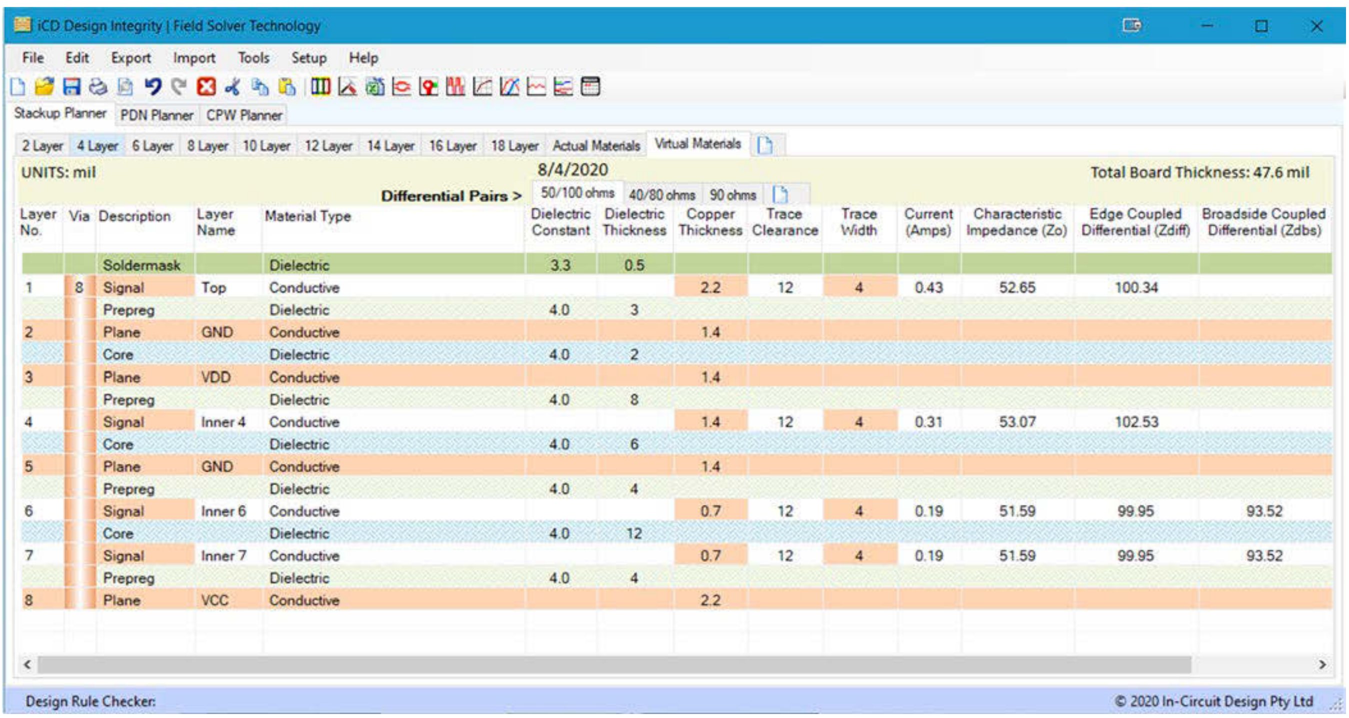
a. A dielectric constant of 4.3 is typical.
b. Low loss materials tend to have lower dielectric constants (~3).
c. Microstrip (outer layer) dielectric should have lower Dk to slow the velocity of propagation of the EM wave to match the stripline speed.
d. A high dielectric constant creates the most planar capacitance, which is used to lower the impedance of the power distribution network. This is good for plane-to-plane coupling.

Start with a value of 4, but if the frequency is 10 GHz or more, use 3 as a starter.

Taking all of the above into account, one should first plan the stackup using virtual materials (Figure 7) to get in the ballpark. In other words, pick an appropriate value, and then hone in on these values with the actual materials stocked.

In this case, I am designing the stackup for three different technologies (50/100-ohm digital, 40/80-ohm DDR3, and 90-ohm USB). The dielectric constant and thickness, together with the trace width and clearance, need to provide near correct impedances for these three technologies (Table 1).

A characteristic impedance of 40–60 ohms is typically used for a digital design. However, this value becomes more critical as the edge rates become faster. Also, different technologies have their specific impedance requirements. For example, Ethernet is 100 ohms and USB 90 ohms differential, and DDR2 memory is


iCD Design Integrity | Field Solver Technology

File Edit Export Import Tools Setup Help

Stackup Planner | PDN Planner | CPW Planner

2 Layer | 4 Layer | 6 Layer | 8 Layer | 10 Layer | 12 Layer | 14 Layer | 16 Layer | 18 Layer | Actual Materials | Virtual Materials

UNITS: mil 8/4/2020 Total Board Thickness: 47.6 mil

Differential Pairs > 50/100 ohms | 40/80 ohms | 90 ohms

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
		Soldermask		Dielectric	3.3	0.5							
1	8	Signal	Top	Conductive			2.2	12	4	0.43	52.65	100.34	
		Prepreg		Dielectric	4.0	3							
2		Plane	GND	Conductive			1.4						
		Core		Dielectric	4.0	2							
3		Plane	VDD	Conductive			1.4						
		Prepreg		Dielectric	4.0	8							
4		Signal	Inner 4	Conductive			1.4	12	4	0.31	53.07	102.53	
		Core		Dielectric	4.0	6							
5		Plane	GND	Conductive			1.4						
		Prepreg		Dielectric	4.0	4							
6		Signal	Inner 6	Conductive			0.7	12	4	0.19	51.59	99.95	93.52
		Core		Dielectric	4.0	12							
7		Signal	Inner 7	Conductive			0.7	12	4	0.19	51.59	99.95	93.52
		Prepreg		Dielectric	4.0	4							
8		Plane	VCC	Conductive			2.2						

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Figure 7: Virtual materials for microstrip, stripline, and dual stripline configurations (iCD Stackup Planner).

Target Impedance	Tol +/-%	Layer No.	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
50/100 ohms	10	1	12	4	0.43	52.65	100.34	
50/100 ohms	10	4	12	4	0.31	53.07	102.53	
50/100 ohms	10	6	12	4	0.19	51.59	99.95	93.52
50/100 ohms	10	7	12	4	0.19	51.59	99.95	93.52
40/80 ohms	10	1	12	6.5	0.62	41.61	79.47	
40/80 ohms	10	4	8	6.5	0.44	42.9	79.88	
40/80 ohms	10	6	15	6.5	0.27	40.6	79.9	72.23
40/80 ohms	10	7	15	6.5	0.27	40.6	79.9	72.23
90 ohms	10	1	6	4	0.43	52.65	91.96	
90 ohms	10	4	6	4	0.31	52.81	91.58	
90 ohms	10	6	6	4	0.19	51.46	92.55	93.4
90 ohms	10	7	6	4	0.19	51.46	92.55	93.4

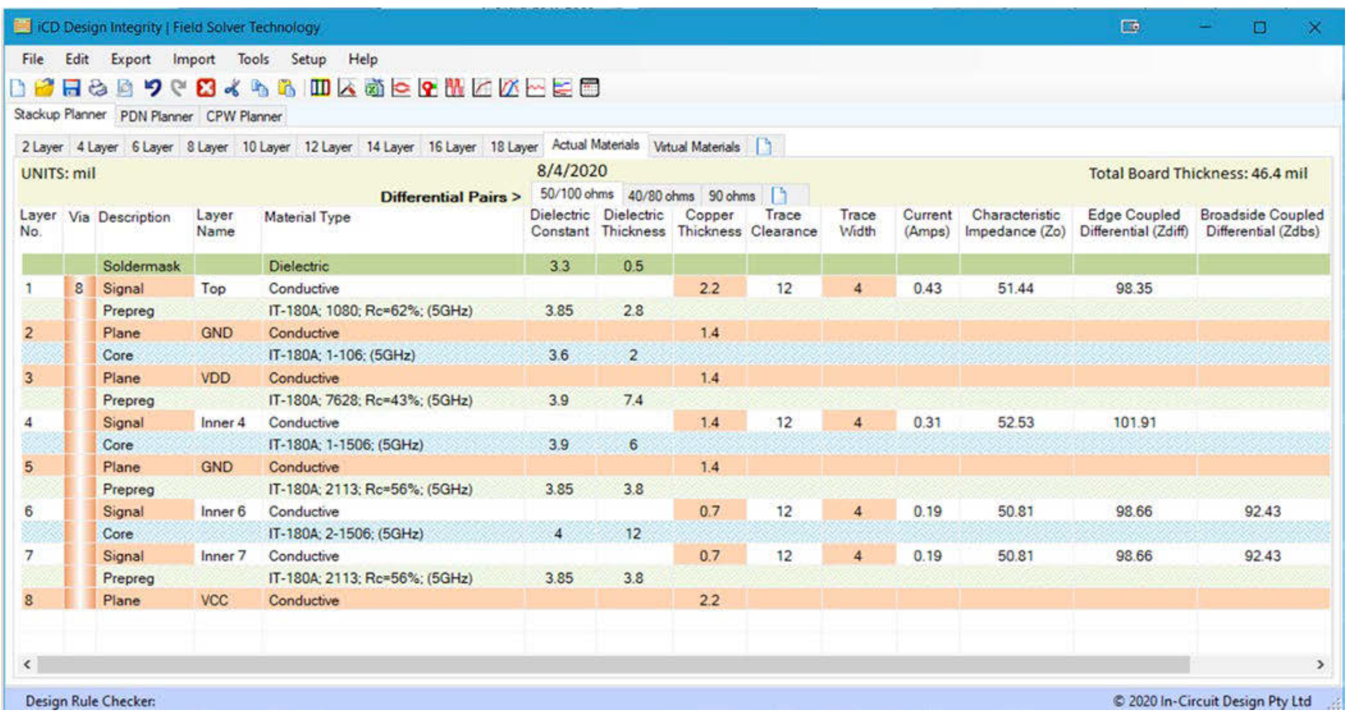
Table 1: The three different technologies using virtual materials.

50/100, while DDR3/4 is 40/80 single-ended/differential impedance. Controlling impedance simultaneously on each signal layer with a number of different technologies can become a challenge.

Unfortunately, your preferred PCB fabricator will not stock these values, so the next step is to convert the virtual materials to actual materials that are available (in the partial stackup of Figure 8). This will also give you the actual materials for the three different technologies (Table 2). This is the step that most, if not all, designers avoid, leaving it to the fab shop CAM engineer.

To do this, we first need to determine an operating frequency that the product needs to perform. Generally, we need to consider the bandwidth up to the fifth harmonic of the fundamental. If we have a clock running at 800 MHz, then 4-GHz material would be appropriate. I have chosen the ITEQ IT-180A, 5-GHz material, which is readily available from Asian fabricators and is suitable for low-cost, high-speed applications. The iCD Materials Planner can be used to narrow down the selection from the fabricator's stock.

The configuration of the PCB stackup depends on many factors. But whatever the



Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
		Soldermask		Dielectric	3.3	0.5							
1	8	Signal	Top	Conductive			2.2	12	4	0.43	51.44	98.35	
		Prepreg		IT-180A; 1080; Rc=62%; (5GHz)	3.85	2.8							
2		Plane	GND	Conductive			1.4						
		Core		IT-180A; 1-106; (5GHz)	3.6	2							
3		Plane	VDD	Conductive			1.4						
		Prepreg		IT-180A; 7628; Rc=43%; (5GHz)	3.9	7.4							
4		Signal	Inner 4	Conductive			1.4	12	4	0.31	52.53	101.91	
		Core		IT-180A; 1-1506; (5GHz)	3.9	6							
5		Plane	GND	Conductive			1.4						
		Prepreg		IT-180A; 2113; Rc=56%; (5GHz)	3.85	3.8							
6		Signal	Inner 6	Conductive			0.7	12	4	0.19	50.81	98.66	92.43
		Core		IT-180A; 2-1506; (5GHz)	4	12							
7		Signal	Inner 7	Conductive			0.7	12	4	0.19	50.81	98.66	92.43
		Prepreg		IT-180A; 2113; Rc=56%; (5GHz)	3.85	3.8							
8		Plane	VCC	Conductive			2.2						

Figure 8: The actual materials using ITEQ, IT-180A (iCD Stackup Planner).

Target Impedance	Tol +/-%	Layer No.	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
50/100 ohms	10	1	12	4	0.43	51.44	98.35	
50/100 ohms	10	4	12	4	0.31	52.53	101.91	
50/100 ohms	10	6	12	4	0.19	50.81	98.66	92.43
50/100 ohms	10	7	12	4	0.19	50.81	98.66	92.43
40/80 ohms	10	1	12	6.5	0.62	40.46	77.52	
40/80 ohms	10	4	8	6.5	0.44	42.3	79.29	
40/80 ohms	10	6	15	6.5	0.27	39.82	78.46	71.11
40/80 ohms	10	7	15	6.5	0.27	39.82	78.46	71.11
90 ohms	10	1	6	4	0.43	51.44	90.6	
90 ohms	10	4	6	4	0.31	52.29	91.58	
90 ohms	10	6	6	4	0.19	50.68	91.73	92.32
90 ohms	10	7	6	4	0.19	50.68	91.73	92.32

Table 2: The actual materials for the three different technologies.

requirements, one should ensure that the following rules are followed to avoid a possible debacle:

- All signal layers should be adjacent to and closely coupled to an uninterrupted reference plane, creating a clear return path and eliminating broadside crosstalk.
- There is good planar capacitance to reduce AC impedance at high frequencies.
- High-speed signals should be routed between the planes to reduce radiation.
- The substrate should be symmetrical with an even number of layers, which prevents the PCB from warping during fabrication and reflow.
- The stackup should accommodate a number of different technologies.
- Cost—the most important design parameter—should also be addressed.

Take charge of the impedance selection process and learn to control the variables rather than just handing the decisions over to the fab shop. This should be done very early in the design process to eliminate the need for change at a later stage, which could require the rerouting of critical nets and result in delays in the development schedule.

Key Points

- Impedance is the key factor that controls the stability of a design.
- The substrate is the most important component of the assembly and needs to be planned correctly to maintain consistent impedance across layers, avoid unintentional signal coupling, and reduce electromagnetic emissions.
- PCB fabricators know their production process extremely well, and their manufacturing expertise is invaluable to produce a high-performance substrate.
- Trace width increases as impedance decreases, so start with the highest impedance technology first.
- 1.4 mil is a good first choice for copper thickness unless you have a high layer count stackup.
- Differential signals that are closely coupled will operate mainly in the differential mode with some common-mode radiation from imbalances in the signals.
- If the two traces are separated enough to prevent coupling, then both act as single-ended signals. A 100-ohm differential pair becomes two individual 50-ohm single-ended signals.
- The combination of trace clearance and dielectric thickness provides the point of coupling. Use the point of coupling to define the crosstalk trace clearance constraints.
- All signal layers should be adjacent to and closely coupled to an uninterrupted reference plane. This provides the shortest loop area and the lowest inductance for the return current path.
- Glass weave skew and pile unevenness can be prevented by using two plies of 1067 glass prepreg combined.

- Low loss materials tend to have lower dielectric constants (~3).
- A high dielectric constant creates the most planar capacitance, which is used to lower the impedance of the power distribution network.
- First, plan the stackup using virtual materials, and then convert the virtual materials to actual materials that are stocked by your preferred fab shop.
- Consider the bandwidth up to the fifth harmonic of the fundamental. **DESIGN007**

Further Reading

- B. Olney, "Beyond Design: The Key to Product Reliability," *Design007 Magazine,* June 2019.
- B. Olney, "Beyond Design: The 10 Fundamental Rules of High-Speed PCB Design, Part 2," *Design007 Magazine,* October 2018.
- B. Olney, "Beyond Design: Common Symptoms of Common-Mode Radiation," *Design007 Magazine,* May 2018.
- B. Olney, "Beyond Design: Controlled Impedance Design," *The PCB Design Magazine,* May 2015.
- B. Olney, "Beyond Design: Signal Integrity, Part 3," *The PCB Design Magazine,* December 2014.
- B. Olney, "Beyond Design: Signal Integrity, Part 1," *The PCB Design Magazine,* October 2014.
- B. Olney, "Beyond Design: Stackup Planning, Part 3," *The PCB Design Magazine,* August 2014.
- B. Olney, "Beyond Design: Practical Signal Integrity," *The PCB Design Magazine,* August 2013.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at icd.com.au. To read past columns or contact Olney, click here.

Pattern Blazer World's Brightest LED Pattern Projector in 3D Vision Applications

Innovations in Optics, Inc. introduces the Pattern Blazer, a high-power, LED fixed-pattern projector for structured lighting and stereovision in 3D machine vision. Pattern Blazer applications include determination of object shape and orientation, contour mapping of parts, surface defect detection, depth measurements, guidelines, edge detection, and alignment. A near infrared version is suited for video identification in long-range CCTV security and surveillance.

The Pattern Blazer projects patterns with an intensity that is at least 5X to 10X greater at the same distance than other "high power" LED Pattern projectors for similar pattern size and wavelength. It can be operated in either continuous, PWM or pulsed current modes. Extremely bright patterns at long working distances enables the use of 3D imaging in vast, well-lit areas including outdoor locations.

The Pattern Blazer features four standard LED spectral options, blue (480 nm), red (660 nm) near-infrared (860 nm), and broadband white (4800K). It uses standard C-mount machine vision lenses designed for 1" image sensors. The Pattern Blazer incorporates pinhole-free precision reticles patterned by photolithography to produce thinner lines, sharper edges, and more homogeneous illumination than lasers and without diffraction or speckle effects. Projected patterns for the Pattern Blazer include lines, grids, edges, and random dot point clouds. Other wavelength LEDs and custom patterns can be provided upon request.

(Source: Innovations in Optics Inc.)

Stop Relating Trace Temperature to Current Density

Feature by Douglas Brooks, Ph.D.

Many design engineers and even many software suppliers make the significant mistake of equating changes in trace or via temperature with current density. This is incorrect at best and dangerous at worst. There is little if any correlation between temperature and current density. Current and trace dimensions (among other things) are the relevant variables, but current density is not. I hope by the end of this article you will see why. Here are four illustrations that will help you understand this.

1. Current Density Is Not an Independent Measure

We can understand that the change in trace (and via) temperatures are a function of other variables. Thus, we can formulate the following as two possible relationships (all other things equal). Let:

C = current
J = current density
w = trace width
th = trace thickness
ΔT = change in trace temperature

Then, we can suggest the following:

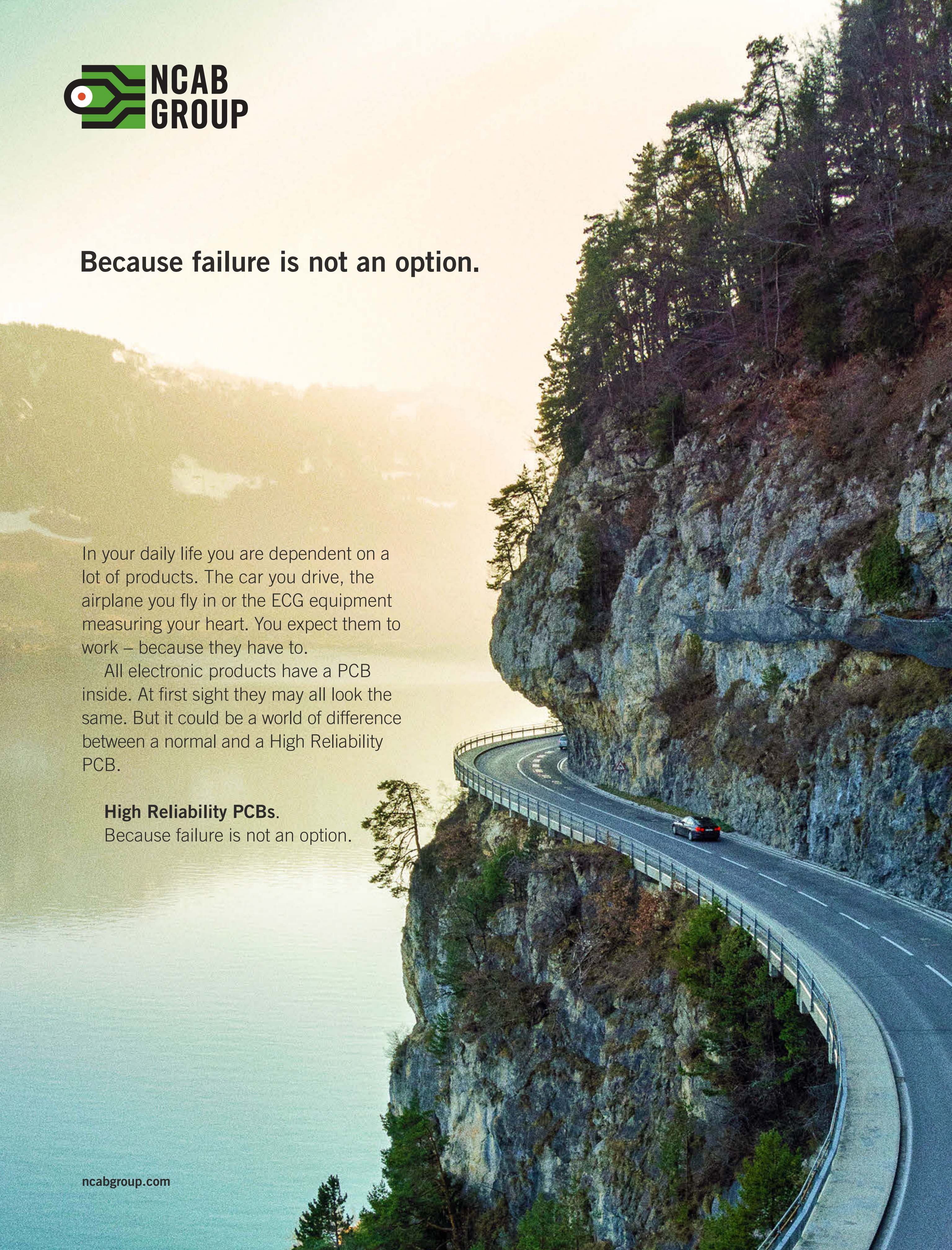
Equation 1: $\Delta T = fn(C, w, th)$
Equation 2: $\Delta T = fn(J, w, th)$

Now, the question is, "Are both of these relationships true, or, if not, is either one true?" We know from the extensive experimental evaluations reported in IPC-2152 [1] that Equation 1 is true, so is Equation 2 also true? From Equations 1 and 2, it follows that:

Equation 1a: $C = fn(\Delta T, w, th)$
Equation 2a: $J = fn(\Delta T, w, th)$

Now, a little thought reveals that Equation 2a does not follow. C is an independent variable, but J is not. J is a derived variable equal to C divided by the cross-sectional area w times th. What Equation 2a really describes is Equation 2b: $C/(w*th) = fn(\Delta T, w, th)$

We cannot independently change w and th on each side of the relationship. We can't have one cross-sectional area on one side of the equation and a different one on the other side. If we move w and th to the right side of the relationship, we find that Equation 2b reduces to Equation 1a. What it means: We cannot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All electronic products have a PCB inside. At first sight they may all look the same. But it could be a world of difference between a normal and a High Reliability PCB.
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determine the desired width and thickness of a trace (or via) by assigning a value to J, which itself already depends on an implied value for w and th. Equation 2 is not the correct relationship.

2. IPC-2152 Curves Can Yield an Answer

It is intuitive that the form factor of the trace impacts its temperature. That is, wider, thinner traces are cooler than narrower, thicker traces with the same cross-sectional area. The reason is that wider, thinner traces have more surface area for conducting the heat away and, therefore, cool more efficiently. Two traces with the same cross-sectional area, carrying the same current (and therefore having the same current density), will have different temperatures depending on their form factor. This can be seen in the IPC data.

IPC-2152 contains a very large set of graphs of the relationship between trace current, trace size, and trace temperature. The gray lines in Figure 1 are derived from the data contained in Figures A-48, A-49, and A-50 (pages 57 and 57) in that publication [1]. The data are simply redrawn on a different set of axes. The green lines are lines of constant current density (J). It is clear, even from the IPC data, that even though the current density is constant, the trace temperature can vary widely because of the form factor.

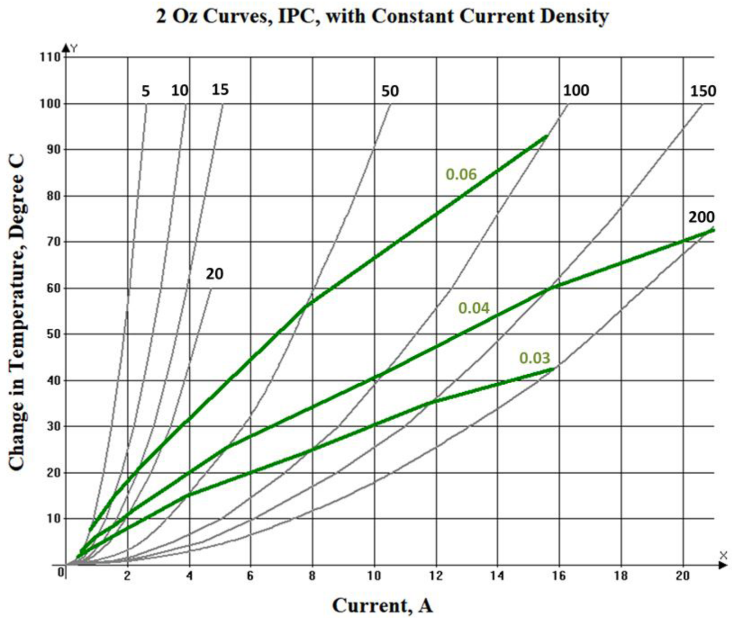

Figure 1: Relationship between current and temperature change for 2-oz. traces of various widths. Constant current density lines are in green. (Black numbers are trace width in mils. Green numbers are current density in amps/mil^2.) (Source: IPC-2152 [1] and Figure 6.10, page 61 [2])

3. Modeling Form Factor

We can use TRM [3] to model a trace with changing form factor and constant current density. We modeled a trace with three segments, as shown in Figure 2. The model parameters are as shown in Table 1.

Although a trace with these dimensions may be difficult (but not impossible) to actually build, the TRM model can easily simulate it. Figure 2 shows the model results for both temperature and for current density. It is clear that the simulation model shows

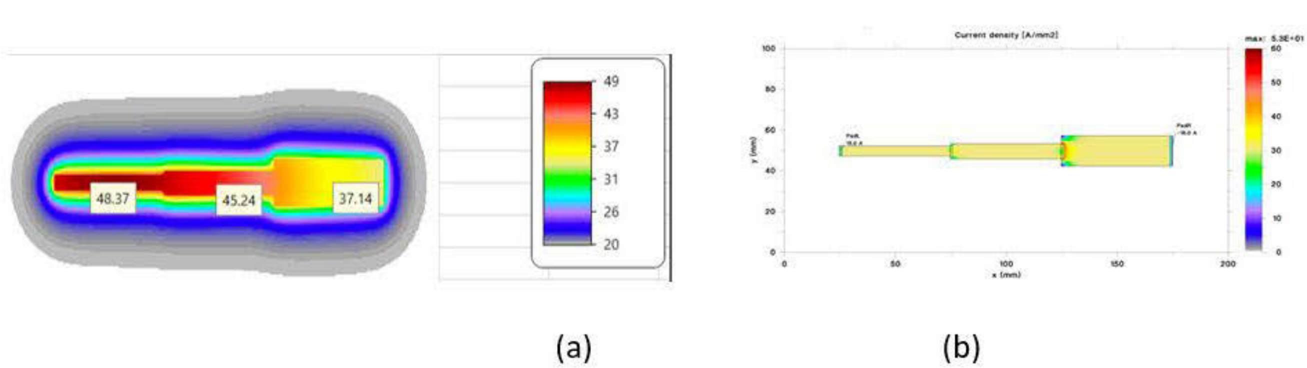

Figure 2: Temperature (a) and current density (b) profiles of our thermal model. The temperatures shown are temperatures at a specific point on the segment and will vary from point to point.

Board size	100 x 200 mm
Trace length	150 mm (overall)
Trace width (seg 1)	5 mm
Trace thickness (seg 1)	0.099 mm
Trace width (seg 2)	7.5 mm
Trace thickness (seg 2)	0.066 mm
Trace width (seg 3)	15 mm
Trace thickness (seg 3)	0.033 mm
Trace cross-sectional area (each segment)	0.495 mm^2
Trace current (each segment)	15 amps
Trace current density (each segment)	30.3 A/mm^2

Table 1: Simulation model parameters.

Board size	80 x 12 mm [6]
Board thickness	1.6 mm
Copper thickness	0.04 mm
Trace length	32 mm, top and bottom 60 mm overall
Trace width	Varies: 0.6–5.0 mm
Via diameter	0.26 mm
Via wall thickness	0.04 mm
Via cross-sectional area	0.02675 mm^2

Table 2: Via simulation parameters.

a constant current density everywhere, but significantly different temperatures in the three segments.

4. Current Density and Vias

One of my biggest concerns is when designers base decisions regarding the number of, or the size of, vias on the current density flowing through them. Dr. Adam and I have already shown [4] that the temperature of a via is not related to the magnitude of the current flowing through it. It depends on the temperature of the parent trace. That is because the trace acts as a huge heat sink for the via and conducts the heat away from the via. This is exactly analogous to how the heat sink above a computer microprocessor conducts the heat away from and protects that component.

Dr. Adam and I used simulation to illustrate that point a few years ago. Knowing that that would be hard for many people to accept, we (with help from Prototron Circuits [5]) later experimentally verified those results. I recently ran another set of via simulations regarding current density. The parameters of the simulations are shown in Table 2.

The trace width was varied from 0.6 mm to 5.0 mm, but the via dimensions remained constant for all simulations. The applied current was adjusted so that the via temperature also remained constant (to the degree practical). The trace temperature for each simulation was recorded at a point mid-way between the beginning of the trace and the center of the via. Figure 3 illustrates the thermal pattern for the top layer of the simulation for the 2.0 mm trace carrying 5.25 A.

The results of the simulations are shown in Table 3 and Figure 4. The first thing to note is that when the trace width is small, such that the via cross-sectional area is about the same as or larger than that of the trace, the via temperature is less than the trace temperature. This is because the via resembles an internal trace, completely surrounded by board dielectric, and so it cools more efficiently than the parent trace [7]. As currents (and therefore temperatures) increase, vias do get warmer than the parent trace, but only slightly so.

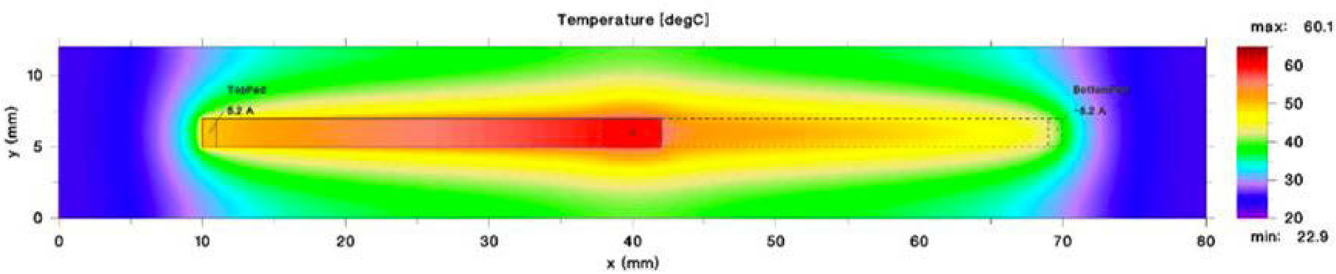

Figure 3: Thermal profile of the 2.0-mm trace carrying 5.25 A. Via is at the center of the board.

Trace W mm	Current A	T-Trace °C	T-Via °C	J-Trace A/mm²	J-Via A/mm²
0.6	2.74	61.2	60.4	114.2	99.1
0.7	2.95	59.5	59.4	105.4	106.7
1.0	3.57	58.6	60.5	89.3	129.1
2.0	5.25	56.5	60.5	65.6	189.9
3.0	6.5	54.8	59.8	54.2	235.1
4.0	7.5	53.7	60.0	46.9	271.2
5.0	8.4	52.7	59.6	42.0	303.8

Table 3: Summary of the constant-temperature via simulation.

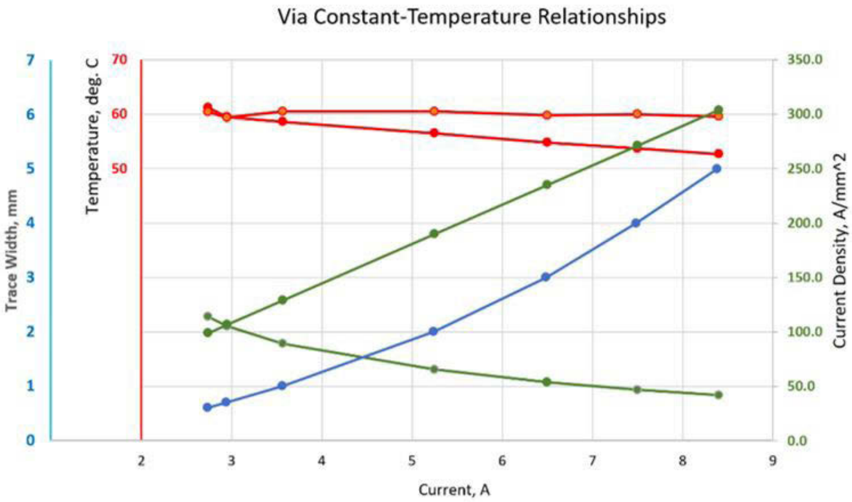

Figure 4: Constant-temperature via simulation.

Secondly, note that even though the via dimensions remain constant, the temperature is remaining (nearly) constant over the entire current range from 2.7 to 8.4 amps. That is because the parent trace is acting as a heat sink. Without the effects of the parent trace, the via would likely melt at 8.4 amps in approximately one second [8].

Finally, and most importantly, note that the current density (green curves) is varying widely, both along the trace and through the via, as we change simulations. Yet the via temperature is remaining constant, and the trace temperature is only varying over a narrow range. This shows that current density is not related to via temperature. This shows that current density is not related to via temperature. (Note: Repeating this sentence is not a mistake.)

Conclusion

If you are designing boards, stop making trace and via decisions based on current density. **DESIGN007**

Notes

1. IPC-2152, "Standard for Determining Current-Carrying Capacity in Printed Board Design," August 2009, IPC., ipc.org.

2. Brooks, Douglas G., Ph.D., and Dr. Johannes Adam, PCB Trace and Via Current and Temperatures: The Complete Analysis, 2nd Edition, 2017.

3. TRM (Thermal Risk Management) was created by Dr. Johannes Adam, president of Adam Research (adam-research.com). TRM was originally conceived and designed to analyze temperatures across a circuit board, taking into consideration the complete trace layout with optional Joule heating as well as various components and their own contributions to heat generation.

4. See Note 2, Chapter 7.

5. Prototron Circuits of Tucson, Arizona, contributed several test boards for our research efforts.

6. Via simulations place about a 100x greater demand on the computer CPU and memory than do trace simulations. This is because via simulations require much greater thermal resolution (due to the small width (thickness) of the via wall). Therefore, from a practical standpoint, via simulations usually are done with smaller dimensions than are trace simulations.

7. Recall one of the surprising outcomes of the IPC-2152 investigation was that internal traces are cooler than external ones, all other things equal.

8. We discuss fusing times and conditions in Note 2, Chapters 10 and 11.

Douglas Brooks, Ph.D., is the founder of UltraCAD Design and co-author of *PCB Trace and Via Currents and Temperatures: The Complete Analysis.*


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Combatting Thermal Challenges With TRM Software

Feature Interview by the I-Connect007 Editorial Team

Johannes Adam is the creator of a simulation tool called Thermal Risk Management (TRM), used to help PCB designers and design engineers predict hot spots on the board before and during layout. He and Douglas Brooks, founder of UltraCAD Design, have used the tool to produce several technical articles and a book on the subject. In this interview, they tackle the biggest misconceptions they see from designers and engineers who deal with thermal management issues.

Andy Shaughnessy: Doug, tell us about your work with thermal and how you got involved with Johannes.

Douglas Brooks: I became involved in thermal issues on PCB design when I wrote an article for a magazine in '96 and compared some results from the then-IPC traces, which went back to the MBS traces. I saw data in another article that was different by about 40%. Then, IPC-2152 was published, and that was about 25% lower temperature than previous NBS data that went back to the 1950s, primarily because they were using more current boards and also because they were doing a more careful study. But it still raises a question of how come there was such a big difference between the article data and the IPC data. I began to theorize that the difference had to do with the difference in measurement technique. IPC used a technique that, in effect, measured the average temperature of a trace, and the article data measured the peak temperature in the center of the trace.

I was looking around for a way to verify that, and I saw a thermal image of a trace that I traced back to Johannes in about 2016. I contacted Johannes, and we started a conversation. He sent me a copy of his software. He was very patient while I started coming down the learning curve of that software, and we entered into a collaboration that went from trying to look at the differences in data to things like, "How hot is this via? Can you measure the resistivity of a trace? What happens when you bring up a parallel trace? Can you get into the fusing questions?" This ballooned over the years into what became the book that we published back in 2018. Then, there were some other ancillary articles that reflected various chapters in that book.

Johannes Adam

Johannes has been a great help to me. I'm now retired, which allows me time to do some of these things. Artech House is going to publish an updated version of our book in the first quarter of 2023.

Shaughnessy: Johannes, give us a quick background. You are a rocket scientist, correct? You're one of the few that I know.

Johannes Adam: I'm not a rocket scientist, but I am an astrophysicist (laughs). And by the way, conduction-cooled boards in vacuum can also be simulated. I've been involved in programming since my undergraduate studies or even in high school, starting with punch cards. Doug actually contacted me in November of 2014 when I was giving an electronics cooling seminar in Hannover. At that time, I had been working in the field of trace heating and temperature prediction more or less since 2001. I knew Doug's work, but I was too shy to contact him. The interest in trace heating came from questions from users of FloTHERM at Bosch, who I was supporting as a support engineer at that time. They asked about the temperature of the trace, and I had to say, "I can calculate the ventilation of your device, but an amp is not an input value." I started looking at these IPC design rules and literature.

It was not until much later that I had the idea of writing my own software that focuses on the PCB traces, layer structure, pads, and drilled holes to calculate the temperature of the traces and components if the amps or the watts are given. This began in 2009, when I started my developments. Now, we have a very good third-generation TRM software tool, and the users are happy because it is easy to use, and neutral design data can be read and parameterized, but you are still free to add additional technological ideas and play with them. We have already made a small step toward electrodynamics in which it is possible to calculate the self-inductance and mutual inductance of nets.

Shaughnessy: I understand your tool now has an Altium interface.

Adam: We have a wizard for Altium users that we created ourselves. Users can export and import the board with just two clicks—one for export and one for import. You can even define amps or watts already in the schematic, but that's optional. There, you specify a certain current to a net, and this can be taken directly from Altium, or define the watts for the components if you want to store it there. But you can also supply the current and the watts after import to our tool, either from keyboard or with ASCII files prepared by other people. Then, you can calculate the voltage drop or current density distribution in a matter of seconds. Wizards for other vendors can be done if the interest is there.

Shaughnessy: That's one of the things that was always said about the existing thermal management tools was that you kind of had to have a Ph.D. to operate them.

Adam: Not at all, but one should have a certain understanding of thermal issues. You should understand that thermal conductivity or a datasheet does not tell you everything. Temperature is always an interaction between general physics and local design. Where is the copper? Where is the FR-4? How wide and where are the gaps? What is the power? What is the number and distribution of heat sources? It happens that under given conditions no reasonable temperature can be achieved, although it would be possible according to the datasheet. However, the datasheet does not know these special conditions. The software is also a virtual experimenting table. By the way, I am also a learner, and I like to work with committed EEs from whom I can learn.

Brooks: For a board designer using board design software, there's a learning curve that he has to come down on in any particular brand of software. Johannes' software is extremely powerful, but there's a learning curve coming down that, too. The work that I've done with that for PCB trace analysis probably touches on 10–15% of the capability of what the software can do. If you are a system engineer and want to look beyond traces at what happens on the rest of the board from the contribution of the components and stuff like that, that is a system engineering function, and this software is very well suited for doing that.

Dan Feinberg: I'm really interested in the fact that Johannes is saying how quickly the software can respond to a thermal change. Can you give me an idea of how quickly that would be?

Brooks: The software isn't real-time. You set up the parameters, push the button, and it will give you a measure of what's going on at the moment you've pushed the button. You enter the data, but it's not a monitoring thing. If I'm doing some complex trace work on a moderately powered desktop computer, it will reach a solution in one to three minutes at most. If I'm doing a via analysis, which is maybe two orders of magnitude more complex because of the size of the via walls and much larger matrices you're working with, a good, solid via analysis is going to be anywhere from 20 minutes to two hours.

Adam: The software can even be faster than real-time; for example, if you wait 10 minutes in the lab for the steady-state, the calculation is done in two minutes. It is the size of the board and the number of layers that determine the CPU time and the effectiveness of heat removal. We calculate a network of up to millions of data points, which takes time. Coupling the electrical properties to temperature or transient processes takes longer.

However, one must not look at the computing time, but at speeding up the time-to-market. For a laboratory test, the components and circuit must be ready for operation, but a simulation can start much earlier.

Happy Holden: This uses finite element analysis.

Adam: It's not precisely finite element, but it's an equivalent.

Holden: When I was at Mentor, I worked with Simcenter Flotherm and a computational fluid dynamic tool, which was three-dimensional.

Adam: Yes. I was a field engineer for Simcenter Flotherm in my previous job.

Holden: But when they gave me the computational fluid dynamics, I went back and said, "Are you trying to fool me? Is this a video? Because this is a 2006 Dell computer desktop, and it's not capable of doing real-time three-dimensional 3D modeling finite element analysis with a single Dell." And they said, "No. That's not fake or a simulation. That's real-time, but it's all Russian software, and they do finite element convergence in a totally different way than we do in the West." I got to play around a lot with three-dimensional computational fluid dynamics.

Shaughnessy: What are some of the biggest misconceptions that you see out there for the designers and EEs who are working with thermal? What are some of the common mistakes?

Brooks: I love that question. The temperature of a via is determined by the amount of current that goes through it. That's absolutely false. There's no relationship between current and temperature in a via.

Adam: Or current density in general.

Brooks: There is a paragraph in IPC-2152 that says the way you size a via is to give it the same cross-sectional area as the equivalent trace. That's all it says. That's about the only thing in IPC-2152 that addresses vias. When I started working with Johannes with the software, the first thing I did was apply the software to the IPC-2152 graphs to see if we could simulate them and get the same answer and, therefore, determine whether the software had some validity from that standpoint. We determined that it did, and we could fit the curves extremely well.

Then, I asked Johannes, "Can we simulate a via?" I don't want to speak for Johannes, but I don't think Johannes had ever thought about looking at something as small as a via, and it took us a few trials with the software to get it modeled. But we did get it modeled, and it was a result of that modeling that showed us that the temperature of the via was not at all related to the current going through it.

The reason is pretty obvious when you think about it. The trace is very much larger than the via. The trace is a heat sink. Whatever current you put into the via, and no matter how hot that via tries to get, the heat just pours right out of that via into the trace—top and bottom—and the via cannot heat up because of the heat sink.

Holden: Does the via ever get as hot as the reflow temperature?

Brooks: The via only gets a little bit hotter than the trace. If you have a trace and a via that are the same cross-sectional area, the via is cooler than the trace because the via is an internal trace, and the trace is an external trace. IPC-2152 showed us that internal traces are cooler than external traces because they are fully in contact with the dielectric, and the traces on top and bottom are only partially in contact with the dielectric; they're partially in contact with the air. The dielectric cools better than the air does. The via might be 10 degrees hotter than the trace, but that's about it. I've run some simulations out to unreasonable situations—250-mil or 500-mil traces and a 10-mil diameter via—and you still don't get more than 10–15 degrees hotter than the trace.

Shaughnessy: Where is most of the interest coming from?

Adam: The most important branches of industry in Germany are the automotive industry and power electronics. This is obvious, but my users come from all areas of electronics development. These areas include consumer electronics, network technology, LEDs, or even technologists who try to find a good solution without having Gerber files or any designs. They create patches with copper and patches without copper, invent a stackup, move holes or vias to where they want them, and apply some current or power. Is heat spreading capable of dissipating the heat from the local heat source?

Brooks: That touches on a parallel topic. When I put on seminars, and I show the simulations and stuff and show what happens when you change the trace width or trace thickness and how it impacts temperature, the question, "What should the temperature be?" always comes up. Remember that it's the board designer's job to design a set of specifications, but what the temperature should be is answered by a systems-level engineer, not a board design engineer. That may be the same person, but it's a system engineering function to determine what the temperature should be and what the allowable temperature is. It's not the board designer's function.

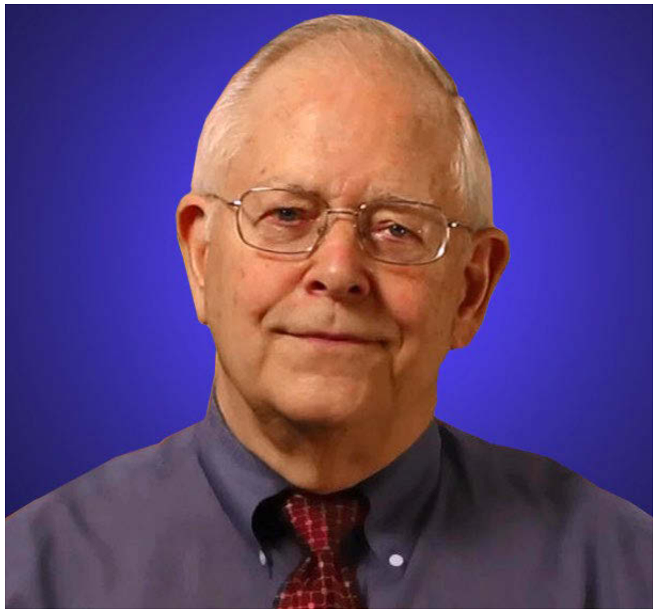
Shaughnessy: Is there any advice you'd like to give the designers or EEs just now getting into thermal?

Brooks: Find a book. Remember that current density is not related to temperature. All the automated tools out there talk in terms of current density, but it's not current density, and I build the case in my article from four different directions why it isn't. But the short answer is current density is a derived variable. It's current divided by area, but the area is one of the variables in the heating equation in the first place. You're taking a true variable and current and creating a derived variable and current density; that uses one of the other independent variables in the first place. You can't treat it as a constant and also treat it as a variable at the same time, and I show illustrations where there's absolutely no relationship between current density and temperature.

Adam: My advice would be to not trust datasheets, especially not the prediction of the component temperature (laughs). You'll find a value called thermal resistance junction to ambient, and for the temperature rise, multiply this numerical value on the calculator by the watts of the component. Hopefully, there's a footnote in the datasheet that reads, "We used a JEDEC-51 like a test board with four layers, and the component was mounted on exactly this test board." What the datasheet then tells you is the thermal resistance of the test board and not so much the thermal resistance of the component—certainly not the thermal resistance of your board. You have to be very careful.

Brooks: If you think very simply to the trace level, the trace heats by I^2R. It cools primarily by conductivity into the board material, and there's a parameter in the board material called the thermal conductivity coefficient, which is the most important factor in the cooling equation. The thermal conductivity coefficient is the most important factor, and the thermal conductivity coefficient is measured in two different directions. It's different in those directions. One is perpendicular to the trace, which is the through-plane measure, and the other is parallel to the trace, which is the in-plane measure.

Coming back to the datasheet, the situation is a bit better than it was, but it's still not good. The dielectric datasheets typically don't have the thermal conductivity coefficient. If it does, it has the single value of the thermal conductivity coefficient, and it doesn't tell you which one it is. One of my calls to the industry is for all dielectric manufacturers to fully characterize their offerings by the thermal conductivity coefficient in both directions.



Douglas Brooks

Adam: It's even worse with specific heat capacity and mass density. If you want to run heating curves or on/off states, you have to know the heat capacity of this FR-4 mix of glass and resin, and it is a very sad situation that we don't know the values properly enough.

Shaughnessy: It seems like the EDA and the PCB design communities are getting a little more interested in thermal.

Brooks: There's more acceptance and recognition of the need, but I don't see much effort in learning what it's all about. You see old-fashioned rules of thumbs that are tossed up in the EDA datasheets or application notes and stuff that reflect they don't fully understand it.

It turns out if you go back to the original IPC data, which was the NBS report published back in 1956, Mike Jouppi did some superb work back in the late 1990s and the early 2000s in tracing down the origins of that stuff. He told me one day that one of the original two authors has passed away, but the other was still living. Mike went to visit him, and he still had the original data in his garage in some boxes. He was thrilled that someone finally took enough interest in it to come out and talk to him about it. Mike got to look at some of the original data.

There were scrap boards that were lying around the office, and that was all the original investigators had. They tested those boards. When they published it, they said, “This is preliminary and uncontrolled. What we really need is more money to do this more correctly.” But the money wasn’t coming. The first curves were published with the heading that said “preliminary,” and the internal curve data was not even experimentally derived. It was just, “The internal traces have to be hotter than the external ones, so we’ll just derate them by a factor of two.” Those are the curves we used for 50 years in the industry.

Holden: They’re like Moses’ stone tablets. It’s fighting words if you say that they’re not correct.

Brooks: We used them for 50 years, and we got away with it because they were so conservative. Now, IPC-2152 is better data, but it is still conservative. I show in one chapter in our book that almost anything you do from a PCB design standpoint lowers the temperature of the trace. If you lengthen it and bring another trace nearby, you could put a plane underneath it—almost anything you do on a board lowers the temperature of the trace because it improves the thermal conductivity. If you are still basing designs on IPC-2152 data, you’re going to be fine. It’s just inefficient. You’re making the traces too big.

Holden: At HP, we designed processors with much higher performance than Intel. But the problem was keeping these HP processors cool enough because they’re using NMOS 3 with a lot of current. They had the heat sinks, but they couldn’t get the massively parallel CPUs close enough. They were forced to go to optical busing between CPUs because of the noise on the high-speed buses separated by the distance it took just to handle the heat. They didn’t want to go with liquid cooling on their systems. They wanted to stay with air cooling.

Brooks: In 1968, I worked with Texas Instruments, and we built the very early stage of ESL integrated circuits. They designed the ILLIAC IV supercomputer for the government. We had as much difficulty designing leak-proof plumbing through the substrate as we did designing the chips to get them all together. Those were water-cooled through channels in the substrates.

Shaughnessy: Well, thermal continues to be a hot topic; I had to say that. This has been great. Thank you for your time, gentlemen.

Adam: Thanks, Andy.

Brooks: Thank you. Always a pleasure. **DESIGN007**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5 Questions About Improving Thermal Management

The Bare (Board) Truth

Feature Column by Mark Thompson, CID+, MONSOON SOLUTIONS

In this column, I will focus on answering five questions about thermal management at the design and PCB levels. These questions were sent to me from one of the owners at Monsoon Solutions, where I now work. Jeff Reinhold, EE and designer, asked:

1. When I get a datasheet that calls out some area of copper for heat dissipation, how do I translate that requirement to fit my board that may or may not have the specified area available?
2. How much heat does a via dissipate, and how does size and fill change that?
3. Does moving heat to internal layers help at all or even work?
4. How do I identify potential thermal issues?
5. How do I translate a heat dissipation requirement, in whatever form it is given, into parameters I can use to design a solution?

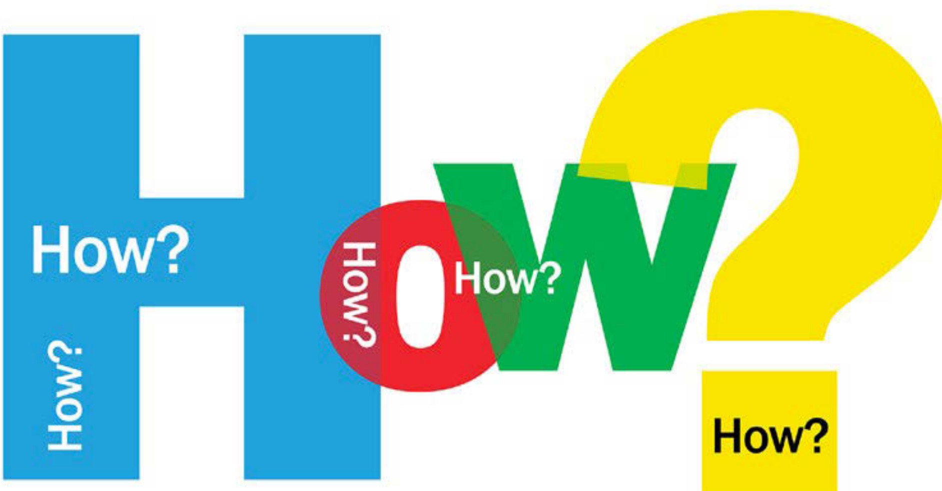
Some of the questions I can answer from my "previous life" in PCB fabrication, but for others, I asked my co-workers for their comments.

Question #1

Regarding the first question, Kevin Carrington, a design engineer at Monsoon, said:

Thermal management is all about deltas. Heat only moves along a gradient, so if heat isn't actively being removed, then it's simply spread, which means your delta-T is diminished. Spreading over a long enough time achieves steady-state, so understanding a use scenario is often important. Putting more copper in the circuit board would have zero impact on thermal management if the board is at a steady-state condition.

The physical size of parts is very important when considering heat dissipation. A great example is the power SO-8 package that many discrete FETs come in nowadays and have largely replaced the DPAK components. Parts in those packages are often rated very similarly for operating parameters, but the DPAK is far superior when it comes to getting heat out because of the size of the thermal tab.



Accounting for the resistance change of metal with temperature can have a big impact on the system. If you ignore copper—like the circuit board, big common-mode chokes, or inductors—you might be cutting a lot of power dissipation and heat out of your analysis. Even if you include them but use room-temperature copper calculations, there can be big differences between analysis and reality.

Kevin Carrington

Thermal foam can be a very useful way to get heat to a metal case when a closed system is used (e.g., no fan). It's critical to have the foam in compression, otherwise, it won't achieve the desired low thermal resistance.

The ambient temperature is very important, and "ambient" is often not considered properly. Just because the air outside your product is 50°C doesn't mean inside is 50°C. For most electronics, the actual ambient temperature in which they're operating is the steady-state temperature inside the enclosure.

Question #2

For the most part, the most effective way of getting the heat out/dissipating heat from one side to the other is to use filled vias.

The best filled-via is a stitching via with solid copper plug matching the CTE of the copper being used on the PCB. The next best solution would be copper epoxy-filled vias. After that, a silver-filled via works okay. Lastly, epoxy fill can get some of the heat out. All work better than a standard stitching via that is unfilled. Air—particularly stagnant air—is a poor thermal conductor, so any material filling the via will lower that thermal pathway's resistance.

A smaller via filled with solid copper and many such stitching vias in an array would be the best if using vias to dissipate heat. Also, note that many fabricators have a size limitation on the size of filled vias; most say 0.008"–0.020."

Question #3

Generally, not increasing the copper area via a ground or power plane and even adding higher copper weight internally is not the answer. This approach may be quite beneficial for transient thermal excursions, but for most products, steady-state power dissipation is the concern.

Here, I would recommend a basic analysis through rough equations would be of a greater benefit than adding copper layers internally. But, as Kevin said, producing a prototype that can be tested in a thermal chamber would really tell you where you are.

If you are looking to dissipate heat and are considering adding copper, the best layers would be the outer layers with copper pour. This helps EMI but can dissipate heat through the surface.

Again, as Kevin said, "There is no magic copper layer that will be the best way to get the heat out."

Regarding heat in an enclosure, what is the best way to get the heat out when a board is in an enclosure? The first and oldest way is to simply have a fan in the enclosure.

Not being able to do that, Kevin mentioned a trick he learned when he was designing for DVRs that cannot have a fan. Another good method is to utilize compressed foam in the enclosure, but why compressed? Common sense would say uncompressed foam is porous.

The idea behind the foam is primarily spreading the heat to a chassis or other system component, which can hopefully get the heat out. The compression helps achieve lower thermal resistance, improving the effectiveness of the thermal pathway.

Question #4

A simple operating test in a thermal chamber using a prototype design can help make substantial leaps in understanding product risks, missed aspects of analysis, and correlating calculations.

Question #5

Question #5 is probably the best and toughest question to answer. The short version is to use the aforementioned techniques to identify, mitigate, evaluate, and optimize the thermal operating conditions of your product. Often, this means implementing a somewhat blind first attempt, using the best practices you can within your constraints, and then checking whether the performance is adequate. Drawing upon previous experience is a key part of this, whether that's the capability of a device, heat sink, or enclosure or understanding the environment in which it operates.

In general, thermal management is something of an iterative process, and explicit technical requirements aren't available nor knowable. For example, the most common requirement is related to the electronic components on the board not exceeding their rated junction temperatures. How to do that is a combination of the system implementation operating in the field conditions, which usually requires prototyping or simulation to baseline. Knowing that a part will dissipate 3W of power is simply not enough. Once you have an idea of where you're at, then you can assess opportunities for improvement.

Generally, these optimizations involve:

- Lower the power dissipation of the device (component selection, functional operating load)
- Improve the heat transfer conditions (thermal pathways through PCB, heat sinks, etc.)
- Constrain the operating environment/ use case (software-controlled limits, environmental ratings)

Whenever something is a risk, we must mitigate it, and because the nature of thermal management is heavily influenced by environmental conditions, prototyping is key. Even if it's just a small portion of the system, being able to characterize the limits will enable an understanding of whether simple thermal pathway improvements can succeed or whether drastic architecture changes are required. The latter is quite important to know as soon as possible. Lastly, use thermal vias and heat sinks where possible.

To remove the heat created by power dissipation of the components, and especially the power components, one solution is to improve the vertical heat transfer through the supporting material.

Typically, this is achieved by providing thermal through-contacts, or thermal vias, going through the substrate from the top side to the bottom side. It is typical to use thermal vias beneath the rear contact or mounting surfaces of the components and particularly the power components, and then plate the through-holes through the entire thickness of the material/substrate.

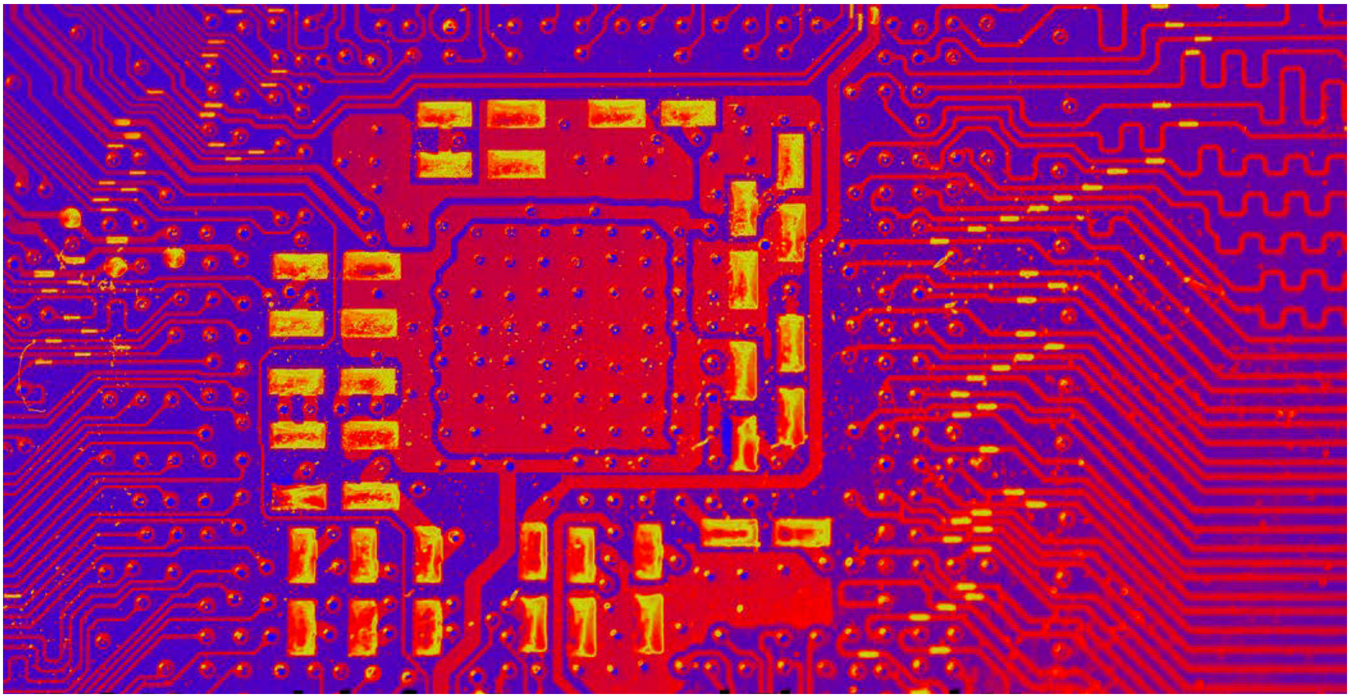
A second remedy for the heat dissipation problem relates to external heat removal. For this, the substrate may be mounted on a metallic cooling body or heat sink, such as a copper plate, which conveys the power dissipation heat to a cooling system. Such a cooling body may be separated from the supporting substrate by an electrical insulating layer, such as an insulating film or foil. After applying the components to the mounting surface of the substrate, the components are electrically connected with contact surfaces or specifically contact pads and the traces.

To achieve this, a solder paste is printed onto the contact surfaces and the top surface of the thermal vias and is then melted in a reflow soldering process to solder-connect the components.

Conclusion

I hope this column has helped to explain just a few ways to stay out of the hot seat. And, as always, I appreciate any feedback. I can be reached at markt@msoon.com. DESIGN007

Mark Thompson, CID+, is a senior PCB technologist at Monsoon Solutions Inc. To read past columns or contact Thompson, click here. Thompson is also the author of *The Printed Circuit Designer's Guide to... Producing the Perfect Data Package*. Visit I-007eBooks.com to download this book and other free, educational titles.



IMS Materials for Improved Thermal Management

Feature Interview by the I-Connect007 Editorial Team

Ventec International Group's Alun Morgan discusses some areas of development he has seen in the company's IMS thermal materials, as well as technological "hot spots" that can prove troublesome to PCB designers and engineers. He also offers advice to designers working on boards with challenging thermal properties.

Andy Shaughnessy: Alun, give us the history of IMS thermal materials.

Alun Morgan: Like many products, it came from a need. They have been around for some time, depending on how you categorize thermal materials, but the big starter was when LEDs suddenly became very popular. LEDs emit more efficiently than incandescent lighting, but they still generate more than two-thirds of their energy as waste heat. Suddenly, you found these fairly concentrated devices generating lots of heat. Mounted on the substrates, laminates are not particularly good at thermal conduction. People were sticking heat sinks on the back, trying to deal with the heat and managing it some way.

But that added cost. The first application for these devices was consumer or domestic lighting, such as a light bulb replacement, so the cost was a really big issue. Somebody had the bright idea of integrating a heat sink on the back of the substrate. It became part of the PCB and thus took a lot of costs away, avoided having to bolt a heat sink on the back, and enabled dealing with the thermal issue as a system approach. That was the start of it. You suddenly saw these substrates with aluminum stuck on the back. Instead of another layer of copper on the back, it was a layer of aluminum; copper was expensive and quite dense, so aluminum was the substrate of choice.

It moved fairly quickly back to DC-to-DC converters. People handling power bricks and then using inverters thought, "This is quite interesting. We can also use that." They were doing it in the past with heat sinks bolted onto the back of the PCB. It's a big advantage if you can just process something within standard PCB technology. That came around.

Automotive lighting was next in line to benefit from the technology. It started in the cabin with courtesy lights, then indicators. Eventually, it came to the headlights when LEDs became powerful enough to drive the main beams on vehicles. That was a big game-changer. You can integrate the whole thing as a single unit. That became a massive area of development for IMS materials because it provided another important advantage: reliability. You don't care so much if the lighting in your living room fails; you can simply replace it with another one. In the car, though, it's a big deal!

The reliability benefit also opened up a host of other application opportunities, particularly in the automotive sector. The market literally came to IMS materials. In the last decade or so, there has been a massive change from conventional vehicles with internal combustion engines to cars with electronic systems. We now have electronic drive systems. There are a lot of applications in the car where electronics are now used in pretty high-power applications: there are DC converters, onboard charges, inverters for traction, electronic power systems, high-power ECUs, and in-brake energy regeneration systems.

There are big advantages. One is cost because the thermal management system is integrated into the board. The second benefit is that the weight can be kept down. Aluminum is light compared to a lot of other solutions that were being used in the past. Overall, IMS evolved from a simple, domestic, low-cost application to something that is high-end. It has been used in many other areas as well.

Thermal management is required wherever there's high power. And what was possibly a niche product before may still be niche in some areas, but there are a lot of high-value niches, and they give a lot of value to the designer. They could design their thermal management around the circuit in the same package, which is separate from mechanical design. That is how we've come to where we are with systems today.

Shaughnessy: If you have a designer working on this board they know is going to have thermal problems, what sort of characteristics should they look for when they're comparing thermal materials?

Alun Morgan

Morgan: The first thing to work out is how much heat you have to move. When you look at the equations for how heat moves and thermodynamics, you find the most important thing is the differential of temperature from the thing that's hot to the thing that's cold. You have to find a solution to maximize that. We think a lot about emissivity. When you look at the back of the aluminum, how much heat does that emit? How much heat does that radiate out? We have a coating that we can provide on the back of the materials called ER1, which gets you pretty close to black-body radiation on the back of the radiator. The number ranges between zero and one. One is perfect, and zero is completely not emitting. With it, we can achieve from around 0.05 for straight aluminum to around 0.85.

The other thing you have to think about is the heat transmission through the substrates as well. There's a number for that. We call this thermal conductivity, which is measured in watts per meter Kelvin. Typical FR-4 laminate might be around 0.4–0.5. The first generation of the IMS materials was in the range of one to three watts per meter Kelvin. Today, we can achieve toward eight or 10 on an IMS substrate.

Again, thermal conductivity is important, but there's also thickness. The thinner the substrates, the more heat is transmitted. We ask OEMs what their design characteristics are. First, what's the temperature they have to deal with? And how big is the space? How big is the substrate they have to deal with? The area is always a massively important part of the calculation. Lastly, what voltage withstand is required in the design? This has a significant impact on what dielectric thickness will be used. Then, we can provide some solutions for emissivity. Given that, we can then design what's required and come up with a material that meets the application requirements. And that approach has proven very successful for a number of automotive companies in particular. They've shared with us their requirements, and based on that, we've come up with an appropriate material.

Shaughnessy: Automotive is one big science project area for PCB technologists.

Morgan: Automotive brings lots of things with it. People sometimes complain about the difficulty of dealing with some automotive suppliers, but we think they're great because they really challenge us. They challenge us on many levels. They challenge us on the technology and price point. They also challenge us in the supply chain. We have to bear in mind that when you find a solution for a particular application in a particular market, within the space of a few weeks or months, it has often required attention across the whole supply chain in the world. That's something that is very important for OEMs. They may do some development work in Germany and then move volume very quickly to China, for example.

Shaughnessy: Do these laminates change the way the designer has to do his design? Does he have to do anything differently?

Morgan: Not so much; although, they are basically single-sided circuits. You have to bear in mind that you only have one side for your circuitry, in general, but that doesn't usually matter. The backside of it is protected during manufacturing. There is a coating provided on that. During the PCB process, it can be dealt with. From the designer's point of view, it's a fairly simple layer design. They just have to design a single-sided board, and the back will be a piece of aluminum. They have to decide how thick the laminate should be because that's important, as well as how thick the dielectric should be and what properties the dielectric requires. Having done that, we can run with it. As our IMS products evolve, we see several requests from the engineering community for multiple layer IMS stackups. This requires multiple stacked layers of circuitry on top of the aluminum base plate that have internal connections through copper vias.

In terms of reliability, the other aspect to take into consideration is the thermal management of the expansion of all the different materials.

In terms of reliability, the other aspect to take into consideration is the thermal management of the expansion of all the different materials. A silicon package has an expansion coefficient of around 10 ppm/°C. For aluminum, it's about 25 ppm/°C, so more than double the amount of silicon. Copper is mid-teens, so maybe 17–18 ppm/°C. That could cause an issue for headlamps, for example, which are switched on and off quite frequently. Those are pretty high thermal cycling requirements. Again, the automotive companies have pretty robust testing for this. Failures can occur because of this constant expansion and contraction of the silicon device on the one hand, and then the aluminum can cause a failure on the other hand.

We've had to look at it very carefully. Instead of going with standard aluminum backing, which is typically around 24–25 ppm/°C, we've selected an alloy now that's around 19 ppm/°C. We've also been able to look at the substrate itself. With the actual thermal transmission material, the insulation layer, we've been able to reduce the modulus of that. Rather than having a very stiff material between the aluminum and the silicon package, we've put a slightly softer material in there so that it can take some of the strain and provide a compliant layer. By doing those two things, having this slightly lower modulus and lower CTE of aluminum, we've been able to pass automotive tests that just didn't run at all on conventional materials on the first run.

Shaughnessy: Does this add extra steps for the fabricator?

Morgan: Not at all. We just supply material that has a slightly different dielectric and a different aluminum on the back. With fabrication, there's nothing at all to do. They just run with it. But the basic properties of the material we supply have the benefit of being suitable for higher thermal transitions, or multiple transitions or thermal cycles.

Happy Holden: You mentioned expanding applications. People want to multilayer this material now. If so, aluminum is a pretty terrible poison for conventional printed circuit chemical processes. What step did they add to separate the aluminum from that? Do they use different chemical processes if they want to go to through-hole metallization?

Morgan: As I said, these are really single-sided devices. When you process the aluminum, it has a coating on the back to stop it from contaminating the baths. But when you get to the end of this, there's no reason at all why you can't have hybrid constructions here. People do that. They have part of the structure that will contain the IMS material, and the rest might be a multilayer. That's the way you have to get it in your mind.

Holden: I could make them multilayer. If you have bonding sheets, then a final step can be bonding the thermal material.

Morgan: I should have mentioned that from the point of view of the supply, we do supply prepregs as well, of course. Bonding layers with these thermal properties are available so that you can just build that in later into the process, with or without a heat sink, for that matter. You don't have to use aluminum on the back of that. You can use whatever you like.

Holden: In that sense, the designer has to now think about heat paths, much like they worked with electrical paths because part of the PCB is going to be the construction of this heat path to properly get into these materials and things like that.

Morgan: That's still a possibility, but with most applications, you don't have to consider the heat path so critically because most of them aren't really leading edge. You might have a very high emitting device or a very high-power device that you have to put a copper coin underneath, perhaps, to conduct it down to the layer where the heat will be dissipated. But the general principle is it's a matter of spreading the heat out.

Second, you then emit that heat from whatever you have as a radiator at the back of the IMS typically into the environment. That's the second part of the equation. I recall those days, Happy. There used to be devices bolted onto big metal structures to dissipate the heat. You can generally do that now using just PCB technology and not have to worry about the mechanics, but I wouldn't rule it out.

Shaughnessy: What advice would you give to designers who are just now starting to work with designs and know there are going to be thermal challenges before they even start?

Morgan: The key advice I'd give them is to talk to the material suppliers early on. That's what I always tell designers. The PCB is often the last thing to be designed and the first thing to be needed. That's a saying that's been around for a while, but it's very true. People think it's just an interconnect, but you have to consider that this PCB now is handling not just the electrical flow, it's handling the thermal flow as well. You have to have that in mind from the beginning. Again, talk to your suppliers and say what your need is.

We've experienced some great conversations with OEMs, where we've been able to come up with a really good solution because they've involved us from the very beginning. When you know from the outset what's required, you can advise much better, and this can result in a lower total system or product cost. Talk to your suppliers. Then, the whole supply chain will be linked up as well. In terms of supply chain design, from the end-users to the PCB manufacturing suppliers, the more we can talk together, the more we can find better solutions that meet the market need at the right price point.

Shaughnessy: Thank you, Alun. I appreciate your time.

Morgan: It has been great talking to you, Andy. **DESIGN007**

Allegro MicroSystems Acquires Voxtel, Inc. to Drive Eye-Safe LiDAR Solutions

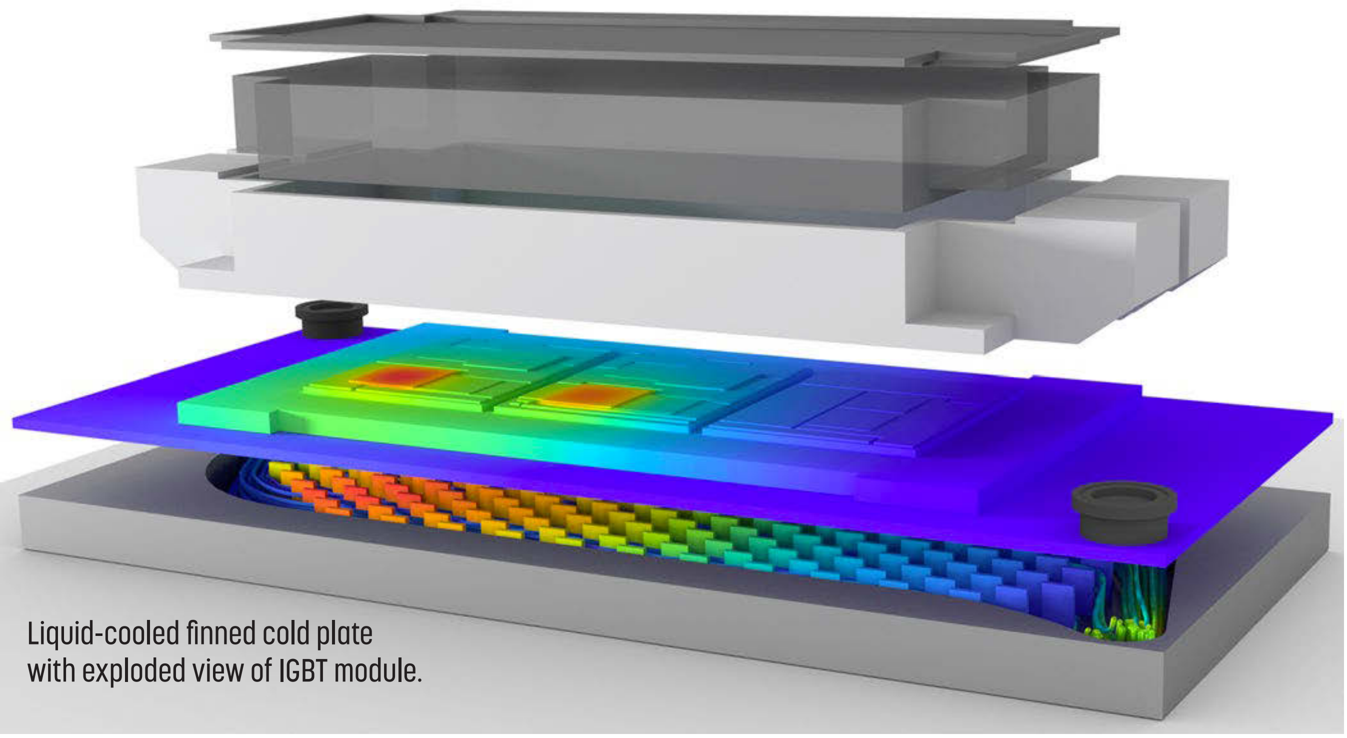
Allegro MicroSystems (Allegro), a global leader in sensing and power semiconductor technology, announced the acquisition of Voxtel, Inc, a privately held company specializing in advanced photonic and 3D imaging technology including long-range, eye-safe Light Detection and Ranging (LiDAR). This acquisition brings together Voxtel's significant laser and imaging expertise with Allegro's automotive leadership and scale to enable the next generation of Advanced Driver Assistance Systems (ADAS).

Voxtel, Inc. has been pioneering photonics since 1999, developing cutting-edge solutions for military, space, automotive and surveillance applications. Its ultra-miniature lasers, read-out integrated circuits (ROICs), and near-infrared (NIR) and short-wavelength infrared (SWIR) photodetectors, supported by more than 38 US patents, represent one of the broadest LADAR/LiDAR photonic technology suites available in the market today. Allegro's innovative portfolio of motor drivers, position sensors, regulators, and current sensors provides most of the key semiconductor components in the transmit and receive blocks of automotive LiDAR systems.

LiDAR typically uses lasers, photodetectors, and readout integrated circuits (ROICs) with time-of-flight (TOF) capability to measure distance by illuminating a target and analyzing the reflected light. LiDAR technology provides the high-resolution, three-dimensional information about the surrounding environment necessary to make fully autonomous driving a reality. It also supports adaptive cruise control, complements car cameras and radar and adds situational awareness.

Historically, a barrier to broad adoption of LiDAR technology in vehicles has been the restriction of maximum power output of the laser in order to comply with eye safety guidelines. Allegro's photonics portfolio now includes devices made in silicon and InGaAs, providing components for both eye-safe, long-range 1D or 2D scanned front-facing LiDAR and side- or rear-facing FLASH LiDAR. Devices based on InGaAs operate at wavelengths at which the human eye is less sensitive (1500-1600nm), enabling higher laser power levels for longer range object detection beyond 200 meters.

(Source: Globe Newswire)



Liquid-cooled finned cold plate with exploded view of IGBT module.

Everything You Need to Know to Beat the Heat

Feature Interview by Andy Shaughnessy
I-CONNECT007

When we started planning this issue on thermal design and management, we knew we had to check in with Dr. John Parry. He has been involved with computational fluid dynamics for decades, joining the U.K. firm Flomerics when it opened in 1989. When Mentor, a Siemens Business, acquired Flomerics in 2008, John joined, too, and is now strategic business development manager. I asked John to discuss today's thermal management challenges, his advice to newcomers to this segment, and how software tools, such as FloTHERM, can help technologists beat the heat.

Andy Shaughnessy: John, what are some of the biggest issues that PCB designers and engineers now face in thermal management?

John Parry: The biggest challenge is increasing mechanical and electrical integration. There are four consequences from a thermal standpoint.

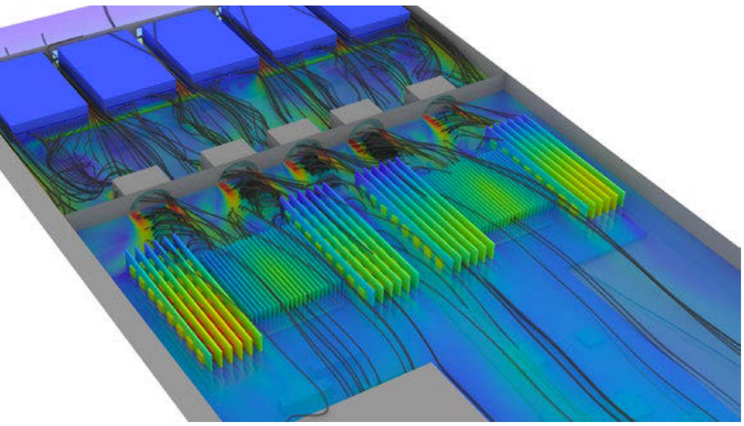
John Parry

The first is that as products have miniaturized, the power density per unit volume has gone up, despite attempts to reduce the power consumption of the components by lowering switching voltages.

The second is that there is less free space within the product. That's critical for an air-cooled product, as space is required to get the air through the system to cool it.

The third is less obvious, but as the free space is reduced, so is the option to make any remedial design changes if the equipment is too hot. In the worst case, the whole design may need to be scrapped, and the best-case scenario is weeks of rework.

A fourth consequence is that it is no longer possible to design equipment to run continuously under worst-case conditions, such as the maximum power consumption arising from how the product is used. It is often no longer possible to design to a lower thermal design



1U server showing effect of internal fans on heatsinks and DIMMs.

power, even in moderate ambient conditions. That means that the thermal design has to consider how the user experience is going to be impacted, when, rather than if, the equipment gets too hot. With thermal performance now tied to the performance the end-user sees, thermal design is receiving more focus.

In part, it is these types of considerations that led us to develop Simcenter Flotherm XT as a sister product to Simcenter Flotherm, which includes a Parasolid-based solid modeler to help users work more easily with native CAD geometry. We have also invested effort in software features that support active thermal management, such as clock frequency control, to reduce power.

As design margins have shrunk, thermal designers require increasing fidelity in late design, which has led to a focus on modeling components in more detail, and using test-based characterization to calibrate simulation models to give 99 + % accuracy on the temperature in both space and time. Boards today can be modeled taking into account the local copper coverage, which strongly influences how heat passes from the components into the board.

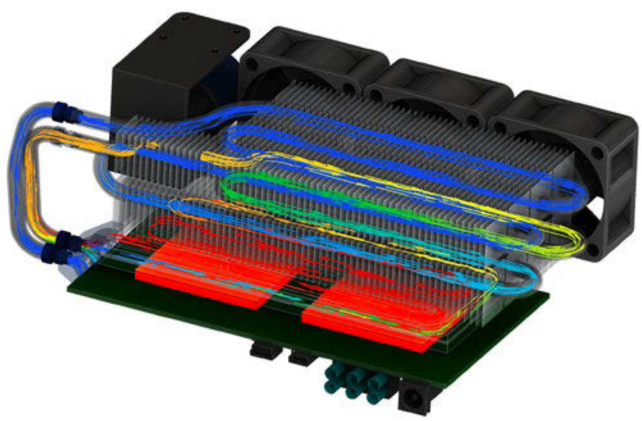
Shaughnessy: Tell us about Simcenter Flotherm. How does this tool help engineers address thermal challenges?

Parry: Simcenter Flotherm was developed as a tool specifically to help designers solve thermal problems in electronics. What we realized many years ago was that the electrical engineers were designing components and PCBs in isolation from the system that the board would be used in, so the environment for the board was unknown. Mechanical engineers responsible for the overall integrity of the product, including thermal performance and reliability, would subsequently have to take whatever action necessary to cool the board. That means building a thermal model of the entire system which they can use to try out different ways to keep the board temperature and the temperature of key components down to acceptable levels.

To help users build models quickly, we developed Smartparts, which are intelligent modeling objects of common cooling components like fans, heatsinks, etc. which make building models in conceptual design fast and robust. Over the years, a lot of sophistication has been added, particularly in the way in which these Smartparts represent boards and components.

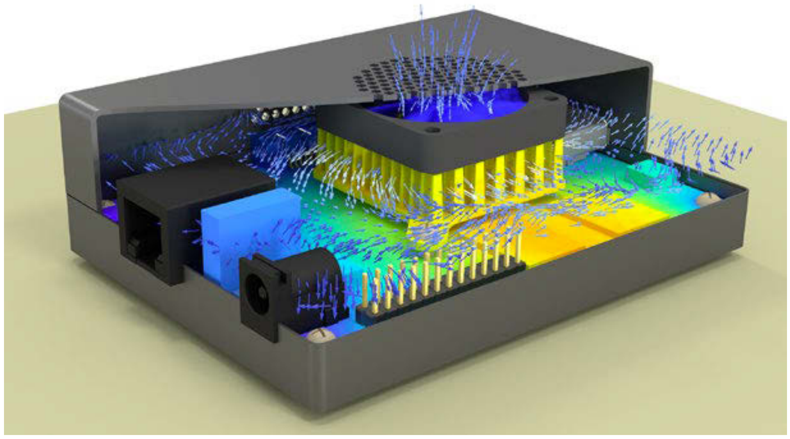
Shaughnessy: You'll get a chuckle out of this. Happy Holden recently told us that when Mentor first acquired the FloTHERM tool, he couldn't believe that he was able to do 3D fluid dynamics on a Dell computer, and not a Cray.

Parry: Yes, it is impressive, isn't it? When we started, Flomerics recognized that most of the computational fluid dynamics (CFD) world was moving in the direction of body-fitted meshes, where the mesh used for the simulation is distorted around the objects in the model. While this has advantages for model-



Automotive sensor fusion box with liquid-to-air heat exchanger.

ing aerodynamic type applications when dealing with a small number of discrete objects, we recognized that electronic systems are built from many hundreds, if not thousands of objects. In Simcenter Flotherm objects carry information about the mesh refinement they need, so they can be moved around in the model or stored in the software's library infrastructure and used again in another model, or provided from a supplier to a customer to use at the next packaging level. In Simcenter Flotherm, the meshing is instantaneous.



Minnowmax MAX board with fansink.

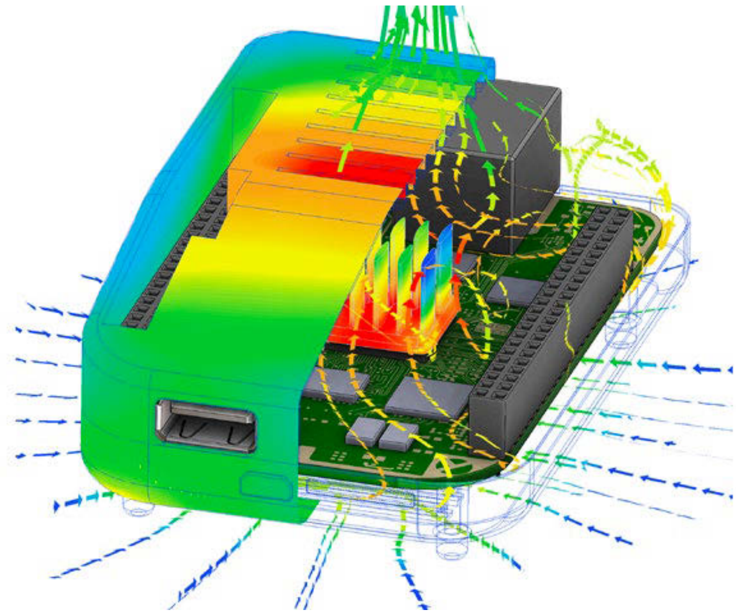
The time overhead of creating a body-fitted mesh was prohibitive back then, and there is additional overhead in terms of computing time per mesh cell. That may be warranted for aerodynamic-type challenges, where the only thing that matters is the fidelity of the CFD, but not for electronics cooling. The reason is that the focus is not on predicting lift and drag, which depend entirely on the airflow, but predicting temperature. A large proportion of the temperature rise we are attempting to predict occurs within the solid structures, from the die outward, and not in the air, so the need for sophistication principally lies in how the components and boards are modeled from a thermal perspective. That sent us down the road of using a Cartesian-based mesh approach, and we haven't looked back. Other tools are now rediscovering the value of Cartesian cell topologies.

Shaughnessy: We're starting to see more companies in the PCB community paying attention to thermal management now. What segments are driving this trend?

Parry: With device miniaturization has come reduced switching voltages to reduce power consumption. While the power consumption per transistor has been reduced, the number of transistors has exploded, so the power dissipation per unit area at the board level has increased. That means that the current running through power and ground planes, and power delivery nets, has increased to the point where the current flowing through the copper heats it up, so we now need to consider the board itself as a heat source, not just the active components. The reason this is affecting the PCB design community is that the temperature rise in the copper changes its electrical properties, so we are starting to see situations where, to close the PCB design, that has to be taken into account. The PCB design flow needs to be made temperature aware through tools like Mentor's HyperLynx PI and its interfacing with Flotherm.

Electronics systems today are a long way from being simple boxes with boards and lots of space. Even data center servers are densely packed, with power densities now at a level where the main CPUs may be liquid cooled using chiller blocks, or the boards fully liquid cooled. Some of the biggest challenges are being faced by companies in industries that fall outside of traditional electronics, such as automotive. This is everything from electric vehicle powertrains, where power electronics are used as an inverter/converter between the motors and the battery, to ever more advanced driver assist systems, including head-up displays that the driver directly interacts with and thorough to sensor fusion boxes used to process sensor data in autonomous vehicles, where the amounts of data being processed are huge, and processing dissipates hundreds of watts.

5G is a big challenge both for mobile devices and wearables and for the networking infrastructure to support it. With 5G, we are seeing



Beaglebone black with heatsink design for overclocking.

more sophisticated active power management approaches being taken to manage the heat while minimizing the impact on the user's experience.

Shaughnessy: What advice would you have for any designers and engineers who are just starting to deal with thermal management issues?

Parry: Companies often focus on thermal problems at the point they find them, which is in late design or prototyping. For the product that is in trouble, that's clearly the right focus, and simulation can really help understand the problem and what the possible remedies might be to save the product or project. Companies often repeat the mistake by not considering thermal in the next project until late design. It is an easy habit to get into because it is easier to wait until everything is known before building the model.

That's the wrong approach, and also a difficult way to start with thermal, because there is a huge amount of data from the EDA system about components and boards, the MCAD system about the enclosure and other mechanical aspects of the model, information on cooling solutions, material properties and powers, some of which may have to be entered manually.

What's required is to start early and start simple, building a model of the entire product, which can provide insight quickly, especially if the architecture of the product is different from what has been created before. That model can then be evolved over the development as more information becomes known about the design, for example importing the layout once this is in the EDA system. Before that, a rough idea of the layout can be used based on discussions with the board designers, so information about how the proposed layout behaves thermally can be investigated and proactively fed back to the board design team. The following quote from a friend of mine perfectly sums it up.

Wendy Luiten, thermal specialist and DFSS Master Black Belt, once said, "Your thermal design is made or broken in a few vital early architecture choices. It is absolutely essential to figure out what they are and then guard these choices through the entire design flow. These can easily be choices that electronics engineers and mechanical engineers overlook."

Shaughnessy: Good stuff. Is there anything else that you'd like to add?

Parry: Thanks for the opportunity to have this discussion. Thermal design is a growing area, and we are continuing to invest in developing our tools to meet future challenges. One really exciting area is in the use of reduced-order models (ROMs), where we have a technology that allows the ROM, once created, to be used in any environment. These ROMs can be solved 10,000X faster than the full model in CFD, so they are a potential game changer, particularly when exported in SPICE or VHDL-AMS formats for use in conjunction with circuit simulation software.

Shaughnessy: Thanks for your time, John.

Parry: Thank you for the opportunity. DESIGN007

PCB007 Highlights

I-Connect007 Editor's Choice: 5 Must-Reads for the Week ▶

Nolan Johnson's top 5 picks this week include the SpaceX Dragon splashdown, the Mars 2020 mission's Ingenuity helicopter—featuring an interview with the carbon fiber company that built the helicopter's landing gear—and the U.S. Air Force's efforts to secure space systems with the help of volunteer hackers. Readers also responded to news from IPC and iNEMI, and blockchain turned out to be hugely popular.

The Right Approach: Guerilla Tactics to Pass Any QMS Audit, Part 4 ▶

Concluding Steve Williams' four-part series on "Guerilla Tactics to Pass Any QMS Audit," he shares Tactic 10 on techniques to reverse a finding.

Trouble in Your Tank: CAF Formation—Correction of Misrepresentation of Origins and Causes ▶

In Mike Carano's words, "In my April 2020 column in PCB007 Magazine, I incorrectly misrepresented the origins and causes of conductive anode filament (CAF) formation. This follow-up column will provide more insight and depth of knowledge on the CAF failure mode."

Summit Interconnect Inc. Acquires Integrated Technology Ltd. (ITL Circuits) ▶

Summit Interconnect Inc. is pleased to announce the acquisition of ITL Circuits.

Testing Todd: Too Much Automation? ▶

The last six months have brought monumental changes to commerce, manufacturing, recreation, and almost every aspect of our daily lives. Todd Kolmodin shares his thoughts on how much automation is enough.

Got a Question? Just Ask Joe! ▶

A few months ago, we launched our "Just Ask" series with Happy Holden. Many readers took us up on it, sending all manner of questions for happy to answer. Now, Joe Fjelstad—inventor, technologist, author, and Flex007 columnist—is getting in on the action. Here's your chance to pick Joe's brain. What's the one question about this industry that you've always wanted to ask Joe?

Punching Out! Due Diligence: Quality Inspection for Business Sales ▶

Although the due diligence process can be exhausting, Tom Kastner explains how it is important that buyers and sellers keep their eyes on the prize of closing, stay positive, and don't allow emotion to run the deal.

Sunstone Circuits Launches New Text Message Notification Feature ▶

Sunstone Circuits—a PCB solutions provider for prototypes, medium-volume, and production quantities—announced new optional Order Status Text Alerts (Sunstone Order Status) communication platform.

Ladle on Manufacturing: LED UV Cure—Does It Really Work? ▶

Machines that have been made to UV cure inks used in printed circuits and other manufacturing processes have largely used vapor lamps. In the search for good alternatives, Marc Lade explains how LED technology has been hovering in the background, but it has struggled to position itself as a serious contender.

Arlon EMD Launches New Website ▶

Arlon EMD, a specialty electronics material manufacturer, based out of Rancho Cucamonga, California, announced the launch of its new website.

Thermal Management for PCB Designers: Staying Out of the Fire

Tim's Takeaways

Feature Column by Tim Haag, FIRST PAGE SAGE

The Life of a PCB

If there's one thing in life that really feels the pressure of being in the hot seat, it's the PCBs that we design. After putting up with the trauma of having copper added and then etched away through exposure to ultraviolet light and various chemical baths, you would think that the PCB would deserve a little break. Instead, the board goes from the frying pan into the fire, so to speak, as the different layers get laminated together. This involves a great deal of heat and pressure, as the epoxy in the prepreg is melted to fuse the PCB layers together. Next comes drilling and plating, which is also no picnic, and by this point, the heat and pressure should finally be over for this little guy, right? But now the board needs to be assembled.

Our plucky hero has gone through all kinds of processes to complete its fabrication, including some intense scrutiny by both automated equipment and human inspection. Now, it's back into the oven again—literally—for PCB assembly. Once the board has had its components pasted down onto it, it will be subjected to temperatures in the solder reflow oven that can get up to 255°C. That is almost 500°F for those of you who are thinking that perhaps it really isn't so bad. Let me just say this; there isn't a sunblock in the world with an SPF-value high enough to help with this kind of heat.

Not every PCB that is manufactured will go through the solder reflow oven—you're right. But if they don't go through reflow, they're most likely go through wave solder instead. If you're thinking that going through a wave sounds a little more pleasant than going through an oven, think again. We're talking about a molten wave of solder, which can get up to 270°C if lead-free solders are used. How would you like to dip your toes into that kind of a wave?

Removing heat from high-power LEDs

Aismalibar
COOLING ELECTRONICS

Most of the electrical power in a LED generates heat rather than light approximately 70% heat and 30% light output. If the heat generated is not effectively removed, the LEDs will run at higher temperatures, which lowers their efficiency and decreases their lifespan, making the LED design less reliable.

Aismalibar Insulated Metal Substrates ensure excellent thermal management of high-powered modules, where the efficiency of the product and its operational life is unquestionable.

Discover our laminates for PCBs:
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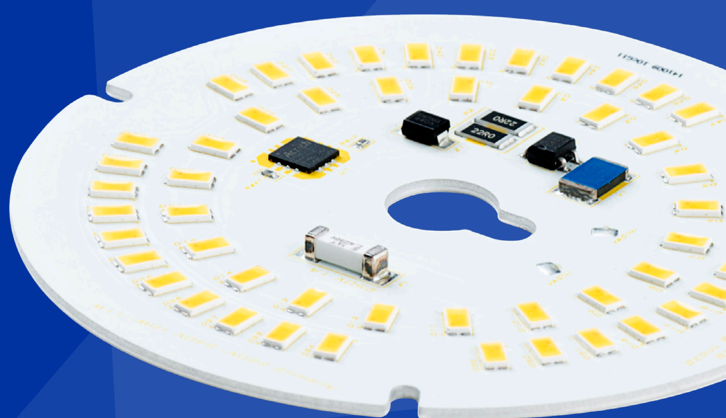

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As you can see, the PCB deserves our admiration for all the heat and pressure it has to deal with during manufacturing, but that is just the beginning. Next comes the regular day in and day out thermal stress of the board's normal operating environment. All those electronic components can generate a lot of heat in themselves, and life for the board can get pretty toasty. That is what PCBs are created for, though, and why PCB designers like you put so much effort into designing them to survive and flourish in all that heat.

A PCB Designer's Job

We start by designing boards with symmetrical layers of precisely-controlled copper evenly spread out to help with the fabrication process. We also take care in the placement and routing of PCB components to ensure there aren't any problems with soldering during assembly. Additionally, we design the boards with their operating temperatures in mind by giving hot parts the space they need, as well as placing them where they can leverage the airflow across the board for cooling. We also use thermal vias to distribute heat throughout the board and incorporate heat sinks, fans, and other thermal management tools and devices, as necessary.

As PCB designers, we are accustomed to using a variety of procedures to manage the heat on our PCBs. However, the question is, "Do we give the same level of attention to managing the heat in our jobs as PCB designers?" Many designers tell me that they often find themselves under a lot of pressure while doing their work, which puts them squarely in the hot seat, looking for a fresh breeze of relief.

Four Techniques

We are already good at PCB design thermal management, so let's consider four techniques in thermal management for PCB designers that might help.

1. Plan a Schedule

A lot of folks will ride the wave of the day in the performance of their jobs without any sort of planning at all. While this works for repetitive tasks, it can create a lot of stress for those who have schedule obligations that must be met. Certainly, we have our meetings and other company events planned in advance, so why not put a schedule around our design work too? The goal here is to prevent everything from piling up at the last moment and creating a catastrophic train-wreck with your deliverables. By planning regular milestones as you work, you can better manage the project's long-range delivery dates and give yourself plenty of room to make schedule adjustments along the way, if necessary.

2. Manage Interruptions

When working in an environment where there are continual interruptions, it can be easy to get frustrated as each new interruption raises our temperature another notch. For PCB designers, this can be especially troublesome as the design process involves keeping several sequential tasks going all at the same time. "This via can move over as soon as this resistor is rotated, which I can do as soon as these traces are re-routed, which can only happen after I slide the capacitor a little down and to the left…" You can almost see the tasks floating around a designer's head like little bubbles until an interruption causes all the bubbles to simultaneously pop, taking all those ideas crashing to the floor with them. To avoid this, try scheduling times when you shut down electronic interruptions and go dark to the outside world for a while. Of course, this requires planning so that other team members (and your boss) know what you are doing, but carving out blocks of uninterrupted time in your schedule can be a real game changer.

3. Document the Process

The temperature in the design room often gets elevated through poor communication. People may not know what they are supposed to be doing, or they may not know what you are doing. The best way to remedy this is through documentation. Make sure that everyone knows who the stakeholders are and who is calling the shots. It is also helpful if everyone has access to project schedules and timelines.

Also, take the time to take some notes. I'm not talking about writing a novel here; just keep up with some simple entries in the project log. This makes it much easier for people to pick up where you left off, or for you to demonstrate why or why not certain tasks have or have not been completed.

4. Relax a Little

When the heat is on us, it is easy to get really wrapped up in our work. I'm sure that all of us have found ourselves working through the night on more than one occasion to get an important project out the door. The concern, though, is that having such a tight hold on what we are doing may make it difficult to let go when we need to. Sometimes, board designs change in mid-stream or even get canceled, and that can be really tough to deal with if we are hanging on too tight. What's worse is to find out that we've made a mistake somewhere along the way and now we have to go back and correct it. Relax. We're all human, and mistakes happen, so let it go. The important thing is to learn from any errors we have created so that we don't make those same ones again. Take a deep breath and forgive yourself, and then get back into the game again.

Conclusion

There is one thing in life for certain: when an object gets too hot, it will change. In PCB design, we know this better than most, which is why we design our boards to manage an excess of heat. Objects that overheat tend to get crispy, inflexible or even melt away, which is the last thing we should allow to happen to us as PCB designers. The world of electronics design is constantly changing, and we must remain flexible to stay ahead of the rapidly changing curve and avoid the pressure that could lead to a melt-down.

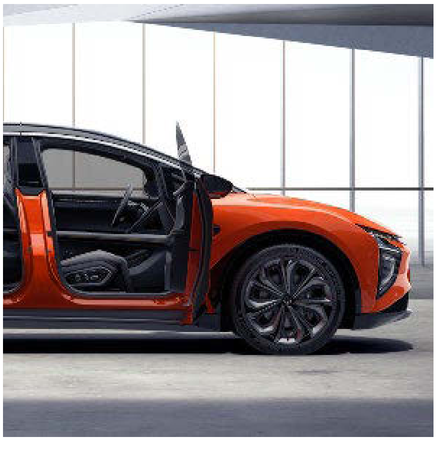
What do you think? Has this helped to turn the thermostat down in the old design room yet? Remember, you already know how to manage the heat in your design to protect it; now, take the time to do the same for yourself. Until next time everyone, keep on designing. **DESIGN007**

Tim Haag writes technical, thought-leadership content for First Page Sage on his longtime career as a PCB designer and EDA technologist. To read past columns or contact Haag, click here.

HiPhi X Launches With Electronically Controlled NT Door System

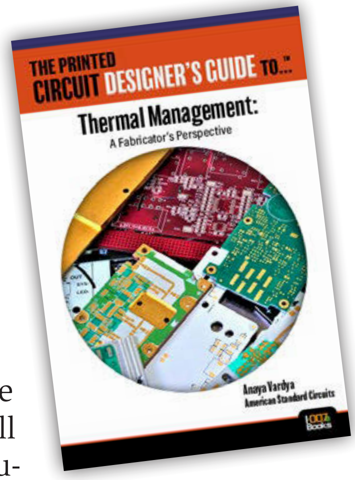
HiPhi, Human Horizons' premium, smart, all-electric vehicle brand, is excited to announce the application of its world-first NT Door system on the HiPhi X. The innovative new entry to the premium automotive segment will debut at the 2020 Beijing Auto Show.

HiPhi X, the first model of the HiPhi brand, is positioned as a self-learning, supercar-inspired SUV, adopting the world's first Human Oriented Architecture (HOA) enabling a secure, developer-open software platform. HOA comprises of 6 "super brain" domain controllers, connected by 1G Ethernet, over 500 sensors, and a 5G-V2X technology network.



HiPhi X comes with 2 battery options, the larger being a 96 kWh unit. The battery technology, highly efficient electric drive system and a low drag coefficient of 0.27, delivers a range of 610 km (NEDC). The HiPhi X will accelerate from 0 to 100km/h in just 3.9s. The advanced vehicle has been developed with dual-redundant systems which is a key enabler for its Level 3 autonomous driving capability. The HiPhi X is equipped with the worlds-first NT Door system, Programmable Matrix Lighting (PML), Intelligent Signal Display (ISD), a theatre-style co-pilot screen and other leading technologies to bring users a truly new experience.

(Source: PR Newswire)



An Excerpt From the Book
'Thermal Management: A Fabricator's Perspective'

Feature by Anaya Vardya
AMERICAN STANDARD CIRCUITS

Introduction

Thermal management in the printed circuit board (PCB) world is big business! A recent Markets and Markets report projects the thermal management market to reach $16 billion by the year 2024 with an average CAGR of 8% over that period [1]. This is one of the fastest-growing segments of the PCB business and far outpaces the projected growth for the overall industry. While demand was originally driven by high-power telecommunication and mil-aero applications, it has rapidly expanded to include automotive, consumer electronics, and medical sectors. The components used in any electronic assembly generate heat whenever an electrical current flows through them, and the amount of heat depends on the particular attributes of the design (power requirements, design characteristics, transmission speed, etc.).

In addition to the heat generated from the electronic components, the resistance of the electrical connections, copper trace configuration, and PCB via structures contribute to the thermal output of the product. While RF/microwave and IMPCB applications hold the lion's share of thermal management challenges, reduced PCB footprints combined with increased component densities can require advanced thermal management solutions on "vanilla" designs.

In our experience working with PCB designers throughout the years, there is a wide range of knowledge on the design side regarding the impact of thermal management design decisions on the PCB manufacturing process, and ultimately, product success. As we strenuously encourage early engagement between the designer and the PCB fabricator in all cases, it is particularly critical when developing an advanced thermal management solution. A disconnect between what the original design manufacturer (ODM) wants in performance and what the printed circuit fabricator recommends for the application is the biggest reason for an unsuccessful build of a new PCB design.

It is important to understand a couple of terms right from the start: thermal conductivity and thermal management. Thermal conductivity is the property of a material to conduct heat, while thermal management is the process of analyzing the system as a whole and effectively dissipating the thermal energy away from the heat source.

We have chosen to focus this book on providing designers a thermal management desk reference on the most current thermal management techniques and methods from a PCB fabrication perspective, including a case study on an extreme mixed-technology design that we recently produced. We hope you find value in our efforts. DESIGN007

Reference

1. Markets and Markets, "Markets and Markets report projects the thermal management market to reach $16 billion by the year 2024 with an average CAGR of 8% over that period," July 2019.

To download ***The Printed Circuit Designer's Guide to... Thermal Management: A Fabricator's Perspective,*** click here. You can also view other titles in our full library. Check out other books from American Standard Circuits, including *The Printed Circuit Designer's Guide to... Fundamentals of RF/Microwave PCBs* and *Flex and Rigid-Flex Fundamentals.*

Thermal Laminates:

One More Tool in Your Toolbox

Feature Interview by the I-Connect007 Editorial Team

Jeff Brandman, president of Aismalibar of North America, discusses the company's thermal materials and how they can help designers and engineers facing thermal challenges. He also details which segments are driving the development of these materials and offers tips for technologists who are new to dealing with thermal issues.

Andy Shaughnessy: Jeff, tell us about Aismalibar and some of your thermal materials.

Jeff Brandman: Thank you for having me. I appreciate the opportunity to speak to you. Aismalibar has been a manufacturer of PCB laminate pretty much since PCBs started being manufactured, and it has been involved in FR-1, FR-2, FR-4 materials, as well as CEM-1 and CEM-3. In the late '90s, Aismalibar saw that there was a huge opportunity in thermal management and became the first manufacturer to produce insulated metal substrates in Europe.

Shaughnessy: Give us some more info on the thermal laminates. What should a designer or electrical engineer look for, and what's driving the development of these laminates?

Brandman: The largest segment for thermal laminates that we're involved in right now is the LED market. LEDs have come a long way since they were originally introduced into the market. They've become extremely small and efficient, and the footprint that's needed on a PCB for an LED right now is extremely compact. Even though the LEDs are becoming very small from a footprint perspective and efficient from a heat perspective, that just means that designers are going to cram more into a smaller space. As a result, the opportunity to move the heat outside of that area is extremely critical. A lot of our products at the moment are designed for this industry. A lot of our clients in volume use our products for the automotive industry.

Shaughnessy: If a designer is working on a board that you know has these thermal issues with LEDs or whatever it may be, how can these materials help that designer?

Brandman: Traditionally, many designers have been really focused on the thermal conductivity number, watts per meter kelvin. How much heat can you move in your PCB away from the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LED? However, the thermal conductivity number is not necessarily the most important number because if you're taking a single side of an application, where you have your copper, dielectric layer, and heat sink, which could either be copper or aluminum, you want to move the heat from that active copper layer. If you find the material that has five mils of dielectric but has 10 watts per meter kelvin, on paper, sometimes designers get really excited about the super-high thermal conductivity number.

But the number that is important to focus on is either thermal resistance or thermal impedance, and where we try to focus our technology is to make that dielectric layer as thin as possible to be able to move the heat as quickly as possible. Sometimes, the thermal conductivity is not as high as 10, but with a solid thermal conductivity number and an ultra-thin dielectric layer, the opportunity to move the heat is quite significant.

Shaughnessy: You mentioned that designers often over-design boards with thermal requirements, which makes the board more expensive and difficult to manufacture.

Brandman: As a laminate manufacturer, we get a lot of PCB shops reaching out to us. They say, "We have this drawing for this PCB. Which of your materials best fits this drawing?" A lot of times, I'll see a specification in a single-sided material where the aluminum back or the copper back is a weird thickness. For example, a very common thickness for that copper or aluminum back is 1.5 millimeters, but then I'll see people stack 2 millimeters or 78 thou, or 2.5 millimeters or 100 thou. What the designers may not realize is that although they may be getting a small percentage of other proof thermals for doing something like that, the cost of the PCB could double or triple.

Maybe you're going to see 1–2% in the junction point temperature on the LED, but is it really worth all that extra money? Sometimes, designers design ultra-conservatively because that's their nature, and that's good. But at the same time, more communication with the PCB shops and the laminate manufacturers could be really positive to value technology vs. cost.

Jeff Brandman

Shaughnessy: It seems like you would have to communicate with the fabricator and the laminate maker when you're dealing with these boards where you just see hotspots all over.

Brandman: We get a lot of designers from OEMs who reach out to us about their design, asking, "Which would be the best material to suit what we're designing here?" In those cases, I make recommendations based on cost vs. technology. I try to remind them, "If you put 3-ounce copper here, that's going to be a lot more expensive than you think. Is there a way that you can do this with two-ounce copper?" Most of the time, the designers are quite receptive to these recommendations.

Shaughnessy: If they've never dealt with this sort of material before, does it change the way the designer does the layout in any way?

Brandman: For a PCB designer who hasn't had experience working in a heat application, there would be a learning curve, but many PCB designers who have experience with heat, whether it's single-sided or multilayer, would be able to pick up the advantages of using these types of materials right away.

Shaughnessy: Automotive is one of the big drivers. I just read that automotive sales are up this year in North America, despite COVID-19. Do you see that?

Brandman: We're involved in several North America-driven automotive programs in the full cycle, from supporting design, prototyping, and production. The year started really strong, where pretty much all of the programs we're involved in were at either full capacity or close to full capacity. Then COVID-19 happened. Because automotive is not part of the critical supply chain, a lot of that business was completely shut down for 4–6 weeks.

April was a very scary month for everybody because no one really knew what was going on in the world and the impact COVID-19 was really going to have. Globally, when everyone understood where things are at with COVID-19, the factories opened back up. When they opened back up, they didn't go from 0% to 25%. They went from 0% to 125% because they needed to make up the time on these programs from having the factory shut down. Other than being shut down on these programs for a short period of time, it has been a very strong year, production-wise.

Barry Matties: On the automotive side, what trends do you see? We see a lot of e-cars coming out. How is that playing into your market? Do you see more demand in that area?

Brandman: We're looking at that right now. We have people reaching out to us with respect to e-cars, but keep in mind the production of e-cars at the moment is only a small fraction of what gasoline cars are, so many of those opportunities are still in their infancy. And a typical design cycle for the electronics and automotive industry until it goes to production is a few years.

Matties: It seems like an emerging sector.

Brandman: There's a huge opportunity for growth. There are a lot of opportunities for prototypes floating around right now, which is really in a power conversion side of things. The top market we're focused on is LEDs. Power conversion is also another market where we do a lot of business, and that's moving heat, but it's really focused on electrical installation and assurance of that electrical installation.

Matties: Are the heat demands greater or less for e-car aside from the LEDs?

Brandman: Like power conversion, you need to have a solid dielectric to ensure electrical installation. You're going to be able to move heat, but there are going to be some barriers as far as how much you can move because you need to have that electrical installation. On the lighting side, a lot of the high-end, high-power LED headlights work with a pedestal light design where the LED has an isolated thermal pad, and they're putting the isolated thermal pad right on top of the copper heat sink. The electrical pads are still on top of the dielectric. They're moving the heat from the LED right into the heat sink with no dielectric. The capability to move heat in that pedestal lighting scenario is significantly greater than in the typical power design because in power, you're going to have pretty solid dielectric, and you're going to be pretty limited by it.

Matties: There are also environmental aspects of thermal that will never go away.

Brandman: Typical automotive testing for laminates and PCBs is about -40°C to +125°C, and they do a lot of thermal cycles in this area. I'd say automotive is one of the markets where they do the largest amount of thermal reliability testing on the PCBs. It's very hot in Arizona, but on the other side, people are driving the car in Alaska in the winter, and it has to work in both scenarios, no matter what.

Matties: That's a tall order to fill. You mentioned more communication around the designers with fabricators and material suppliers. We've been hearing this for years. Is it happening, or is that still just a wish?

Brandman: It's happening. We're in communication with a lot of designers. They contact us all the time, but I also run into a lot of cases where the designs weren't well thought through, and I wish that the designer had reached out to a PCB shop or a laminate manufacturer. Sometimes, designers design things that are great on paper but are not always great in reality. When you talk to front-end engineering people in a PCB shop, a lot of the time they're going back to the customer, saying, "Can we change this on your design? It was really hard for us to manufacture that." That's pushing the limits on that process for anybody. Those conversations right now are mainly happening organically. There's no formal communication. People are just designing something. They like our material or someone else's, and they go on Google to contact us out of the blue, which is great, but I'd love to be involved in promoting that communication.

Matties: How is everything going from a business perspective?

Brandman: Business is good, and our people are doing well. Our factories are in Spain. That was a scary time, especially when the [COVID-19] numbers were going crazy in Spain, but we never closed or stopped going to the office. We were able to stay open, but we had to reduce our shifts and really be smart about it.

Shaughnessy: What advice would you give to somebody who is new to designing boards with thermal issues?

Brandman: My best advice is to reach out to your PCB shop and even reach out to the laminate that you're specifying. When you're designing, ask them if there's any input that they would have specifically on the design that would be helpful. If that conversation happens, it will really help them in the long run.

Shaughnessy: Communication eliminates a lot of problems.

Brandman: Everybody has expertise and experience. When you engage other people who know what they're talking about and what you're trying to do, you're always going to learn quickly.

Matties: Jeff, it has been great to catch up with you.

Brandman: Thank you so much. I look forward to meeting you again when things look a little better globally. **DESIGN007**

MilAero007 Highlights

Aurora Circuits on Ultra-Heavy Copper PCBs ▶

It's always fun to talk with a company that can do something different—in this case, ultra-heavy copper PCBs, meaning over 20-ounce copper. Wanting to know more, Dan Beaulieu talked to Aurora Circuits Director of Business Development Thad Bartosz.

Understanding MIL-PRF-31032, Part 2 ▶

In Part 2 of this series on understanding the military PCB performance standard MIL-PRF-31032, Anaya Vardya explains how the first step in the process is to develop a quality management plan (QMP).

From the Hill: 7 Steps for MIL-PRF-31032 Certification ▶

Mike Hill's past columns have detailed how military electronics are being used in an ever-increasing application rate. In this column, he shares seven certification steps, resources, and timetables for consideration when certifying to MIL-PRF-31032.

Electronics Manufacturing Industry Applauds Congressional Actions ▶

IPC, the global electronics manufacturing association, applauds leaders in the U.S. Senate and House for approving IPC-backed measures that will bolster the resiliency and security of the U.S. defense electronics industrial base.

NASA Awards Rapid IV Contracts for Spacecraft Systems and Services ▶

NASA awarded contracts to five aerospace firms for the Rapid Spacecraft Acquisition IV spacecraft and related services. Each contractor has one or more core spacecraft offerings available under their contract.

U.S. Air Force Awards Virtual Reality Training Contract to Street Smarts VR ▶

Street Smarts VR, whose virtual reality training platform is used across U.S. military and law enforcement organizations, announced a contract with U.S. Air Force Global Strike Command (AFGSC) Security Forces that deepens their commitment to maximizing readiness for Airmen through more realistic training.

NASA Astronauts Safely Splash Down After First Commercial Crew Flight to Space Station ▶

Two NASA astronauts splashed down safely in the Gulf of Mexico for the first time in a commercially built and operated American crew spacecraft, returning from the International Space Station to complete a test flight that marks a new era in human spaceflight.

Goodwinds Composites: Putting a Helicopter on Mars ▶

On July 30, 2020, Nolan Johnson spoke with Leland Holeman and Amelia Cook, the owners of Goodwinds Composites. While Goodwinds may be a small business, they still pack a heavy punch in the carbon fiber fabricating business. Case in point, the NASA Perseverance Mars rover mission, which had just launched as we captured this interview, carries a helicopter (named Ingenuity) in its payload and contains custom parts fabricated by Goodwinds.

Sandia Labs Honors STEM High School Students ▶

Sandia National Laboratories honored 26 girls from California high schools in the Tri-Valley, East Bay, and San Joaquin County at the annual Sandia Women's Connection Math & Science Awards.

Monsoon Solutions: Creating the Perfect Fab Notes, Part 2

Interview by the I-Connect007 Editorial Team

We recently spoke with Monsoon's Jennifer Kolar, vice president of engineering, and Dan Warren, principal PCB designer and director of designer development, about some of the common problems that they see in designers' fab notes, the impact that bad data can have on the fab process, and the steps that designers and design engineers can take to ensure that they are creating complete, accurate fab notes every time. This is the second half of the conversation that began in the August 2020 issue of *Design007 Magazine*. Click here to read Part 1.

Andy Shaughnessy: Do you try to educate each customer if the data is inaccurate or incomplete?

Jen Kolar: We try to silently help for the first few designs if they have poor data. When we see a trend, or if the data is unbuildable, we start pushing back. We try to absorb and clean up as much as we can. We're pretty careful and keep track of when we are doing a new spin. We'll also track what questions and issues came up previously, so they're ready to be incorporated into the next spin. We try to make sure that the PMs will remind the designer/customer, "I had these questions last time. Can you make sure to make these changes next time?"

For internal designs, we also have a policy that, in general—unless it's during weird hours—whichever designer did the work, they get to be part of answering the DFM. We get to share the love. They find out what the issues are, but they also get the pain of the late-night call.

Nolan Johnson: That's part of what we've heard too. The feedback loop breaks down after you shipped the board because, by the time that job is done, there are four or five jobs down the road.

Kolar: Right. That's something where, internally, our folks do get that feedback—maybe not all of it, but they get a lot of it. Darin, our COO, and I are the ultimate escalation point for all DFM. Our fab vendors have our cellphone numbers, and they know to call us and not put the job on hold on the weekend without trying to reach us. We have this process in place, but then our designers hear about it. It's like, "I was just up for three hours in the middle of the night. This wasn't so fun. Next

Jennifer Kolar

time, would you please make sure to regenerate the drill drawing."

One of the things that we added in our fab notes that have uniformly saved us at least 24 hours every time is that we call out overhanging parts in assembly. If you haven't told the fab vendor in advance that you have overhanging parts, how are they supposed to know? They send you back a panel to review, and then you say, "Wait, I need X millimeters of clearance in each of these different areas." People don't think about assembly when they do fab notes. They think the parts should be in assembly, but they're fundamental to the panel. That's one example of something that massively improved our throughput. It's so simple.

Shaughnessy: What would you say are some of the most common problems that you see in fab notes that just never seem to go away?

Kolar: Some of the biggest problems are not updating drill tables, not having the dimensions match the Gerbers, or having every possible impedance in the world in the table, even if not used. Another problem is having multiple boilerplate notes that don't apply and may contradict. Some companies have boilerplate fab notes that are like, "If it's a production build, do this, or for an ENIG finish, do this, and for OSP do this." Another problem we see often is not calling out important things, such as, "Don't add thieving in this area with all the copper cleared out."

Dan Warren: I want to touch on the impedance. It's pretty common that you'll get a layer stack back from your fab shop up front, so you tell them, "I want 90-ohm pairs, 80-ohm pairs, and 50- and 45-ohm single-ended." They'll come back, and every layer will have that calculated. Some people put all of that in the fab drawing, even though that 90-ohm pair may only be on two layers. If it's called out on any of the others, most fab shops will stop and question you: "We can't find this on any other layer. Is it supposed to be there?" You just lost a day. Don't put anything on the drawing that's not in the database.

And I know it's tedious, but I go through every one and match my impedance on my layers and make sure that table's up to date. There's nothing extra in there. I'm not saying I don't miss one once in a while, but I make an effort to ensure there isn't extra data in there. We've gotten people out of the habit of just copying the layer stack from the fab shop.

Kolar: That's a common one, in addition to not calling out intentional shorts.

Warren: We had quite a few questions on some of these common areas before our current process. Once we added to our processes and made it part of our notes and it became a part of our stock drawing example, we don't get many calls on that anymore. But as far as the stuff not getting updated, anything that has to be updated manually is usually the stuff that doesn't get updated and causes a problem, even if it's just something simple. One of my pet peeves is why have a note with the drawing number in it, the drawing number is already on the drawing, and then you added another note over here with a call-out, and you have to update all three?

Kolar: We treat design as a first-order engineering effort. We care about the quality of what we put out. We want the boards to look nice, not just work. We want the product to be consistent and look nice. That's something we also really indoctrinate in our folks, and we've had to indoctrinate in the new folks. "No, it's not just throwing slop together and getting it over the wall. It does matter how it looks. There's a reason why, and you'll learn when you get to more complicated designs."

Warren: As Jen said, we try to let everybody know how important it is. I've had to flat-out tell a designer, "If you keep producing this, you're not going to be around here much longer." And that it's worth the extra effort of having processes and monthly design meetings. We have monthly principal design meetings with five of us principal designers. We all have 30+ years of experience, and we go over the fab notes and other processes. A lot of companies, especially smaller ones, don't see the value in doing that because they have limited resources, but we benefit from the effort of doing that.

Kolar: A lot of electrical engineers look at the layout as a connecting-the-dots exercise. They don't value the effort. They balk on quotes that include time for iteration and documentation. There's a lot of pushback on that, and many service bureaus only care about billing by the hour. We bill by the hour, but our employees are not pestered or paid based on the hours they bill. We aren't trying to have our designers billing at 100%. We typically think, "Do you have about 24 billable hours out of each week?"

Barry Matties: A couple of things strike me. One, it looks like you're looking at this not from a price point of view but a total cost point of view, which makes a lot of sense. The other is that it all starts with design. It's a domino effect: it's crap in, it's crap out.

Warren: I agree. That's funny; that's what I heard when I started as a designer.

Johnson: Shifting gears, what trends in design do you see? We know that there are a lot of new high densities, smaller packaging, etc.

Kolar: It seems like new aerospace companies pop up about every other minute, such as new satellite companies.

Warren: Everyone wants to launch something into space. They don't know what it is, but it's going into space.

Shaughnessy: What's your greatest challenge right now?

Kolar: We have a lot of different big projects going on, and we tend to see cutting-edge stuff a lot. That's pretty fun. A lot of times, we'll have challenges in finding a vendor who can build the designs. That has nothing to do with design. It's just, "Here's the customer requirement. We need a vendor that can build this."

That's where we end up. Because we are on the cutting edge a lot with design, it's a challenge to find a fab vendor that can build something. Then, it is working with the customer to figure out, "It could be built if XYZ." We try to iterate with our vendors and customers, rather than just saying, "This is impossible." We work with the fab vendors or the assemblers, and say, "In which case are we okay with violating IPC rules? In which cases are we okay with doing this? If we just did this? Yes, they would accept the rest and build it." That's where we have the biggest challenges. Otherwise, it's just time. Everybody wants things faster than possible.

Warren: One of the things I see as a challenge is that everything's getting smaller and smaller. We were just talking about DFM and early DFM involvement by the designer. Instead of waiting until the end of the design, I just finished one part that had the smallest clearances, and the smallest vias I'd ever done on a board. I wish I could tell you details, but I can't because it's proprietary. But I went through three DFMs with the fab shop before we came up with something that worked for me to get the design done and worked for them to get the board fab kit. I started early with DFM once I got the CPU pinned out.

Dan Warren

I had a pretty good feeling that I could do it in X number of layers. I knew this is what I wanted, so I threw it to the fab shop. They came back and said, "Okay, that sounds good." But once I got into the routing and was about halfway done, I ran it back to the fab shop and had them do a full DFM on it. They came back and said, "This is good. But this clearance here has to go because we need more space." They explained why, and it all made sense. By the time it was sent to fabrication, we'd ironed out all the issues.

Shaughnessy: We've heard from CAM people who have customers who say, "Why are you asking me all these questions? The other shop never asked me that stuff. Why don't you just build it?"

Kolar: And some shops to do that. We've had issues with that because a lot of times, we do earlier builds for customers that will later go to production. If they don't hear issues because the assembler just happened to manually work something in or we don't know the fab vendor scrapped half the boards, then the customer won't learn until way too late downstream. We educate our vendors not to be a black box so we can learn from the builds. Internally we try to be that special magic for our customers and hide as much of the mess under the covers as we can, but we want to make sure they're learning anything important from it at the same time. However, you're right that a lot of shops, depending on the philosophy of the shop, it's about being close enough to go, and at close enough, they go.

Matties: I appreciate your passion. It's exciting to hear your excitement as you discuss what you do and how you follow a process.

Warren: Thank you.

Shaughnessy: What advice would you give to new designers as far as creating fab notes or documentation in general?

Kolar: Think in terms of quality and the things that you need to convey. We have a whole series of things we ask customers when doing a layout. We don't assume what is or isn't high current. We ask a ton of questions up front. What is it that you want to be known about this so that it doesn't get screwed up? What's going to happen if somebody picks it up in five years and you're not available, and they go to build it? Will they be able to do it? Is it a standalone package? When we have EEs who were doing the design and their own layout, they almost never do fab notes.

For them, part of it is helping them treat layout as a first-class task and not as a second-class task and having them understand how important that is in the process. A number of our customers are at companies that feel like, "Any EE can do layout." There's very much that philosophy.

Warren: Care about and take pride in your work. Learn from your mistakes and take time to do it right. A good layout is visually great to look at; it's clean and organized. Don't be sloppy, and don't think you know everything.

Happy Holden: I'd like to reiterate what Barry said. It's really a pleasure to talk to an organization that has the customer and quality and the process in mind. I want to commend you for that. I'm glad to see that there are organizations like you out there, and we need to spread the word. What percentage of fabs that you work with are capable of thinking like you and working on some of these tough, new things that are coming down the line?

Kolar: We carefully pick our vendors. We don't use any "bucket shops." Sometimes, we just have simple four-layer test boards, but we work with our customers and vendors as partners. We try to have them see that if they're struggling with something or we're struggling with it, we're in it together. We're pretty good at picking partners who want to do the same thing. We've worked with the best shops. We try really hard. We don't just put our partner under the bus.

Holden: A couple of weeks ago, in a conversation with a fab vendor, we heard the same kind of story: The fab notes seemed to be this lost, ignored art. But as both of are saying, there are best practices out there. Some people make money by throwing it over the wall because it seems like a quick and cheap way to do it. But in the long run, it always comes back. Somebody's going to pay for it.

Kolar: We've seen some customers that do their own designs as if they have enough money and don't care. We're on a fourth-spin design while the first one is still going in fab because they found some mistake, and they threw it over the wall at us again and said, "Start this one now," and then did the same thing again later. They're leapfrogging because they just care so much about going fast, and their budget allows it. This may not be the EE's choice; it's just the company and industry pressure.

We've worked with the best shops. We try really hard. We don't just put our partner under the bus.

Warren: I've been doing this for 34 years now. I have one engineer that if he called today, I would hang up the phone. Other than that, I don't really have a mental list of customers. There are a couple of fab shops that I hate working with, and I'll do everything I can to avoid it. Most of the rest that we work with are great.

Matties: Obviously, don't name the names, but what makes it so bad to work with these shops? Why is that?

Kolar: They don't hold the schedule, and they aren't transparent in any way about the process that they'll say, "It's booked. We'll have it by this date." And then you hear nothing. When you reach back out five days later, you hear, "We just started DFM, and we just put this on hold." The clock will start over when they resolve it, and you've just lost a week.

Matties: When you look for a fabricator, what's the most important attribute?

Warren: Communication is huge. As Jen said, I had a pretty complex board before I joined Monsoon. It was a 12-layer stacked via board, and they had an internal process problem, but I learned all this after the fact. The day the boards were supposed to be delivered on a six-week turn was when I got a call, saying, "We ran into a problem, and we had to rerun them." While the problem was known four weeks before, they tried to bring in the date, and when they realized that they couldn't, then they finally called me.

Then, they had another problem, and I was supposed to get boards on a certain date. Again, I didn't find out until the day after that the boards weren't coming. By the time we got the boards back, the engineer had thrown them in the garbage because we had moved so far beyond it. If they would have communicated with us what was going on, we might have just said, "Forget it," and not built that second batch that they were doing and saved them the headache of building that second batch. But it was just all lack of communication.

Kolar: And it's a lot that's put on the EEs now, not just that they throw it over the wall; it's their schedule, too. Plenty of our customers just assume that any EE should be able to do a layout, that layout is trivial and easy, so there's a lot on their plate. We have many excellent customers, including ones who also have solid processes for design and fab, but in conversations like this, that can get overshadowed by all of the challenges.

Holden: It's as if they don't believe it takes a village to raise a child; it takes a team to design a PCB.

Kolar: Especially one that's manufacturable. A lot of them don't understand manufacturing. The most complicated, crazy designs we get are from junior engineers who have no idea how a stackup comes together.

Matties: This has been great. Well done. We appreciate your time.

Kolar: Thank you. We appreciate it. DESIGN007

How to Know If a CAD Tool Is Right for You

Connect the Dots

by Bob Tise and Matt Stevenson, SUNSTONE CIRCUITS

Carpenters have hammers, bricklayers have trowels, and painters have their brushes; for PCB designers, the tool that defines us is our CAD software. Designers spend hours, days, or weeks in their CAD tool for each circuit board design, examining each connection, plotting each through-hole, and carefully placing each specific component. They discover quickly that not all CAD tools are created equally.

How can designers find the right CAD tools to fit their particular methodology and needs?

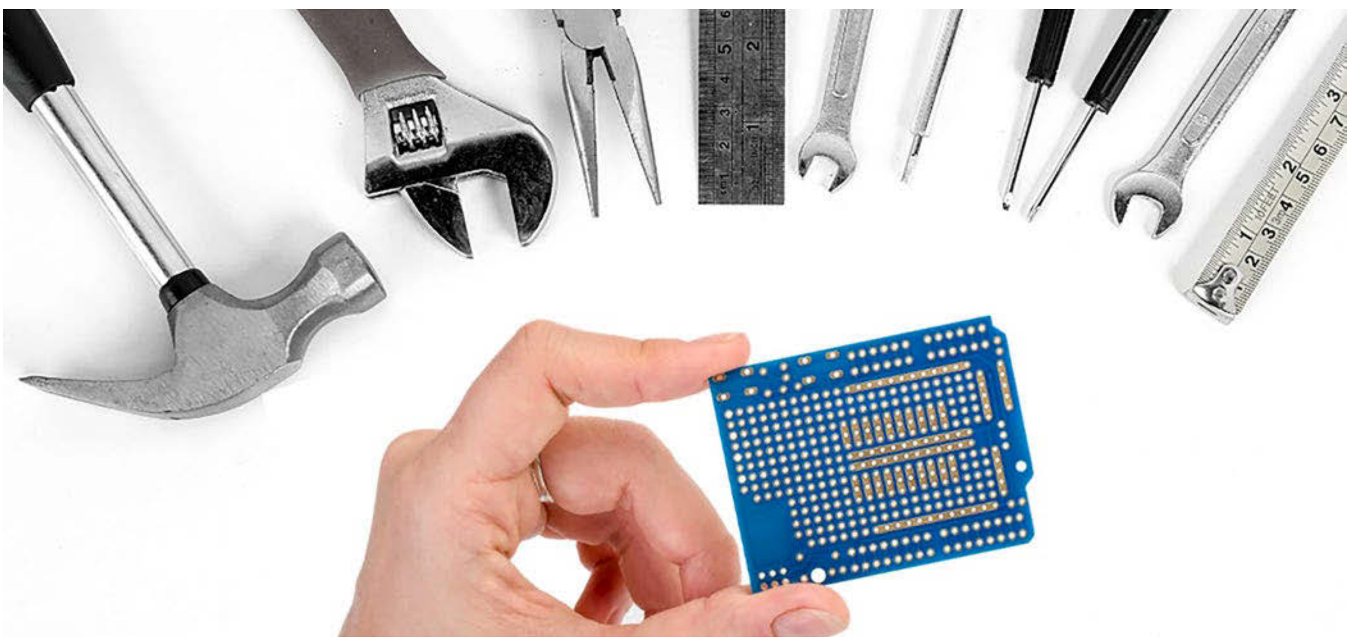
Not every designer spends the same amount of time immersed in a CAD tool. Some designers may just work on a few designs per year, which means there is limited opportunity to learn the ins and outs of complex CAD software. They definitely won't have the time to invest in heavy customization. Sporadic use can also equate to a limited software budget to invest in an expensive CAD package or heavy customization of the one they have. Some designers go right from one design to the next with barely enough time to catch their breath, making that high-priced CAD tool a bargain due to its versatility, customizability, and sheer raw power. No names here, but we've worked with some real hotrods.

What's Available in the CAD World?

A quick search reveals that the world of PCB design is flooded with tools. We read one article [1], promising "46 Must-Have Tools to Streamline PCB Design." The average PCB designer is too busy to evaluate more than a handful of tools. To narrow the field, we need to look at some basic criteria.

Price

For hobbyists and part-time PCB designers, the price will most likely be the most important



criteria, so let's look at that first. Luckily, there are lots of low-cost and free CAD tools available, keeping students and hobbyist designers in the game.

When evaluating free tools, though, pay close attention. Some of them will be open-source or community-run projects, and while the philosophy behind them might be attractive, make sure those tools are still being actively maintained. When you run into a problem, you want to make sure you can get help.

Some low-cost and free CAD tools are funded and developed by PCB manufacturers. They produce tools that specifically work with their manufacturing process, which can be great if you have a specific manufacturer in mind. However, this choice can also lock you into a specific manufacturer path, so choose carefully. If your CAD tool is tied to a manufacturer, can you get the Gerber files? Do they cost money? Is the price reasonable?

Commercial packages can become expensive quickly. There are a few CAD tools available that charge a monthly subscription price, but most offer prices ranging from about $75 all the way up to over $2,000. Pay attention to the limits placed on products with multiple tiers of pricing and be particularly careful not to get caught in a "freemium" trap, where a piece of software seems great until that really important feature is locked behind an expensive paywall.

Design Tip: If you have a PCB manufacturer in mind, make sure their process is compatible with your CAD tool before you spend any time or money on it.

Component Libraries

CAD tools should be customizable with libraries full of parts and components, but you need to be sure that the tool you're looking at can support the parts you need to use. Many tools like to brag about the size of their parts libraries, but don't be fooled by a big number.

A typical designer might need a library of about 10,000 parts, but when looking at the library offered by a CAD tool, are you finding the parts you need? Look for commonly used parts and check whether the tool comes with proprietary libraries or access to specialized libraries.

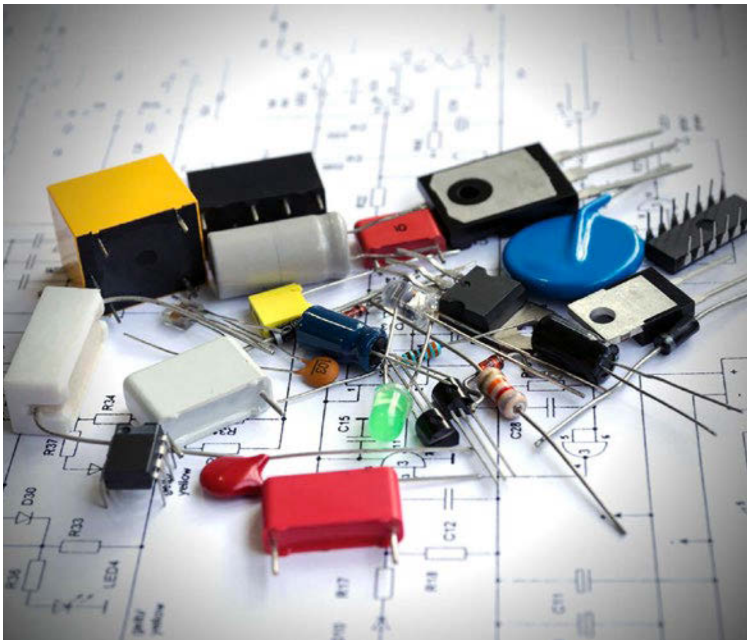


Figure 1: Are you finding the parts you need?

No matter the CAD tool, eventually you'll have to create components yourself. Make sure the tool provides the capabilities you need to both create new components and add them from external sources.

Complexity

CAD tools exist to tackle the complex problem of designing PCBs. Unfortunately, it's inevitable that your CAD tool will itself be somewhat complex, but that doesn't mean you shouldn't evaluate a tool based on how intuitive and easy it is to use.

Ease of use is an area where open-source software tends to lag behind. If the price is an important factor in your choice, you may end up looking at a balancing act between price and usability.

Help and Documentation

There will come a time when something in your PCB project will get too complicated, and you'll end up needing help. You want to make sure that help is available before you put too many hours into a CAD tool, so evaluate these resources early in the process. Check out the tool's documentation. Some tools make their documentation available online. Look for YouTube tutorials and websites that might be offering solutions to common problems. If there is a phone number for support, call and ask some questions.

Those last two suggestions—checking the tool's documentation and looking for video tutorials— can also help you evaluate a CAD tool without even downloading it. If there are too many people reporting problems, that might mean the tool is too difficult to use. Likewise, a YouTube tutorial that takes the viewer through too many convoluted steps can be a red flag toward usability.

Figure 2: CAD software should be customizable.

Final Thoughts on Finding the Right CAD Tool

CAD software is almost always highly customizable with design rules, favorite libraries, shortcuts, and modules to increase productivity and make the design process personalized and special.

Designers add their own libraries of specific ICs, parts catalogs, and components to make sure the right pieces are available. Getting all of these customizations just right can take a long time, so a designer doesn't want to invest a lot of effort in one CAD tool just to abandon it and start over with another.

Pay attention to limitations, such as board size, and the number of pins or layers a tool can support. Watch for limits on minimum component pitch and the supported sizes for traces, spacing, and vias. Once you have narrowed the field, download the CAD tools that look the most promising, and try them out. Fifteen minutes or so should be enough to tell if the tool is intuitive and will fit your PCB project.

The most important part about picking a CAD tool, though, is that it shouldn't make designing too much of a chore. You want designing to be productive and efficient, and in the end, maybe that's the most important element to evaluate when you're trying out different tools.

Design Tip: Double-check your components and ensure they have proper mechanical drawings. Be sure the physical dimensions of your components fit your design, not just the pins, and make sure your library parts match the datasheets; don't just trust them out of the box. **DESIGN007**

References

1. Trey Hooper, "Top PCB Design Software Tools for Electronics Engineers: 46 Must-Have Tools to Streamline PCB Design," Pannam Imaging.

Bob Tise is an engineer at Sunstone Circuits, and **Matt Stevenson** is the VP of sales and marketing at Sunstone Circuits. To read past columns or contact Tise and Stevenson, click here.

Bob Tise

Matt Stevenson

IPC-2231 Captures Board Design Best Practices

Design Circuit

by Patrick Crawford, IPC—ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES

Introduction

A few months ago, at the height of the global shutdowns due to COVID-19, I highlighted how working from home gave IPC volunteers more time to focus on standards development activities. For the superstitious readers out there, don't worry; while typing "the height of the global shutdowns" with one hand, I was knocking on wood with the other! Regardless of the unfortunate circumstances that enabled it, the labor of the past few months has started to bear fruit, and there are new document revisions being prepared for industry review throughout the IPC standards development ecosystem. This month, I would like to focus on one such document: the IPC-2231 DFX Guidelines, which is currently being revised into IPC-2231A.

DFX Guidelines

The IPC-2231 DFX Guidelines establish best practice methodology for use in developing a formal design for excellence (DFX) process for laying out printed board assemblies that utilize surface-mount and through-hole devices. But the X in DFX means so much more than a catchy way to stylize "eXcellence." It is a variable that can represent the many factors for a robust board design, including design for manufacturing, fabrication, assembly, testability, cost, reliability, environment, and reuse.

If you have not used IPC-2231 before, then think of it as a compendium of best practices to consider while designing your boards. For example, if your board includes any vias in thermal pads, then you might want to read the IPC-2231 section on thermal pad outgas-

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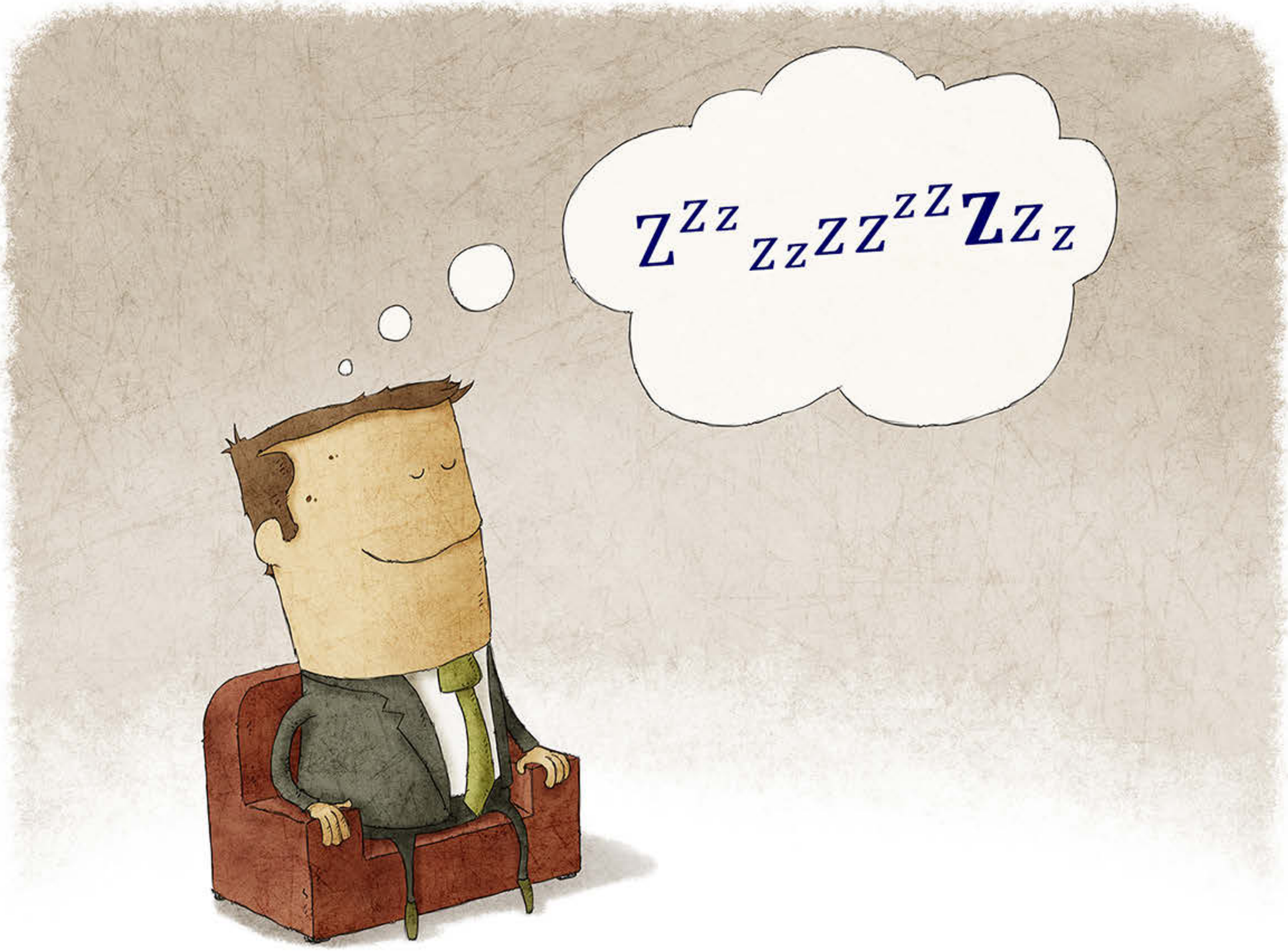

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sing before going any further with your design. Therein, you will find paragraphs of recommendations on how to mitigate outgassing, as well as references to other IPC and non-IPC guidelines and requirements for that specific issue.

Proposed Revisions to IPC-2231

While it is still in development and may change (more on that later, and how you can help shape it), the current proposed draft of IPC-2231A builds on its predecessor by proposing greater depth to many existing sections, streamlining others, and even adding entirely new content to better address design challenges faced by board engineers.

The printed board assembly design process section is proposed to be enhanced to better elaborate on the steps necessary to iterate through the design process: concept design and analysis, detailed design, first build, product validation, manufacturing validation, and support. Specifically, the detailed design step is proposed to be reinforced by additional detail concerning design documentation. An entirely new step in the process—manufacturing validation—is also being considered for addition to IPC-2231A. The largest proposed addition to the IPC-2231A is a brand-new section on design impacts on fabrication processes and includes discussion, recommendation, and references to help the user design for critical fabrication processes—such as the application of surface finishes or preparing a board for laser drilling.

Standards Development

But these proposed changes are exactly that—proposals. The servants of industry who have made these proposals comprise the IPC 1-14 DFX Subcommittee responsible for the development of IPC-2231A. As the IPC staff liaison to the 1-14 Subcommittee, I had the pleasure of attending every bi-weekly development meeting for the past year and listening in on how some of the leading experts in the field conduct their meetings and build their document. This group has three co-chairs from around industry: Karen McConnell of Northrop Grumman Corporation, Steve Golemme of Google Inc., and Dock Brown of DfR Solutions.

Along with a small group of dedicated volunteers, these three individuals have coordinated the recent efforts to revise IPC-2231. For those who might be unaware of how IPC standards are developed, the most common strategy is to deploy A-Teams who handle chapters, sections, or even single figures for a larger standard or guideline. The 1-14 Subcommittee employed these A-Teams to great effect by selecting individuals with the most expertise of the various DFX topics to work on those sections.

While this might seem so obvious as to be a trivial point, I think that it is worth exploring as a call to action. Even if you think that your expertise is only applicable to 5% of a given standard—not even necessarily an IPC standard—then that expertise is welcome. In the case of IPC-2231, there are many discrete subsections that deal with related, but not necessarily linked, topics. For example, in contrast to the thermal pad outgassing issue noted above, there is a section detailing design guidelines for system enclosures only five pages later. If you know very little about thermal pad outgassing but quite a bit about best practices for designing system enclosures, then your input on only that small fraction is critical for the good of the whole document. Of course, there are individuals who know "a whole lot about a whole lot," and they are more than welcome to sprinkle their knowledge over the entire document. This was the case for many of the dedicated industry veterans who donated their time and talent to the production of IPC-2231A.

IPC-2231A is currently in working draft and is being reviewed by the committee until September 18, 2020, at which point it may be tweaked per any feedback received after review. The final draft of the document will then be delivered to the industry for a mandatory 30-day review period. The beauty of transparent and open document development is that during this industry review period, any individual can render comments on the document, even if they are not members of the committee or have not previously worked on the document.

Summary

In conclusion, I will thread the sections of this column together. IPC-2231A is currently in the working draft, and there are proposals for additions to the document that greatly enhance its usability and value to designers everywhere. Your input into the document is welcome, and if you review the draft document and find that it is missing some critical other value for X, then you are invited to join the effort and have your voice be heard. If you would like to join the IPC 1-14 DFX Subcommittee, or if you would like to review the document as part of the final draft for industry review, please contact answers@ipc.org.

At its core, IPC-2231 is built to capture board design best-practices and condense them into a repeatable, reliable guide for creating excellent boards. After all, as the philosophical historian William Durant once wrote, "We are what we repeatedly do. Excellence, then, is not an act, but a habit." **DESIGN007**

Patrick Crawford is the manager of design programs and related industry programs at IPC. To read past columns or contact him, click here or email PatrickCrawford@ipc.org.

Veoneer, Qualcomm to Power Next Generation ADAS and Autonomous Driving Systems

Automotive technology company Veoneer, Inc. and Qualcomm Technologies, Inc. have decided to collaborate on the delivery of scalable Advanced Driver Assistance Systems (ADAS), Collaborative and Autonomous Driving (AD) solutions powered by Veoneer's next-generation perception and driving policy software stack and Qualcomm® Snapdragon Ride™ ADAS/AD scalable portfolio of System on a Chip (SoC), and Accelerators. This ranges from L1 to L4 systems uniquely designed to create an open platform for Tier-1 suppliers and Automakers.

Designed to address the growing complexities associated with developing advanced driver-assistance systems (ADAS), including safety compliance, the integrated software and SoC platform aims to address the growing needs of the automotive ecosystem for scalable and upgradable solutions, which require highly advanced and power-efficient compute, connectivity and cloud service capabilities across all vehicle tiers.

This platform will integrate Veoneer's fifth generation perception software and driving policy software with the current and future Snapdragon Ride portfolio.

The parties have signed a non-binding letter of intent and expect to finalize a definitive agreement during second half of 2020.

"We are pleased to work with Qualcomm Technologies to develop next generation solutions for ADAS and collaborative and autonomous driving. Working with a recognized leader like Qualcomm Technologies, using their ground-breaking Snapdragon Ride products, provides us the remaining piece of the puzzle. This relationship not only strengthens our product portfolio, but also broadens our go-to-market position and opportunities, while giving customers more ways to access world-leading technology," said Jan Carlson, Chairman, President & CEO, Veoneer.

"There has been a growing desire within the automotive ecosystem to have a full SoC and Stack solution that can scale from the entry tier of active safety systems to higher-end automated driving solutions. Combining our best-in-class product roadmap of integrated automotive platforms, which supports broader functionalities like 5G/4G, telematics and infotainment, with Veoneer's proven software stack for perception and driving, creates a unique offering to support this need. Qualcomm Technologies remains committed to offering high performance and advanced automotive solutions for all vehicle tiers and levels and we look forward to working with an industry pioneer like Veoneer to accelerate innovation to deliver comprehensive systems," said Cristiano Amon, President of Qualcomm Incorporated.

(Source: Qualcomm Technologies)

Education Unlocks the Golden Door to Freedom

The Digital Layout

by Kelly Dack, CIT, CID+, PCEA

"Education is the key to unlock the golden door to freedom." —George Washington Carver

Introduction

This month, I speak with the PCEA Educational Committee regarding the team's take on the PCEA's role in education. What do they have in store? Next, PCEA Chairman Steph Chavez weighs in on the strength of the Education Committee and why it is crucial to the PCEA's mission. Finally, along with our normally provided list of professional development opportunities and events, I give you a preview of what is in store for next month's column.

PCEA Updates

The PCEA Educational Committee discusses the importance of well-rounded technical curricula, as well as how they started in the industry. They cover available PCEA educational resources, including technical books, papers, and lunch and learn webinars, as well as chapter presentations and field trips. Upcoming presentation topics include materials, high speed, advanced placement and routing, power distribution, and flexible circuits. You will also learn more about the PCEA's mentor pairing program.

Kelly Dack: Today, I am speaking with Rick Hartley, Mike Creeden, Tara Dunn, Gary Ferrari, and Susy Webb. Thank you for coming together as members of the PCEA Educational Committee. One of the main goals of the PCEA, along with collaborating and inspiring the electronics community, is to find ways to engage our membership in the realm of education and seek out ways to fulfill their needs. How is that going?

Rick Hartley: Over the past few months, as we were generating content for our website, we

brainstormed ideas about what to offer our audience and how best to reach them. What you are going to hear from us is about efforts to share knowledge with our industry peers.

Susy Webb: Our website is chock-full of technical information. We provide informational links to guide industry professionals through links to technical papers. The topics range from general electronics theory to high-speed SI, EMI, power, flex design, HDI, and DFM. It is a very comprehensive list.

Our website is chock-full of technical information. We provide informational links to guide industry professionals through links to technical papers.

Mike Creeden: Not only do we provide a full page of content links under our technical info section, but we also have another full page of book references in our books section. We list works from authors including Bruce Archambeault, Eric Bogatin, Clyde Coombs, Clive Maxfield, Christopher Robinson, Lee Ritchey, Howard Johnson, and many more.

Dack: Let's talk more about what value-added content the PCEA Educational Committee is bringing to the electronics PCB engineering community. Do you have any plans for programs offering financial assistance or scholarships for young engineers?

Creeden: We have a spot explaining our mentor pairing program on our website. Our website is becoming quite automated, and we now have a way of taking feedback request data entered on the site and matching it with other solution data on the site.

Readers can find that on the education page of our website under the topic "mentor pairing." It is a very simple process to sign up for this service. We have a section to fill out if you would like to be a mentor or be mentored. Then, we have a place to fill in your areas of expertise and the software you use or are proficient in. This keeps users of the same category of software tools in the same family. We make the introduction to facilitate the mentoring relationship but then allow the mentor and mentee to take it from there. We feel this is a very good solution to fulfill the collaborative commission we speak about.

Dack: Gary, you've served quite a lot in the PCB fabrication industry. How did you get your start? Were you mentored?

Ferrari: I did not have any mentors on the electronics side. On the mechanical side, I was mentored in doing castings and other machine gears and metals technology through meeting contacts and by job shopping in the early years. Even as I moved around the country, I always had friends. Wherever you work, you should make connections and find somebody to share knowledge with. It's about planting seeds for lasting relationships.

Dack: You learned on the job from your co-workers and peers, which transformed into a network of friends and colleagues that you could tap into for advice wherever you found yourself.

Susy, you teach so many PCB design classes. Where did you fill your head full of knowledge early on?

Webb: Back then, PCB layout was an art. Now, it is definitely an electrical engineering trade, which is dramatically different. I gained a lot of knowledge by attending the many electronics trade shows and conferences that began to spring up, especially in the '90s. I learned so much from the speakers at these shows that I felt a compelling need to share the knowledge I'd gained with others, so I started teaching my own subjects at these conferences.

Dack: Tara, I know from first-hand experience that you are well-versed in teaching and mentoring folks in the electronics industries about flex circuit manufacturing and flex design and DFM. Did you start with a mentor?

Dunn: I got my start in the electronics industry just out of college, working for a small flexible circuit manufacturer. Working with a small company provided the opportunity to wear many hats and learn the PCB fabrication process and industry quickly. I was fortunate to work with several mentors helping me understand both flex technology and the PCB industry in general. Because of the foundation that effort provided me, I feel strongly about mentoring and helping others new to the industry, or new to flexible circuits.

Hartley: In addition to what we mentioned earlier, there will be a great emphasis on local presentations to our local chapters whose members have incredible backgrounds and much to share.

Dack: Susy, you emphasize the importance of going to these shows to connect and learn. Do you feel a need to facilitate education by getting your students out of the classroom and into a PCB fab shop or EMA site for a more tactile learning experience?

Webb: Getting our membership out to see the equipment that makes design so important is not to be underestimated. This practice has been implemented in many of our local chapters over the years. We have discussed ways of doing this in a virtual fashion recently with COVID-19. But there is nothing like showing up at a PCB shop with boots on the ground. It makes it easy to ask spontaneous questions and get feedback. Without feedback, it's hard to become a good designer.

Creeden: Rather than tell stories of mentoring, which people don't fully get, I explain it like serving as an apprentice under the guidance of a tradesman. We all grew up in the companies that hired us, and they modeled the designer hierarchy similarly by calling us first junior designers. As we gained knowledge, we became designers and then senior designers. The electronics industry has bypassed that system of gradual learning. Without understanding the complexities of the trade, management now just hires a new engineer and says, "Here is a 32-layer board design that will require HDI. Get 'er done."

Our industry has lost the apprenticeship. New EEs today may have taken a couple of day-courses in PCB layout or can find a 40-hour class offered by an organization, but there is nothing that will systematically build our profession like the unions of the trades.

Dack: In a sense, all company structures can facilitate an apprentice program in some way if they have the experience existing already within their staff. But if their staff is not experienced, they may suffer from intellectual inbreeding. Is this where the PCEA comes in? Does meeting within a local chapter fill this gap of outside knowledge by bringing it into the chapter via presentations?

Combatting intellectual inbreeding requires getting out of the office and being subject to new ideas and methodologies.

Hartley: Not only that, but it couples with the mentoring that we discussed earlier. Combatting intellectual inbreeding requires getting out of the office and being subject to new ideas and methodologies. Our presentations and mentoring are not only about learning a software tool; it can also be about a method or a process. A junior designer could mentor with any of us in the PCEA; besides some colorful language, who knows what they could learn! (laughs)

Webb: It is important to continue this type of education throughout your career because if you have only designed one board—and you think that if it was somehow built successfully, you are a board designer who can design anything—you might be surprised. The importance of continued learning is critical because the next board design could have an entirely different scheme of technology, which could cause you to fail miserably.

Ferrari: I've mentored several people over the years about how to grow their long-term career paths. I've guided them to look out for the future and where they want to go. Mentoring is all around, and we want to be a part of it because we feel we have the right experience in the PCEA to help. Our local chapters are dialed in to help, too. There is a lot of opportunity in our local chapters to ask questions and get help through presentations and peer review.

Dack: It has been really good to hear about your progress and plans for the upcoming months. Thank you deeply for your service to the industry.

Message From the Chairman
by Stephen Chavez , MIT, CID+


Stephen Chavez

Another month has gone by, and I am still amazed at how the PCEA continues to expand globally, as each day, week, and month comes and goes. There is so much positive activity taking place regarding the PCEA, as our membership continues to grow along with our sponsorships. As I take a moment to collect my thoughts on all the activities taking place, I can't keep myself from feeling a sense of euphoria that is still in the air from our grand opening in early July.

When I think about the powerhouse of industry professionals on the PCEA Education Committee, the first word that pops into my head is, "Wow!" The PCEA Education Committee consists of five main individuals whose combined industry experience is easily over 200 years. The PCEA is blessed to have the following individuals that make up the Education Committee:

1. Mike Creeden, technical director of design education, Insulectro (vice-chairman of the PCEA)
2. Tara Dunn, president and founder, Omni PCB
3. Gary Ferrari, executive consultant, Ferrari Technical Services Inc.
4. Rick Hartley, principal engineer, RHartley Enterprises
5. Susy Webb, senior PCB designer, Design Science PCB

At the core of the PCEA, our mission is to collaborate, inspire, and educate. These five people have been doing that on a daily basis for a very long time. They are more than industry professionals; they are also very close and dear friends of mine whom I have had the pleasure to come to know for over 15 years now.

At many industry conferences and workshops around the world, Mike, Tara, Gary, Rick, and Susy bring it. They pack the house every time they step up to the microphone, walk on stage, or set up to lecture as a featured speaker on many industry webinars. These five professionals are true industry icons. When I think about how blessed the PCEA is to have these five amazing professionals on our Education Committee, I strongly feel that we could not be in better hands moving forward.

Again, the most important thing that our PCEA Education Committee brings to the table is its combination of over 200 years of industry experience, along with endless wells of industry knowledge when it comes to printed circuit engineering.

If you have not yet joined the PCEA collective, I highly encourage you to do so by visiting our website (pce-a.org) and becoming a member. I continue to wish everyone and their families to be healthy and safe.

Next Month: Chapter Reports

You can distance this body but not this mind. You can't keep good folks down. This virus has certainly tried, but our PCEA chapter leaders have been working in the background on building plans for events to bring the membership in local areas together. Next month, I am looking forward to pulling our local chapter leadership together for some behind the scenes reaction to the challenges of COVID-19 and what they are doing to overcome its attempts to shut down our collaboration engines—the local chapter meetings.

Our chapter activities are coming alive, and our membership is benefitting from the synergy of their collaboration. Please look forward to my Zoom meeting interview with this dynamic group of leaders in next month's column.

Upcoming Events

- September 8-11, 2020:
  PCB West (Santa Clara, California)—***Virtual***
- September 28 -October 23, 2020:
  SMTA International—***Virtual***
- October 7-9, 2020:
  AltiumLive (San Diego, California)—***Virtual***
- January 23-28, 2021:
  IPC APEX EXPO (San Diego, California)
- January 26-28, 2021:
  DesignCon (Santa Clara, California)
- May 5-6, 2021:
  Del Mar Electronics & Manufacturing Show (Del Mar, California)
- May 11-13, 2021:
  IPC High-Reliability Forum 2021 (Baltimore, Maryland)
- November 10, 2021:
  PCB Carolina (Raleigh, North Carolina)

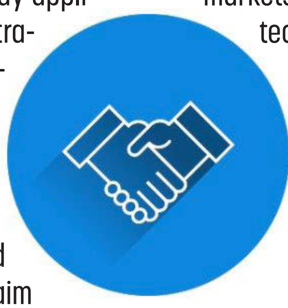
Spread the word. If you have a significant electronics industry event that you would like to announce, please send me the details to kelly.dack.pcea@gmail.com, and we will consider adding it to the list.

See you next month or sooner! **DESIGN007**

Kelly Dack, CIT, CID+, is the communication officer for the Printed Circuit Engineering Association (PCEA). To read past columns or contact Dack, click here.

Nordson Acquires vivaMOS, Adding Key Sensor Technology

Nordson Corporation has acquired vivaMOS Ltd., which designs, develops and fabricates high-end large-area complementary metal-oxide-semiconductor (CMOS) image sensors for a wide range of X-ray applications. This acquisition builds on Nordson's strategic objective to enhance its test and inspection capabilities for diverse end markets.



Based in Southampton, U.K., vivaMOS is a leader in its field for high-end large-area CMOS image sensors. The company was established in 2015 as a spinoff from the U.K.'s Science and Technology Facilities Council (STFC) with the aim of commercializing its X-ray image sensors. Its latest generation sensor offers a unique combination of speed, resolution and low-noise performance, enabling a wide range of X-ray applications.

"This acquisition gives Nordson differentiated and leading-edge X-ray sensor technology that will substantially enhance our product offerings across multiple end markets. Large panel CMOS sensors represent a critical technology for X-ray imaging. We look forward to further integrating the industry-leading sensor technology and expertise while developing new test and inspection innovations to offer our customers," said Jeff Pembroke, Executive Vice President, Advanced Technology Solutions.

vivaMOS will become part of the Test and Inspection division within Nordson's Advanced Technology Solutions segment. The terms of the deal were not disclosed.

(Source: Nordson Corporation)

Key Benefits of Resins and Differences From Coatings

Sensible Design

by Alistair Little, ELECTROLUBE

Encapsulation resins are available in many forms, with numerous properties that would challenge even the most diligent chemist. While we appreciate that most manufacturers simply want a resin to do the job without wading through all the subtleties a resin has to offer, we also understand how critical it is to get the product detail right in order to make product selection as painless as possible. With so many varying options to protect electronic circuitry, there's a lot of ground to cover. Depending on the application, sometimes a conformal coating may be more suitable, particularly with the two-part coating series that performs like a resin.

In this month's column, I'm going to focus on the benefits of using a thermally conductive encapsulation resin and compare the difference between using a resin and a conformal coating. I will also look more closely at the best way to mix a resin pack and what to be wary of if air bubbles get trapped in the cured resin. Without further ado, let's explore these frequently asked questions in our five-point format.

1. What are the benefits of a thermally conductive encapsulation resin?

As electronics have become smaller and more powerful over the years, the amount of heat generated per unit area on a PCB has increased as well, and it is well known that electronics will perform much better at low temperatures. Used for encapsulating PCBs or devices requiring effective thermal dissipation, thermally conductive resins are designed to allow heat to be dissipated away from sensitive components. The typical thermal conductivity of an unfilled resin is 0.20–0.35 W/mK. Whereas for a resin to be classified as being thermally conductive, it must have a thermal conductivity of >0.8W/mK. This is usually accomplished by using selected

ceramic fillers, which offer a combination of thermal conductivity and chemical stability.

2. What are some key differences between resins and coatings?

The most noticeable differences are the methods of application (aerosol, conformal coating spray equipment, manual spray gun, and brushing for coatings, compared to mixing and dispensing equipment and resin packs for resins), the thickness of application (< 100 microns for conformal coatings, < 500 microns for thick coatings and > 500 microns for resins), and approval ratings (coatings are generally approved to UL746, while for resins, it very much depends on the application). Because of the coating thickness, coatings occupy less space and have a low increase in overall weight compared to resins. There are both coatings and resins that are based on epoxy, polyurethane, and silicone chemistries, but there are also acrylate, acrylic, and parylene coatings that do not have a direct resin equivalent. 99% of resins are 100% solid systems, so they have low, or no VOCs released during curing, while many coatings are solvent-based, although there are two-component (2K) and UV curable acrylate systems that are also available as 100% solids.

3. Why would I choose a resin instead of a coating?

The choice between a resin or a coating is normally down to application specifics. If the unit involved is to be subject to long-term immersion in various chemicals, and subject to long-term thermal, and/or physical shock cycling, then a resin is generally preferred. Also, if there are a large number of large components on a PCB, it is generally better to use a resin to encapsulate these than to coat them. Another scenario where a resin would be preferable is when the unit will be used in a situation where it is not easily accessible, or long continuous service life is required. In this incidence, a resin would be recommended to provide the extra protection and durability needed.

4. What are the consequences of having air bubbles trapped in encapsulation resins, and does this impair performance?

Air bubbles can have a number of impacts upon the performance of the cured resin. Depending on the number and distribution of the bubbles, the actual thickness of the polymer layer applied will be decreased; hence, the level of protection will also be reduced, particularly against chemical attack. If there are air bubbles next to components, wiring, or tracks, then particularly when high voltages are applied, corona discharge can build up inside these voids and ultimately destroy the components or wiring. Voids also act as a weak point for thermal and physical shock, which can lead to the resin cracking in service.

5. Talk me through the best method for mixing a resin pack. Explain what can go wrong and why.

First, you need to remove the resin pack from the outer packaging. In the case of polyurethane and silicone resins, don't remove them from the foil pack until ready to use. Lay the pack out onto a flat surface and remove the centre clip. Use the clip to push the resin from one half of the pack to the other, then pick the pack up in both hands and mix in a circular motion for a couple of minutes. Place the pack back on the flat surface and use the clip to push the resin from the corners into the centre. Pick the pack up in both hands and continue mixing for a further minute.

Repeat pushing the resin from the corners into the centre of the pack and then continue to mix for another minute to ensure that the material is fully mixed and uniform colour. Use the clip to push the mixed resin to the side of the pack with the angled seam. Roll the pack film up so that the pack fits into the hand. Cut off the corner of the pack and then tilt the pack to dispense the resin, applying slight pressure as required to maintain the flow. If the material from the corners of the pack is not pushed into the centre of the pack, then unmixed material can be dispensed. If the resin is not mixed for long enough, then the resin may not cure, or it will have a patchy cure. In the case of filled resin systems, some sedimentation might have taken place over time, so it might take a little more mixing to ensure that the fillers are correctly distributed throughout the resin. With the optically clear resins, they will appear hazy when first mixed but this is perfectly normal and the haziness will disappear as the material reacts.

Conclusion

Every customer and project is different. While we can advise a customer as to which products are best suited to their needs, based on our years of experience, it all boils down to the unit, the dispensing method/equipment to be used, the curing times, and the temperature limitations that may be imposed during the production process. The more information that the customer can provide regarding the resin's ultimate operating conditions—temperature range, likely chemical exposures, and so on—the better. See you next time for more resin-related tech tips. If you have any questions for us, please get in touch. **DESIGN007**

Alistair Little is the global business technical director of the resins division for Electrolube. To read past columns from Electrolube, click here. Download your free copy of Electrolube's book, *The Printed Circuit Assembler's Guide to… Conformal Coatings for Harsh Environments*, and watch the micro webinar series "Coatings Uncoated!"

Ethertronics Releases First UWB Antenna Solutions for Samsung Electronics

AVX Corporation, a leading manufacturer and supplier of advanced electronic components and interconnect, sensor, control, and antenna solutions, announced that its AVX/Ethertronics Korea team has completed the development and mass production of the first ultra-wideband (UWB) antenna solutions to be integrated into Samsung Electronics products. Featured in the new Galaxy Note20 Series, which consists of new 6.7" Galaxy Note20 5G, 6.9" Galaxy Note20 Ultra 5G, and Galaxy Z Fold2 smartphones and was recently unveiled at the Samsung Galaxy Unpacked virtual event, the new high-performance UWB antennas are the result of a strategic partnership and collaboration with Samsung and enable faster, more effective and efficient communication between devices.

Manufactured using a flexible printed circuit laminate with low-permittivity (low-DK/DF) materials, the new UWB antennas require very little power to transmit large amounts of data at up to 8Mbit per second over ultra-wideband frequencies of 6.2GHz-6.7GHz and 7.7GHz-8.2GHz at close-range distances up to 10m. The efficient new UMB antennas also accurately detect other IoT devices within 30cm, providing Galaxy Note20 and Galaxy Z Fold2 users with faster, more efficient and secure communication.

"The new UWB antennas imbue the latest generation of Samsung's flagship Galaxy Series smartphones with the ability to deliver the high-speed, high-bandwidth performance necessary to support today's vast array of connected applications while consuming minimal power in order to help further prolong battery life," said Jeffrey Hilbert, Global Manager and Senior Director, AVX Antenna/Ethertronics. "We are extremely proud to be a strategic antenna partner to Samsung and to have had the opportunity to both collaborate on the first UWB antennas to be integrated into their proven product line and supply the main communication band antennas for their new Galaxy Note20, Galaxy Z Fold2, and Galaxy Buds Live products."

(Source: Global Newswire)

Let's Talk About the Basics of Flex

Consider This

by John Talbot, TRAMONTO CIRCUITS

Flexible PCBs, by their very nature, are designed to be flexible. This presents problems in securely and reliably attaching the ends of the flex circuits to a solid, stiff, main PCB or other electronic devices. A combination of hard, as well as semi-flexible, stiffeners is used for this purpose. Hard stiffeners used include FR-4, aluminum, as well as heat conductive aluminum-backed metals. A hard stiffener has a limit as to how close the flex circuit bends to the stiffener without stressing the joint or causing the flex circuit to crease (Figure 1).

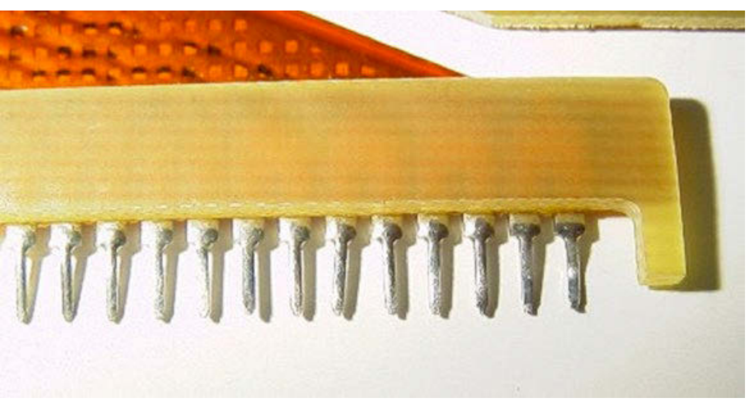


Figure 1: Solid FR-4 stiffener with locating tabs.

Thick, flexible cover coat material is used as a semi-stiffener where the flex circuit needs to retain some flexibility close to the attachment point. The slightly less flexible stiffener allows for attachment of the flex to the FR-4 PCB while providing an area of reduced flexibility, allowing for a more reliable connection without creasing the flex near the attachment point (Figure 2).

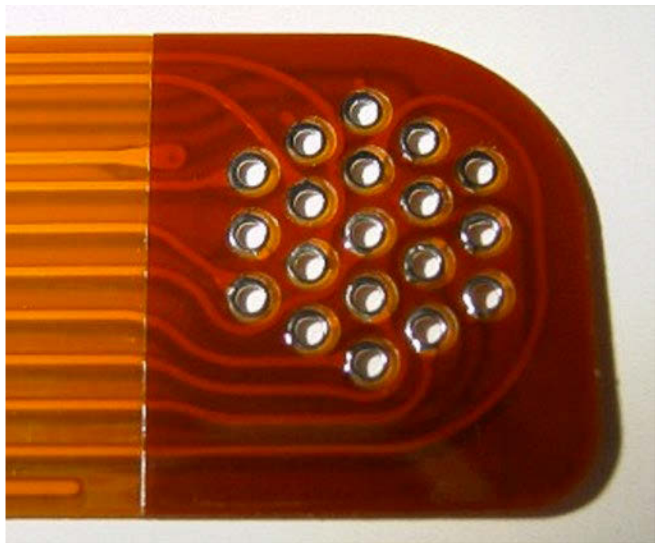


Figure 2: A 5-mil, double-sided, thick cover coat used as a stiffener on a 1-mil very flexible circuit.

Double layers of thicker cover coat stiffeners create a slightly bendable flex attachment point, such as a printer head to a fixed PCB. The cover coat material allows for some stress transition from highly bendable to rigid, reducing the chance of a crease crack in the copper, similar to a short tapered cord protector on a power tool. Flex circuitry can rip or create

opens in the copper traces if the bend radius is too small or the number of cycles is too large. A transition area from the hard mount, no flex stiffener to a fully flexible one will extend the life of a flex circuit. The viscoelasticity of many 3M™ adhesives and tapes improves resistance to vibration fatigue by imparting flexibility to a joint or bonded area.

Many modern flex ZIP FFC connectors use a self-adhesive tape wrap or a solid mount with screws, which then slip into a connector soldered to the rigid PCB.

A transition area from the hard mount, no flex stiffener to a fully flexible one will extend the life of a flex circuit.

Typically, flex stiffeners are added after the panel is laser routed or die-cut, using 3M double-sided tape, epoxy glue, or a lamination process using a glue sheet prepreg. The FR-4 stiffeners will be routed out of the desired thickness of FR-4. The adhesive glue sheet is applied to the flex and the two parts aligned, using etch marks or silkscreen marks, and pressed together. The double-sided acrylic adhesive tape will securely attach the two parts together. This method also allows for the stiffeners to overhang the flex area and provide mounting holes or points (Figure 1).

In addition to the pressure-sensitive tape, the parts can be thermally bonded with heat and pressure in a lamination press as a large panel. The typical method is to thermally bond the stiffener to the circuit with the same flexible adhesive that is used to attach the cover lays. Using high heat and pressure and gluing the parts together, this method will result in a very strong, permanent, stiffener bonding. However, using lamination as a method to glue stiffeners is limited to larger panels with a large number of stiffeners that do not extend past the flex circuit. The flex final circuit and stiffener will have to be routed, or laser cut out of the main panel.

Bonding with pressure-sensitive adhesive (PSA) tape is the most used attachment method available. The attachment is done with a PSA material, such as 3M/Tesa Tape, 3M467, or 3M9077. There are over 100 different types of PSA available from 3M alone. The specific PSA will depend on whether the flexible PCB will be subjected to a high-temperature reflow cycle. The type of adhesive used will also depend on the configuration and/or location of the stiffeners. If a stiffener extends pass the flex circuit side, in most cases, it will require a PSA attachment with a locational stiffener outline added to the copper etching data or silkscreen to allow for accurate placement. The flex and stiffener can both be accurately drilled with alignment holes, fitted over a small jig with alignment pins, and pressed together with PSA very accurately. Simply press the adhesive side down onto the flex and then peel off the poly-coated Kraft paper lining, aligning the stiffener into the pins and apply pressure to secure together.

The PSA creates a very thin, aesthetic bond line caused by glue squish-out between the flex and the stiffener. The stiffeners can be laminated by hand or in an automation setup. The adhesive sheets are easy to die-cut or CNC rout, as well as laser cut. The PSA is easy to use, has a long life, and is an industry-leading solution for attaching stiffeners. 3M Adhesive Transfer Tape 467MP is the visually clearest of the 3M Transfer Tapes and offers a neat, precise application with no mess or waste when applied to flat surfaces. It has excellent shear strength, as well as high temperature and chemical resistance, making it an ideal choice for stiffener attachment. The PSA tape features 3M high-performance acrylic adhesive 200 MP, an adhesive thickness of 2.0 mils (0.05 mm), and a poly-coated Kraft paper liner of 4.2 mils (0.11 mm).

The 3M 9077 double-sided, PSA tape is a high-temperature adhesive and release liner system that is easy to use. This is the recommended tape to be used for reflow soldering, as it survives short term exposure to

500°F/260°C for lead-free solder reflow. The 9077 tape maintains high adhesive strength in high temperatures and is excellent for heat-intensive processing, as well as in high-temperature attachments to heat sinks. It is ideal for flexible printed circuit attachments to clean metal surfaces with excellent holding power and low outgassing. 3M 9077 PST features a 2-mil 3M ultra-high-temperature acrylic adhesive 100 HT and a 3.6-mil (0.05-mm) clear, heat-resistant, non-woven liner that adds stability for die-cutting and converting. The long term temperature rating is 300°F (150°C) and suitable for automotive under the hood.

Aluminum is also used as a stiffener with an insulator cover coat strip. This allows for hard mounting to a flat surface other than a PCB. In some applications, a thermally-conductive material and aluminum or copper heat-conductive laminate can be used to manage heat while providing a hard mounting point for the flex circuit. FLEX007

John Talbot is president of Tramonto Circuits. To read past columns or contact Talbot, click here.

Foresight Completes Development of Automatic Calibration Software

Foresight Autonomous Holdings Ltd., an innovator in automotive vision systems, announced that it has completed the development of a commercial version of its groundbreaking automatic calibration software. In addition, the company submitted a patent application to the U.S. Patent and Trademark Office, pertaining to the company's innovations in the field of automotive sensor calibration.

Continuous sensor calibration is essential for creating accurate stereoscopic 3D perception required for safe and robust automotive stereo vision systems. Miscalibration occurs when external factors change the position of the sensors with respect to each other. A miscalibrated system may lead to inaccurate perception of the driving environment, affect the decision-making mechanism of the vehicle and risk passenger lives. Foresight's revolutionary innovation allows for automatic calibration between vision systems that are composed of multiple sensors, such as thermal infrared and visible-light cameras.

The company's groundbreaking software solution is designed to ensure that the sensors remain calibrated regardless of their configuration or position on a car. This will allow vehicle manufacturers flexible placement of sensors, whether on a rigid base or as separate units, while ensuring accurate perception and improving the sensors' detection capabilities.

Photo illustration: Pixabay

"Completing development of the commercial version of our proprietary automatic calibration software is an important milestone for the company, and will allow us to offer this software as a standalone product," said Haim Siboni, Foresight's CEO.

Foresight submitted two additional patent applications pertaining to multiple-sensor camera systems. The first allows repetitive and robust calibration and optical testing for vision systems composed of both visible light and thermal (infrared) cameras to ensure sensor accuracy. The second patent application enables real time assessment of the quality of information coming from each sensor set, allowing smart sensor fusion capabilities and dramatically reducing the required computational resources of the system.

(Source: Business Wire)

Thermal Management: Electronic Technology's Rodney Dangerfield

Flexible Thinking

by Joe Fjelstad, VERDANT ELECTRONICS

"I tell ya, I don't get no respect," was an opening line made famous by one of the funniest comedians of the last century, Rodney Dangerfield. And while decidedly not funny in the world of electronics, thermal engineering has, unfortunately, often been treated with less respect than it deserved. Dealing with the heat generated by electronics was often not given full consideration until after the design was completed and prototyped, and the problem manifests as a failure.

It's a simple fact that where there are electrons flowing (superconductors aside), there is heat. "How much heat?" is the salient question, as well as, "Will it be a problem?" The next question is how to deal with it. To the first point, heat in electronics is almost always a problem. The reason is that there is an inverse relationship between heat exposure and the reliability of electronic devices. Integrated circuit transistors are vulnerable to failure due to diffusion of metals through insulators causing shorts. In short form, the higher the heat, the lower the reliability. Thus, keeping devices cool is a vital objective.

There is another reason to keep things cool, however, which is to mitigate the mechanical strain that is manifested when devices having vastly different coefficients of thermal expansion (CTE) are intimately joined, such as a BGA soldered to a PCB. It is a well-known fact that solder joint failure is a leading cause of assembly failure.

There used to be a saying employed by thermal engineers that helped succinctly frame both the challenge and the solution. "It all goes back to air," and that has remained true since it was first observed and uttered, perhaps as early as the first vacuum tube amplifier. The challenge that has remained ever since is how to get the heat generated by electronics "back to air."

There are multiple ways that heat can be managed. At the earliest steps, the choice of technology is important. To provide some perspective, the world's first electronic computer, the ENIAC, had some 30 separate computing units

plus a power supply. The system weighed some 60,000 pounds, was 100' x 10' x 3', and contained roughly 19,000 vacuum tubes; 1,500 relays; hundreds of thousands of resistors, capacitors, and inductors; and required 500,000 hand-soldered interconnections. Its power consumption was about 200 kilowatts. The smartphones we carry in our pockets are several orders of magnitude both smaller and more powerful than the ENIAC, but use a fraction of the energy. Transistors are much more efficient; however, the energy density of the processor chip in watts per square millimeter is still arguably many times greater. It's all a matter of perspective.

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Both computers require cooling to perform efficiently. The ENIAC employed a forced-air cooling system to deal with the massive amount of heat generated by the tubes. Those who remember cathode ray televisions will likely remember just how warm the area around the TV was.

When it comes to managing heat, there are only three fundamental ways: conduction, convection, and radiation, as well as a number of ways to augment them. Of these, conduction is arguably the easiest, fastest, and most efficient, but conduction needs a thermal sink to further remove heat from the conduction source to keep it cool, and that is convection—the means by which the heat is transferred to air. Radiation is the least efficient (it's also the way the Earth attempts to rid itself of excess heat at night as the Earth rotates and at least part of the reason global warming is a problem), but for electronics, all three methods can be and often are combined to keep things cool.

To help deal with the heat, thermal engineers have developed many clever solutions over the years to protect electronics from overheating. This often happens in concert with system designers. One such solution is what has been called a "stepped phased system protection" protocol. The first level of thermal protection is passive thermal protection. These include heat sinks, heat spreaders, heat pipes, and the like to remove heat directly through conduction aided by convection from the device (normally a CPU). If things get too hot for the passive and semi-passive solutions, a fan is often engaged to assist heat removal at the first thermal threshold. Additional sophistication and the use of software is the next solution, where the CPU/system clock speed is reduced to reduce energy generation when a threshold is reached. This is followed by an overheat condition warning to the user. If that fails, to get a response, the system will automatically shut down.

There have been many solutions to the thermal problem as watt densities increase. It is recommended that the designers familiarize themselves with both the solutions and to not ignore the importance of thermal interface materials (TIM), which are vital to assuring that the first thermal pathway is a good one.

Thermal challenges are unlikely to go away so long as electronics persist. Photonics have been suggested as one prospective solution. There have also been suggestions that biologic computers using neural networks assembled by DNA are in the future by some futurists, but—come to think of it—isn't that what humans are?

Stay cool—and give all those thermal management engineers some well-deserved respect. **FLEX007**

Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185 patents issued or pending. To read past columns or contact Fjelstad, click here. Download your free copy of Fjelstad's book *Flexible Circuit Technology, 4th Edition*, and watch the micro webinar series on flexible circuit technology.

Documenting Your Flex Circuit Design

Flex007 Article by Tony Plemel
FLEXIBLE CIRCUIT TECHNOLOGIES

As a flex circuit applications engineer, when I receive an RFQ, the first thing I do is look at the customer's data and review their manufacturing notes. Quite often, I find notes that supersede IPC specifications in manufacturing documents, as customers often believe these added notes and associated specifications will make the circuit more robust. However, these non-standard IPC manufacturing specifications/notes can wreak havoc on the manufacturing process and can actually lead to a less robust circuit.

For example, a customer will sometimes specify additional copper plating, believing it will result in a more reliable circuit. In reality, that type of requirement can make the circuit less reliable, more difficult to manufacture, and more expensive. When manufacturing yields go down, the price goes up!

In taking a deeper dive into manufacturing notes and the potential issues that they can create, let's use a three-layer multilayer flexible circuit as an example. The first note on a manufacturing print is usually "Manufacture to IPC-6013, Class 2, Type 3." This note should always be included; I cannot stress that enough!

Unfortunately, in the continued review of the documentation, I often find one or more additional conflicting notes further down in the manufacturing notes that overrule IPC-6013 specifications.

Copper average[2,3]	Class 1	Class 2	Class 3
Type 3 and Type 4 except as noted	25 µm [984 µin]	25 µm [984 µin]	25 µm [984 µin]

Table 1: IPC-6013 copper plating requirements.

Copper Plating

One example would be "Minimum copper plating shall be 0.0015"." This note supersedes the IPC-6013 specification in Table 1. PCB designers who are not well-versed in flex circuit manufacturing may not know that exceeding IPC-6013 of 984 µin (0.000984") can cause the circuit to be less reliable and possibly cause problems later in the manufacturing process. Having a specified requirement this large (0.000516" thicker) will require the plating line at the factory to plate more than 0.0015" to ensure the minimum plating is 0.0015" thick.

Also, if there are impedance-controlled traces on the outer layers, we then need POP plating (pads only or button plating). Plating thicker than IPC-6013 recommendations can cause the POP pads to poke through the dry film resist during the roll or vacuum lamination, imaging, and developing process. The exposed bump will then result in pitted etching on the surface of the POP ring, causing rejected parts.

Additionally, this excess plating thickness will then require a thicker cover coat adhesive layer to compensate for the thicker plated bump. The extra adhesive thickness needed to encapsulate the bump will result in more adhesive flow around the pad, causing annular ring issues and also making the circuit more rigid.

On a Type 3 (three layers or more) circuit with 1/2-oz. copper plated to standard IPC recommended panel plating or POP plating, the cover-lay typically only requires 0.002"' of adhesive. However, with the 0.0015" minimum plating thicknesses, the cover-lay may need 0.003" adhesive. Additionally, when

ENIG	Electroless Nickel – Rigid	3.0 – 6.0 µm [118 – 236 µin]	IPC-4552 J-STD-003	b4
	Electroless Nickel – Flex	1.27 – 6.0 µm [50 – 236 µin]		
	Immersion Gold	0.04 – 0.1 µm [1.58 – 3.94 µin][5,9]		b4

Table 2: IPC-6013 ENIG requirements.

laminating FR-4 stiffeners to the flex, the high-pressure lamination process can put undue stress on the plated through-hole barrel, subsequently making the circuit less reliable.

ENIG Final Finish

Another manufacturing note often seen is a customer's own specified ENIG thickness that does not align with IPC-6013 (or IPC-4552) requirements (Table 2). This superseding note can also cause a price increase.

The reason to try to always use the IPC ENIG thicknesses is that the factory sets up their ENIG line to adhere to the IPC ENIG standard. If the customer specifies a different plating parameter that does not meet IPC-6013 specifications, the factory must allow all normal products to completely clear the plating line, then modify the plating line and separately process the non-standard product. The plating line is then changed back to the normal parameters to continue plating the rest of the panels to the standard IPC ENIG parameters. Changing the normally accepted plating specifications unless specifically needed only creates a higher-cost circuit board.

Material Specifications

It is advised not to place detailed material brands on the print unless the customer has specific reasons to do so. Please allow IPC specifications to determine the material selection. For example, it is common for a customer to specify Dupont™ AP8515R (1/2-oz. copper x 1-mil polyimide x 1/2-oz. copper) on the manufacturing print. Simply specifying 1/2-oz. copper x 1-mil polyimide x 1/2-oz. copper on the print, and/or per IPC-4204/11 material is sufficient. This eliminates redundancy, as well as reduces the chances of an error while trying to decipher the manufacturing notes. By calling out materials by name brands, you may have increased the cost of your circuit by 10–20% with no real reason to do so!

Print Templates

Another suggestion is to create print templates and use a fresh template when designing new circuits. If you should have questions on how to lay out a good print template, contact your flex provider and allow them to guide you.

When working with customers, I recommend that they never copy and paste from previous projects, as this leads to copying notes that simply do not pertain to the current project. Using print templates and filling them in on a per-project basis will help eliminate costly mistakes.

If in doubt as to the acceptability of your manufacturing notes, ask your flex engineer to help redline your prints so they will be acceptable to any flex manufacturer. This will eliminate confusing deviations or redlines next time the circuit is built or quoted.

Conclusion

To summarize, utilize IPC-6013 for standard specifications as this allows processes and yields to perform at their best. Keep notes standard and have print templates to work from, and you likely will see improved results related to attaining the products that you desire and an improved cost. In my next article, I will get into details related to certain requirement-driven occasions where one might choose to supersede the IPC-6013 specification, but trust most often in following IPC-6013, and you will be served well! **FLEX007**

Tony Plemel is a senior applications engineer with Flexible Circuit Technologies.

Flex007 Highlights

Flex Workshop Update With Joe Fjelstad and Anaya Vardya ▶

When Anaya Vardya, president and CEO of American Standard Circuits, heard that Joe Fjelstad, founder and CEO of Verdant Electronics, was releasing an updated version of his flexible circuit technology workshop, he knew ASC had to be a sponsor. We recently asked Joe and Anaya to discuss the flexible circuit technology workshop, as well as the ongoing need for flex and rigid-flex training—even in the time of COVID-19—as the demand for flex continues to rise.

All Flex Conducts Successful Study on High Wattage Heaters for Medical Instruments ▶

All Flex has tested its high watt heaters up to 115 watts per square inch, which is 50% higher watt density compared to the next highest available. These test results showed that etched foiled heaters stood up against the demands of molecular diagnostic/DNA testing, where fast warm-up and rapid cooldown is required, with no degradation after 100,000 thermal cycles.

Murray Percival Takes a Bite Out of Board Costs: Partners With Board Shark ▶

The Murray Percival Company, a supplier to the Midwest's electronics industry, announced a new partnership with Board Shark, a PCB solution provider. The Board Shark factories offer expertise in different niches of PCB and flex circuit manufacturing.

Flex Talk: Additive and Subtractive—When Opposites Attract ▶

Market dynamics in the electronics industry are quickly changing. Some solutions add considerable cost to the PCB and often introduce reliability and yield concerns. Tara Dunn explains an alternative that has been installed in three U.S.-based PCB fabrication facilities: the A-SAP™ process, which is Averatek's semi-additive process.

EPTE Newsletter: Is the Global Electronics Industry Improving? ▶

While composing this column, the end of July is quickly approaching, and electronic companies can't forecast business trends with this uncertainty in the market. Why the choppy market? Dominique Numakura explains.

InnovationLab, Heidelberg Collaborate on Industrial Production of Printed and Organic Sensors ▶

InnovationLab, an expert in printed and organic electronics, announced a partnership with Heidelberger Druckmaschinen AG (Heidelberg), a world market leader in the manufacturing of printing presses, that will result in the mass production of inexpensive printed and organic sensors, freeing companies to design and produce low-cost customized pressure sensors on an industrial scale for the first time.

Joe Fjelstad Updates His Online Flex Workshop ▶

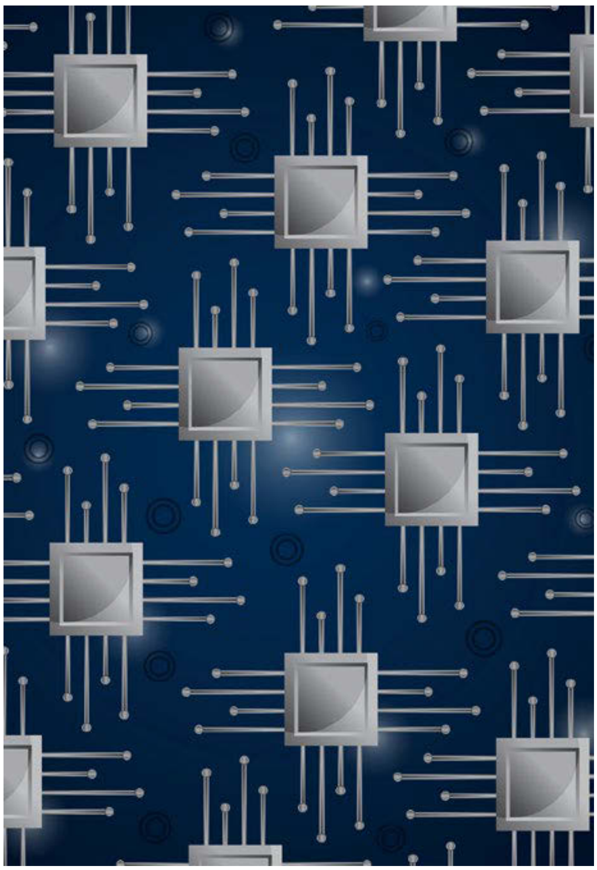
About 10 years ago, I-Connect007 helped Joe Fjelstad produce an online workshop on flex technology based largely on his book Flexible Circuit Technology. Now, Joe is updating his flex workshop to make it current with today's flex technologies and processes. In this interview, Joe explains what attendees will learn in the "new and improved" seminar, as well as his drive to continue sharing his wealth of knowledge with the young flex technologists of today.

Next-Generation Flex Circuits: Textile Base Flex

EPTE Newsletter

by Dominique K. Numakura, DKN Research LLC

The COVID-19 pandemic remains active throughout the world as Phase 3 clinical trials are underway for many pharmaceutical companies. Large R&D investments from Big Pharma could bear fruit in the coming months as the race for a vaccine continues. Several equipment manufacturers are developing medical devices for both diagnosis and treatment to fight COVID-19. This market could be huge in the near future.



Medical electronics is already a big segment of the industry. New medical devices will require different performance standards than typical consumer electronics, such as smartphones, especially when attached to your body. These new wearable electronic devices require comfort as well as reliability. The device's base material must be elastic and permeable to allow air and moisture to pass through it while addressing allergies and skin irritations.

Traditional flexible dielectric materials, such as polyimide and PET films, are not suitable to satisfy these medical requirements. Traditional electronics devices focus on performance from stable substrates, and characteristically have high dimensional stability, no permeability, low moisture absorption, and high insulation resistance. This will not work for most of the wearable electronic medical devices, so where do we go from here?

An assortment of textiles was developed over the years purely out of necessity (the mother of all inventions). There are many fibers that are stretchable and permeable, and more than one could be suitable to use in wearable medical devices.

Creating electronic circuits on fabric substrates is not easy. The subtractive processes in manufacturing use wet chemicals. This causes an adverse reaction with textiles, so a dry process is needed of generating circuits on the textile substrates. I am experienced with two types of dry processes: a die stamping process, and screen-printable thick-film circuits.

The die-stamping process uses a specially formed punching die to cut the copper foil with glue and bond the circuits onto textile substrates—a completely dry process. (Feel free to reach out to me for details on this technology).

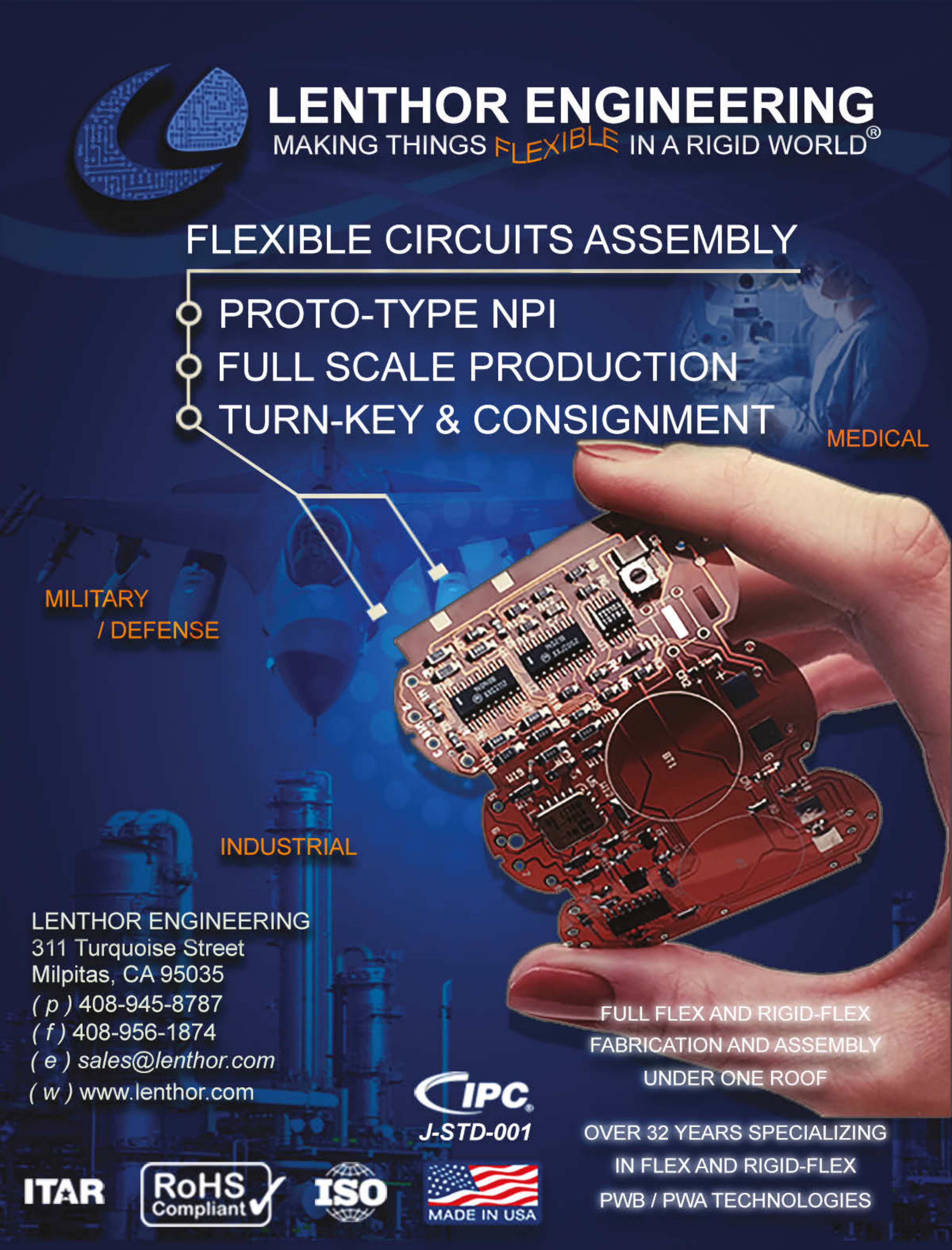

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Figure 1: An example of a pressure sensor array.

The second dry-processing technique uses screen-printable thick film circuits in the manufacturing process. The process is very simple. Conductive inks, such as silver and carbon, are screen-printed on a textile substrate and baked. It is not capable to generate fine lines with high conductivity, but it can create stable traces on the fabric's rough surface using appropriate screen masks. Double-sided and multilayer circuits can be created by repeating the printing processes, and large circuits up to 2x3 meters are available.

Silver and carbon ink are screen-printed to form a pressure sensor array on cotton sheets. The sensor array detects weight distribution continuously while the patient is lying down. An example of this application is shown in Figure 1. The technology is fairly new but used in many applications in the medical and healthcare industries. The technology curve and market upswing will be V-shaped in the near future. **FLEX007**

Dominique K. Numakura is the managing director of DKN Research LLC. To read past columns or contact Numakura, click here.

Kneron Boosts On-Device Edge AI Computing Performance With Cadence Tensilica IP

Cadence Design Systems announced that Kneron, a leading provider of on-device edge AI solutions, has integrated the Cadence Tensilica Vision P6 DSP in its next-generation KL720, a 1.4TOPS AI system-on-chip (SoC) targeted for AI of things (AIoT), smart home, smart surveillance, security, robotics and industrial control applications. Demonstrating its continued leadership in the low-power, high-performance vision DSP market, the Tensilica Vision P6 DSP provides Kneron with up to 2X faster performance for computer vision and neural network processing compared to its prior-generation SoC, while delivering the power efficiency crucial for edge AI.

In designing the KL720, Kneron prioritized design flexibility and configurability for its customers, promoting seamless AI development and deployment when using the new platform.

"Removing hurdles and making AI algorithm deployment on our platform easy is key for us and our customers' success as our mission is to enable AI everywhere, for everyone," said Albert Liu, founder and CEO of Kneron. "The Tensilica Vision P6 DSP packs a lot of compute capacity to tackle the latest AI challenges. Additionally, Cadence's electronic design automation full flow along with on-site support helped tremendously to speed up IP integration and reduce time to market."

(Source: Business Wire)

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1 Just Ask Happy: The Exclusive Compilation ▶


Happy Holden

We asked for you to send in your questions for Happy Holden, and you took us up on it! We loved them so much, and we know that you did too, so we've compiled all 21 questions and answers into one document for easy reference.

2 Altium Posts Positive Financial Growth in Fiscal Year Report ▶

Electronic design software company Altium Limited has announced its results for the full year ended on June 30, 2020. Altium achieved revenue growth of 10% to US$189 million with solid performances in all core business units and key regions. Profit before tax grew by 12% to US$65 million USD. The company delivered an EBITDA margin of 40.0% for the full year.

3 Just Ask Joe: Standardized Grid Designs ▶


Joe Fjelstad

First, we asked you to send in your questions for Happy Holden. Now, it's Joe Fjelstad's turn! Inventor, columnist, instructor, and founder of Verdant Electronics, Joe has been involved with rigid PCBs and flexible circuits for decades, and he's ready to share some of his knowledge with our readers. We hope you enjoy "Just Ask Joe."

4 Beyond Design: The Wavelength of Electromagnetic Energy ▶


Barry Olney

The speed of light is the one universal physical constant that we are yet to break. Barry Olney looks at how to simply measure the speed of light and how the wavelength of electromagnetic energy relates to the multilayer PCB.

5 Quiet Power: Be Aware of Default Values in Circuit Simulators ▶


Istvan Novak

Simulators are very convenient for getting quick answers without lengthy, expensive, and time-consuming measurements. Istvan Novak explains how, sometimes, you can be surprised if you forget about the numerical limits and the limitations imposed by internal default values.

6 Elementary, Mr. Watson: How to Ruin Your PCB Design in 4 Easy Steps ▶


John Watson

John Watson has seen firsthand how quickly PCB designs can “go off the rails” by not following a few simple principles. In this column, he looks at four practices that can easily ruin your PCB design.

7 The Pros and Cons of Working Remotely ▶


Patrick Crawford

Andy Shaughnessy asked Patrick Crawford if IPC had any insight into how the “new normal” of working from home has impacted their members. Here is what the IPC technical staff had to say about the advantages and disadvantages of working remotely, as well as working with IPC volunteers who are new to working from the dining room table.

8 Time to Market: 8 Ways to Know Your Customer Better ▶


Imran Valiani

Now is the time to go the extra mile in getting to know your customers, what they need, and how to help them solve their problems and challenges. Imran Valiani shares eight ways to know your customer better.

9 Design Circuit: An Update on the Italian IPC Design Chapter ▶


Pietro Vergine

Patrick Crawford had the opportunity to speak with Pietro Vergine, the chair of the leadership team for the new Italian IPC Design Chapter. He spoke with Pietro about the design space in Italy, as well as his plans for the Italian IPC Design Chapter.

10 Fresh PCB Concepts: How Do You Calculate Finished Copper? ▶


Ruben Contreras

How do you calculate finished copper on a PCB? This may sound simple, but Ruben Contreras has seen copper thickness called out either on the drawing or the specification, which can lead to additional EQs and, in some cases, additional costs. In this column, he explains the unintentional results that can come from misunderstanding what was requested.

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Career Opportunities

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- To demonstrate our products to existing and potential customers and to assist them in selecting the copper treatments best suited for their needs
- To provide technical assistance to customers in case of claims, technical assistance, new product development
- To promote our products to OEMs
- To attend fairs (IPC, DesignCon,...), technical conferences (IPC 4562A,...) and customer presentations

THE PROFILE:

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- Implement process and perform failure mode analysis to establish correct operating conditions
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- Monitor process operation on a daily basis to ensure consistency
- Perform failure and root cause analysis when product/process problems occur
- Perform chemical analyses on processes when required

Knowledge and Skills:

- Ability to read, write and communicate in English necessary to perform the job
- Knowledge and application of statistical techniques for process control
- Knowledge and application of failure mode effect analysis techniques as applied to process improvement and process development
- Ability to lift 25 pounds
- Will be exposed to hazardous waste while performing daily job duties
- Will undergo chemical handling training prior to start and will actively participate in ongoing hazardous waste and chemical handling training

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Sales Account Manager

Sales Account Management at Lenthor Engineering is a direct sales position responsible for creating and growing a base of customers that purchase flexible and rigid flexible printed circuits. The account manager is in charge of finding customers, qualifying the customer to Lenthor Engineering and promoting Lenthor Engineering's capabilities to the customer. Leads are sometimes referred to the account manager from marketing resources including trade shows, advertising, industry referrals and website hits. Experience with military printed circuit boards (PCBs) is a definite plus.

Responsibilities

- Marketing research to identify target customers
- Identifying the person(s) responsible for purchasing flexible circuits
- Exploring the customer's needs that fit our capabilities in terms of:
  - Market and product
  - Circuit types used
  - Competitive influences
  - Philosophies and finance
  - Quoting and closing orders
  - Providing ongoing service to the customer
  - Develop long-term customer strategies to increase business

Qualifications

- 5-10 years of proven work experience
- Excellent technical skills

Salary negotiable and dependent on experience. Full range of benefits.

Lenthor Engineering, Inc. is a leader in flex and rigid-flex PWB design, fabrication and assembly with over 30 years of experience meeting and exceeding our customers' expectations.

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- Participate in the evaluation of processes, new equipment, facility improvements and procedures.
- Improve process capability, yields, costs and production volume while maintaining safety and improving quality standards.
- Work with customers in developing cost-effective production processes.
- Engage suppliers in quality improvements and process control issues as required.
- Generate process control plan for manufacturing processes, and identify opportunities for capability or process improvement.
- Participate in FMEA activities as required.
- Create detailed plans for IQ, OQ, PQ and maintain validated status as required.
- Participate in existing change control mechanisms such as ECOs and PCRs.
- Perform defect reduction analysis and activities.

Qualifications

- BS degree in engineering
- 5-10 years of proven work experience
- Excellent technical skills

Salary negotiable and dependent on experience. Full range of benefits.

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APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

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Manncorp™

SMT Field Technician
Huntingdon Valley, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:
- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:
- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
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This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.

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Professionals Seeking Employment

D.B. Management Group L.L.C. is currently working with many professionals who are seeking new positions. If any of these qualified professionals sounds like someone you would like to learn more about, contact **Dan Beaulieu** at **207-649-0879** or danbbeaulieu@aol.com. If you are a qualified professional looking for a new opportunity, contact Dan as well. Fees are 10% of candidates' first year's annual compensation. There is no fee for candidates.

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President, Company Leader, Business Builder
This professional has done it all. Built new businesses and turned around hurting businesses and made them successful. A proven record of success. This candidate is a game-changer for any company. He is seeking a full-time leadership position in a PCB or PCBA company.

General Manager PCB and PCBA
Senior manager with experience in operations and sales. He has overseen a number of successful operations in Canada. Very strong candidate and has experience in all aspects of PCB operations. He is looking for a new full-time position in Canada.

Regional Sales Manager/Business Development
Strong relationship management skills. Sales experience focused on defense-aerospace, medical, high-tech PCB sales. Specializes in technical sales. Also has experience in quality, engineering, and manufacturing of PCBs. He is looking for a fulltime position in the Southeastern U.S.

Field Application Engineer (FAE)
Has worked as a respected FAE in the U.S. for global companies. Specializes in working alongside sales teams. Large experience base within the interconnect industry. He is looking for a full-time position.

Business Development Manager
Understands all aspects of interconnect technical sales from PCB design and fabrication to assembly and all technologies from HDI microvias to flex and rigid-flex. Has also sold high-tech laminates and equipment. Proven record of sales success. He is looking for a full-time position.

CEO/President
Specializes in running multi-million dollar companies offering engineering, design, and manufacturing services. Proven leader. Supply chain manager. Expert at developing and implementing company strategy. Looking to lead a company into the future. He is looking for a full-time position.

PCB General Manager
Forty years of experience serving in all capacities, from GM to engineering manager to quality manager. Worked with both domestic and global companies. Available for turn-around or special engineering projects. He is looking for long-term project work.

Process Engineering Specialist
Strong history of new product introduction (NPI) manufacturing engineering experience: PCB/PCBA. Held numerous senior engineering management positions. Leads the industry in DFM/DFA and DFX (test) disciplines. He is looking for either a full-time position or project work.

VP Sales Global Printed Circuits
Worked with a very large, global company for a number of years. Built and managed international sales teams. Created sales strategies and communicated them to the team. One of the best sales leaders in our industry. He is looking for a full-time position.

Plant Manager
This professional has years of experience running PCBA companies. Led his companies with creative and innovative leaderships skills. Is a collaborative, hands-on leader. He is looking for a full-time position.

National Sales Manager
Seasoned professional has spent the past 20 years building and growing American sales teams for both global and domestic companies. Specializes in building and managing rep networks. He is looking for a full-time position.

Global Engineering Manager/Quality Manager
Has experience working with large, global PCB companies managing both engineering and quality staff. Very experienced in chemical controls. She is interested in working on a project-by-project basis.

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These candidates want to work remotely from their home offices and are willing to do full-time or part-time projects.

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