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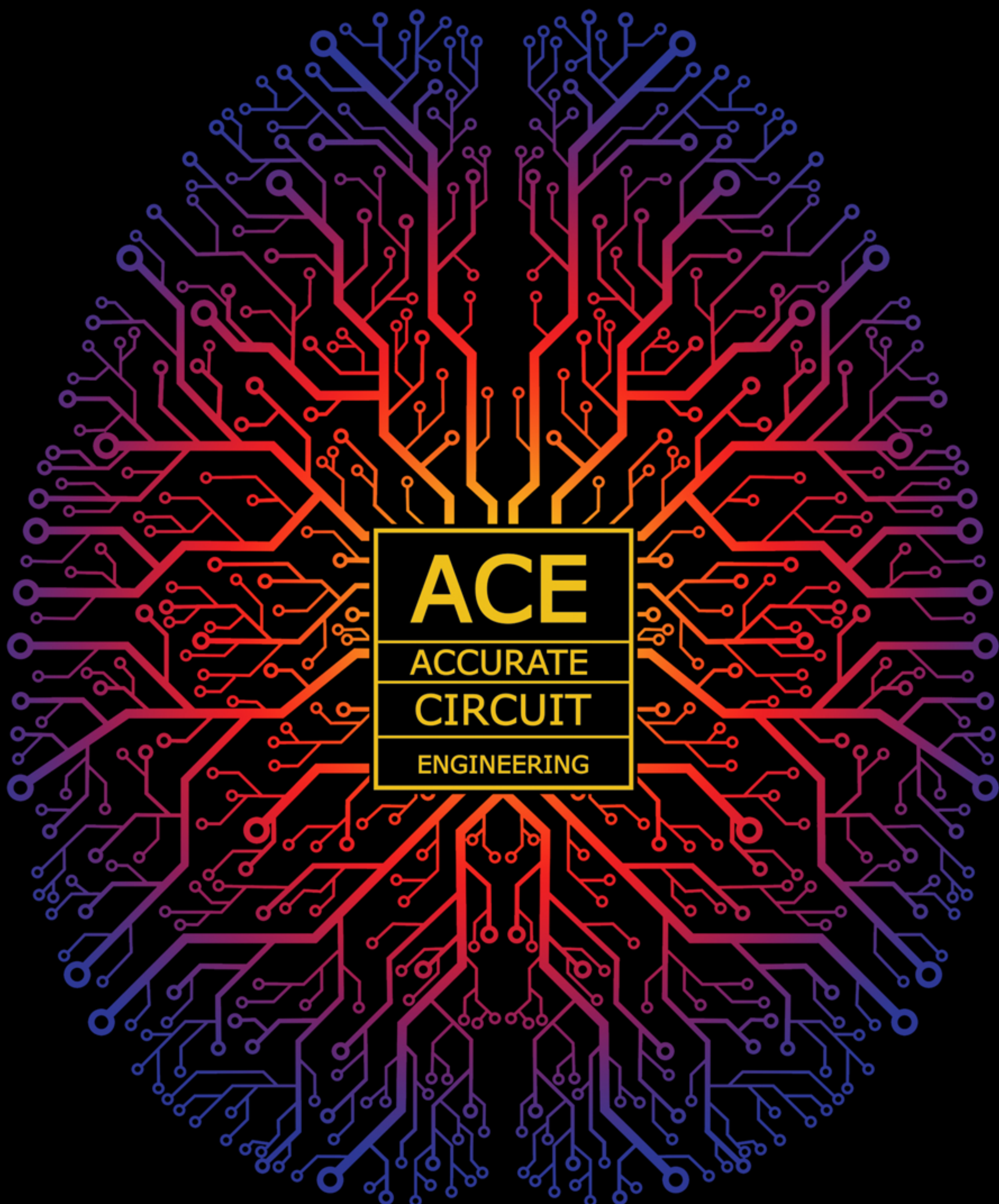
Design for Profitablity

It's easy to define profit, but it's much more difficult to define exactly what "design for profitability" (DFP) means to today's PCB designers and design engineers. How can technologists create profit in every design when the board's stakeholders are often spread out across several time zones and continents? This month, we asked our experts to weigh in on the best DFP strategies and how this can affect the entire PCB development cycle.

FEATURE INTERVIEWS:

FEATURE COLUMN:

Don't Overthink Your Prototype Builds



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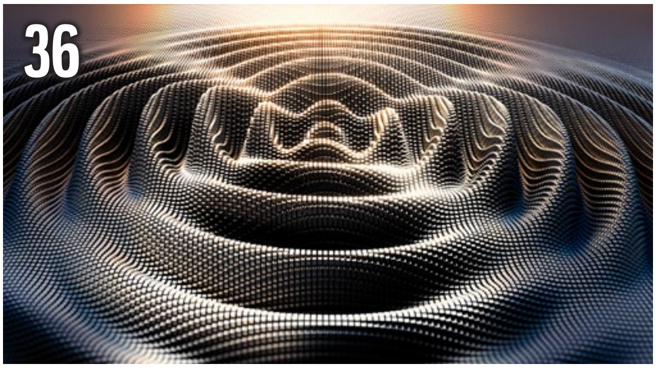

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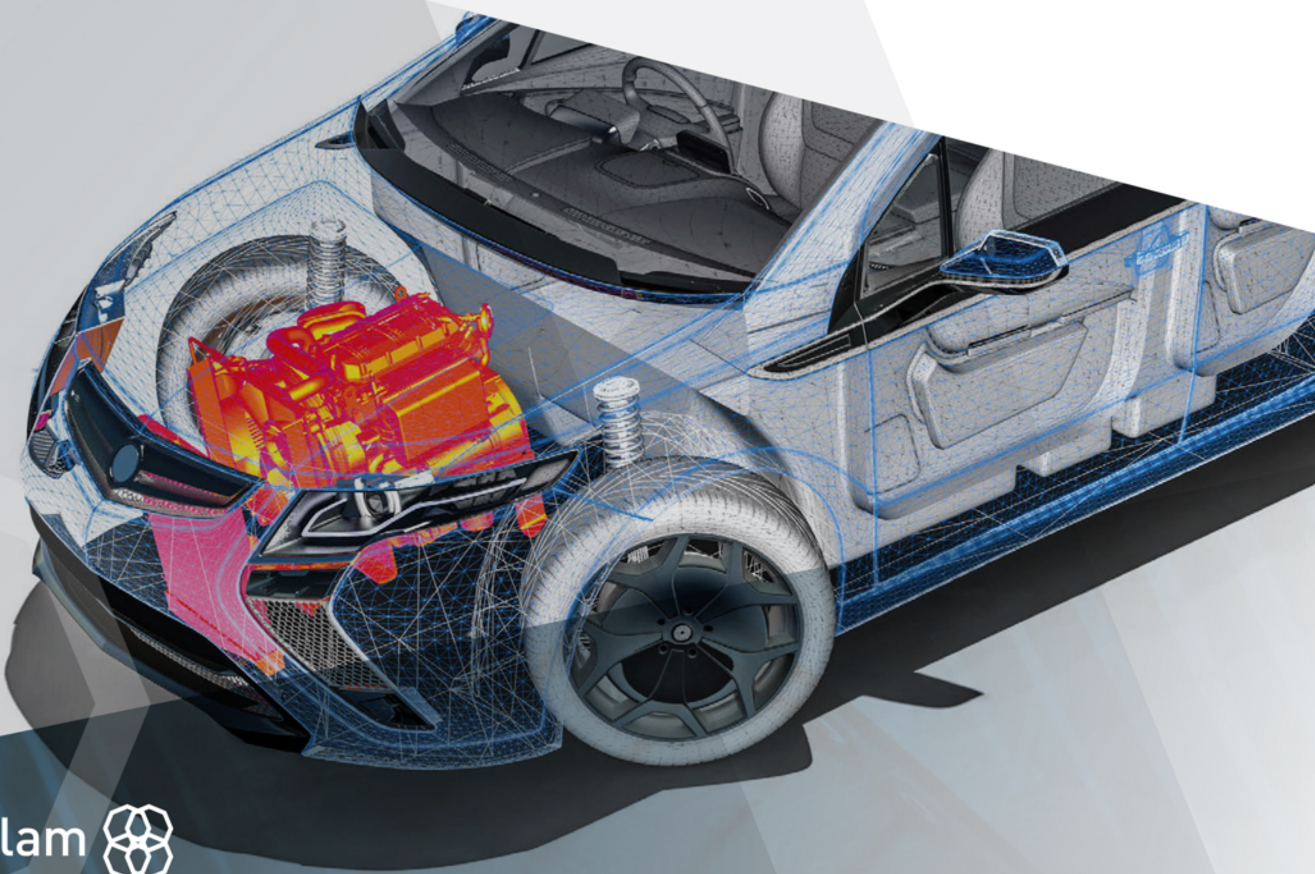

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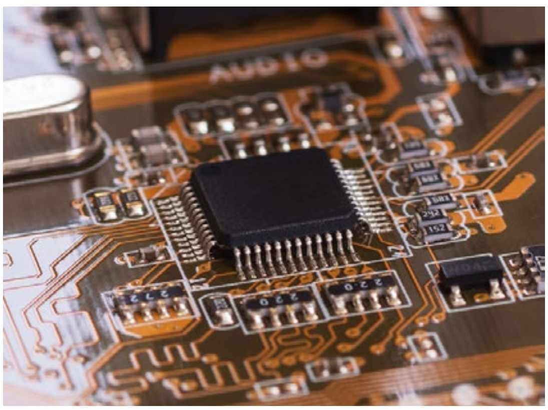
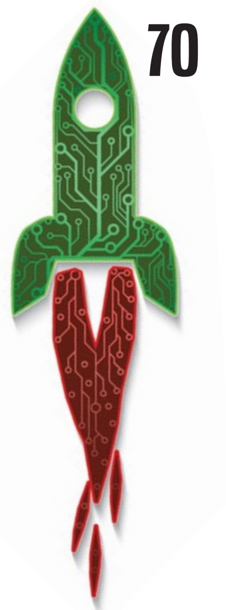
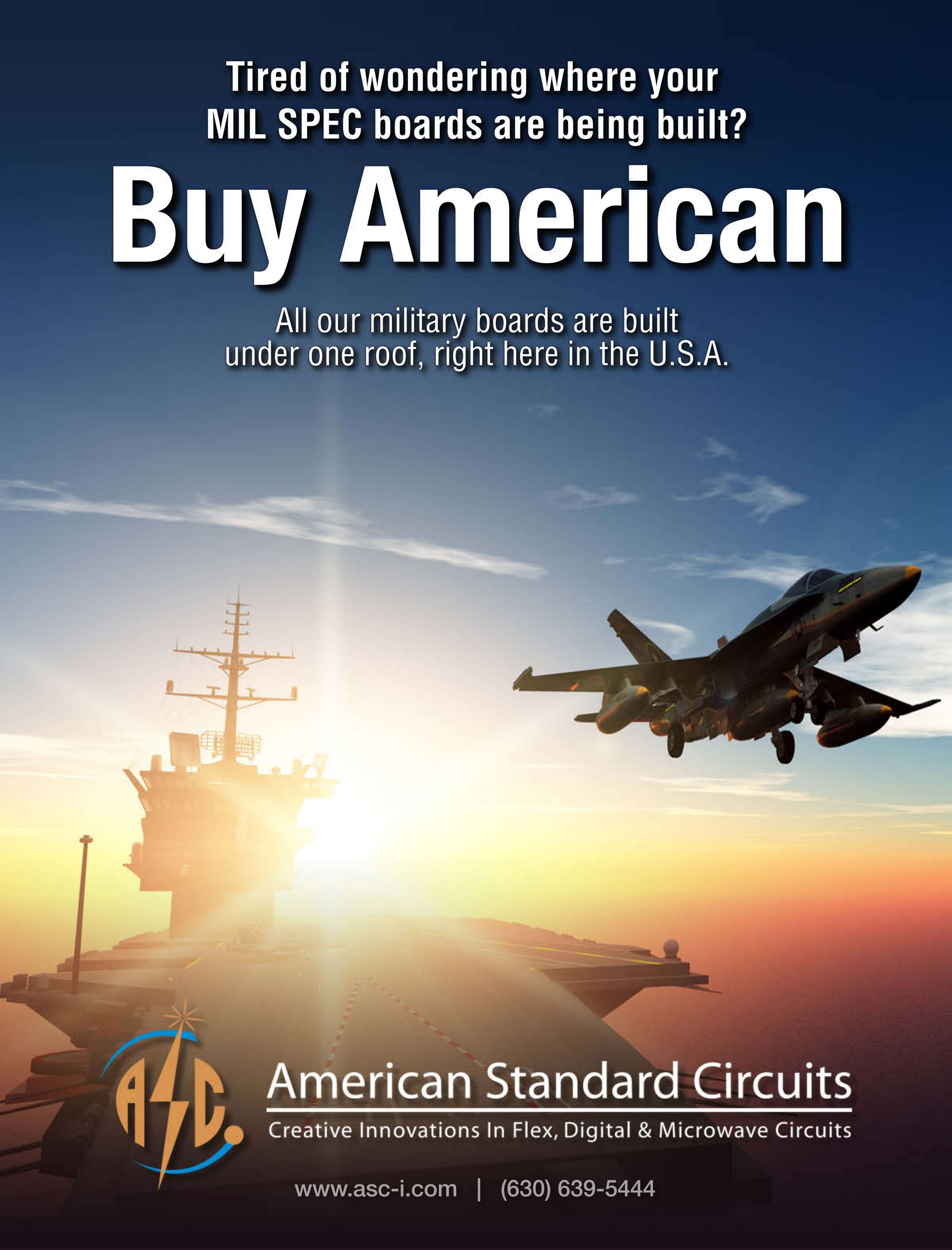
Focusing on Flex

Designing for profitability is tricky enough with traditional rigid PCBs, but because of their unique 3D attributes, flex and rigid-flex DFP can be so much more difficult than for their rigid brethren. This month, we explore a variety of cost-aware methods for designing flex and rigid-flex circuits.



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Design for Profitability Now Part of the Process

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

Merriam-Webster's online dictionary defines the word "profit" this way:

1. A valuable return: Gain.
2. The excess of returns over expenditure in a transaction or series of transactions, especially: The excess of the selling price of goods over their cost.

It's easy to define profit, but it's much more difficult to define exactly what "design for profitability" (DFP) means to today's PCB designers and design engineers. How can technologists create profit in every design when the board's stakeholders are often spread out across several time zones and continents? It's a tough concept to get your arms around. Some of you work in giant OEMs; do you have any idea how much your last design cost—man-hours, components, laminates, etc.?

When I started working on this issue, I was happy to hear that many designers were already familiar with DFP. When I first mentioned DFP to designers years ago, they'd look at me like I had two heads. After all, designers used to feel as if they were the lowest person on the totem pole, and many didn't realize the power that they wield over the profit of the PCB and, potentially, the final product. Fortunately, that has changed, for the most part.

In a recent *Design007 Magazine* survey, about two-thirds of respondents said that cost is a definite factor in their design process. Ap-

parently, most CAD managers are well aware of the designers' power to massage costs; some engineering managers believe that up to 80% of the board's cost can be determined during the design cycle. Some designers are also being tasked with making cost-aware design decisions each day. Designers—already forced into thinking like degreed engineers, often making system-level decisions—must now think like accountants as well.

This month, we asked our experts to weigh in on the best DFP strategies and how this can affect the entire PCB development cycle. We start with an interview with Al Neves of Wild River Technology, who explains why DFP is impossible without good processes, great management, and designers and engineers who continue to educate themselves, even after 30 years of experience. Next, Todd Westerhoff of Mentor, a Siemens Business, discusses how seemingly small problems can lead to increased costs and why accessible simulation tools can help designers make cost-aware decisions. Chris Banton of EMA Design Automation outlines why providing designers with the right data early on can make the difference between a profitable design and a train wreck. And Brad Griffin of Cadence Design Systems looks into how the company helps designers stay in the black by automating time-consuming tasks. Plus, we have columns from our regular contributors Barry Olney, Stephen Chavez, Alistair Little, and Bob Tise and Matt Stevenson.

In Flex007, Tara Dunn asks, "Are you unintentionally adding cost?" She explores why cost-aware design for flex and rigid-flex circuits can be so much more difficult than for their rigid brethren. Joe Fjelstad focuses on how all of the "design fors,"—such as DFM, DFA, and DFE—contribute to profitability. And we have an interview with Carey Burkett of Flexible Circuit Technologies, who discusses the company's growth from a flex maker into a company that provides assembly and box-build services. Does your company stress DFP as one of its major concerns? Let me know. Until next month, take care. **DESIGN007**

Andy Shaughnessy is managing editor of *Design007 Magazine.* He has been covering PCB design for 19 years. He can be reached by clicking here.

Robotic Research to Start Testing Fully Autonomous Unmanned Shuttles

Robotic Research has announced that it will begin testing fully autonomous low-speed shuttles that are totally unmanned in the second quarter of this year.

"Through our work with the U.S. government over the past four years, we have already demonstrated that fully autonomous trucks are a reality. We are committed to making our shuttle and bus manufacturing partners successful by accelerating state-of-the-art technologies for unmanned vehicles ahead of regulatory agencies' progress," said Alberto Lacaze, president of Robotic Research.

Robotic Research has been developing and testing unmanned, autonomous operations for a wide range of vehicles for nearly a decade. The company currently provides autonomy kits that fully automate logistics convoy trucks for the U.S. government and several of its allied nation partners. Nearly 100 trucks have already been delivered. The tests for these vehicles have included operations with no safety attendants on board, with a single operator monitoring three unmanned vehicles.

Robotic Research's AutoDrive autonomy kit is platform agnostic and can be retrofitted to vehicles of all sizes, from small, portable robots to large trucks and buses. The system provides autonomous functionality on surfaces ranging from urban-improved roads to off-road terrain, all while the vehicle is collecting and analyzing data to better enhance the future of autonomous vehicles and transportation.

(Source: Robotic Research)

Designing for Profitability: It's up to You (and Your Management)

Feature Interview by Andy Shaughnessy
I-CONNECT007

If your company is having trouble designing PCBs for profitability, where does the blame fall? Is it management's fault for having inefficient processes, or is it the fault of the designers and design engineers for not keeping up to date with their training? During DesignCon, I asked Al Neves of Wild River Technology to weigh in on this question. As he explains, you and your manager might both be to blame for inefficiencies in the design process.

Andy Shaughnessy: Al, we were just talking about designing for profitability. You mentioned that you had a few pithy thoughts on the subject.

Al Neves: Yes, and I see a trend. The work that we focus on is high-risk, extremely demanding signal integrity projects. About half of our business is service, and the other half is standard products. On the service side, somebody will come out with silicon and want a test platform. Many of the test platforms are 50–70 gigahertz right now, with very advanced embedding, complicated breakouts from their BGA, and high-density routing. The signal integrity has to be really good. One specification—IEEE P370—defines what good signal integrity is at 50 gigahertz.

A customer will say, "We have something that we'd like you to help on." Once we're at the technical credibility part of the meeting, they will say, "We need it done by next month," and we will say, "We don't do things like this by next month. It takes a long time." One of the issues with profitability is that if you want to save money, you need the project manager or an executive in that group to do their job. Your job is to manage the team in a way that you reduce risk.

If you're going to want to do 112 gigs in 2020, you should have been working on the test fixtures—the compliance, firmware, and all of that—three years ago. You can't just pull a stack-up that's suitable; you don't know what the routing is. You have to throw a team together ahead of time. Then, you have to do some test vehicles because each stack-up for that level is very demanding. I'm talking about

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112-gig test vehicles, and the test boards are difficult. You have to do things early, manage the project carefully, and engage in systematic design.

Shaughnessy: Planning ahead is a big part of it, especially for cutting-edge designs.

Neves: Absolutely. Let's say you wanted to climb Mount Everest. That's a daunting endeavor. You may go to the general area of Nepal and hang out at 7,000 feet. Next, you may want to go to base camp, which is around 14,000 feet, and you'll stay there for weeks or a month. Then, you set up a series of camps up the mountain to help mitigate your risk. You're climbing the mountain in a very systematic way, which reduces your risk, and you can acclimate to the problem. That's how advanced signal integrity is; you have to acclimate to the problem.

That's my idea of designing for profitability. If you embark on a project and don't know what you're doing, you delay the silicon in the marketplace, have a lot of people running around like crazy, and have to spend a lot. There's nothing more costly.

Shaughnessy: Without a good process, you're going to have problems.

Neves: Sure. And you know what a champion is? The person who brings you in and says, "We should do business with this company and here's why." In any type of business environment, there's a champion. The champion wants me to be the junkyard dog who communicates to the management on what the challenges are and how they need to change their process.

In my company, I manage teams of people. When things go wrong, it's easy to beat on people and point fingers. It's a difficult thing to say, "I have to figure out how to help them and what process issues contributed to this." Often, it's a process issue that relates back to the leadership of the company or the person who's defining that, and they get caught into this. A lot of the profitability issues are management and leadership issues.

Shaughnessy: You worked for some other companies before you started Wild River. Did you always want to start your own company?

Neves: One of the compelling reasons I started my own high-tech company was although I was rated as one of the company's best engineers, my interpersonal skills and likability were not rated as high as my technical skills (laughs). Again, management would say, "This project isn't going very well, and they're not motivated. You're the lead person. What are you doing about it?" I'd say, " I think we need new management. You are completely incompetent and show a lack of leadership. While we worked all weekend, you were off skiing. You make twice as much money as we do, and you're overly compensated. We don't see that you're really part of the solution, and when employees needed help for buying certain capital equipment, you weren't there. You're not doing your job."

Shaughnessy: It sounds like you wanted to tell the manager, "Sorry, but we're going to have to let you go."

Neves: For a while, I was trying to figure out why I kept getting fired and laid off because my reviews all said, "He's one of the best engineers and gets a lot of work done." One man pulled me aside and said, "You might want to think about starting your own company." I listened to him.

Shaughnessy: How long ago did you start Wild River?

Neves: We started the company nine years ago. Right now, we're viral in the amount of business that we have. We're one of two companies that consistently do first-spin 50 gigahertz, and we typically take another spin to do 70. Very few companies are constantly doing 70 gigahertz designs. Next year, we're looking at going to 90 and 100 gigahertz.

Shaughnessy: What's your technology cutoff for accepting a job?

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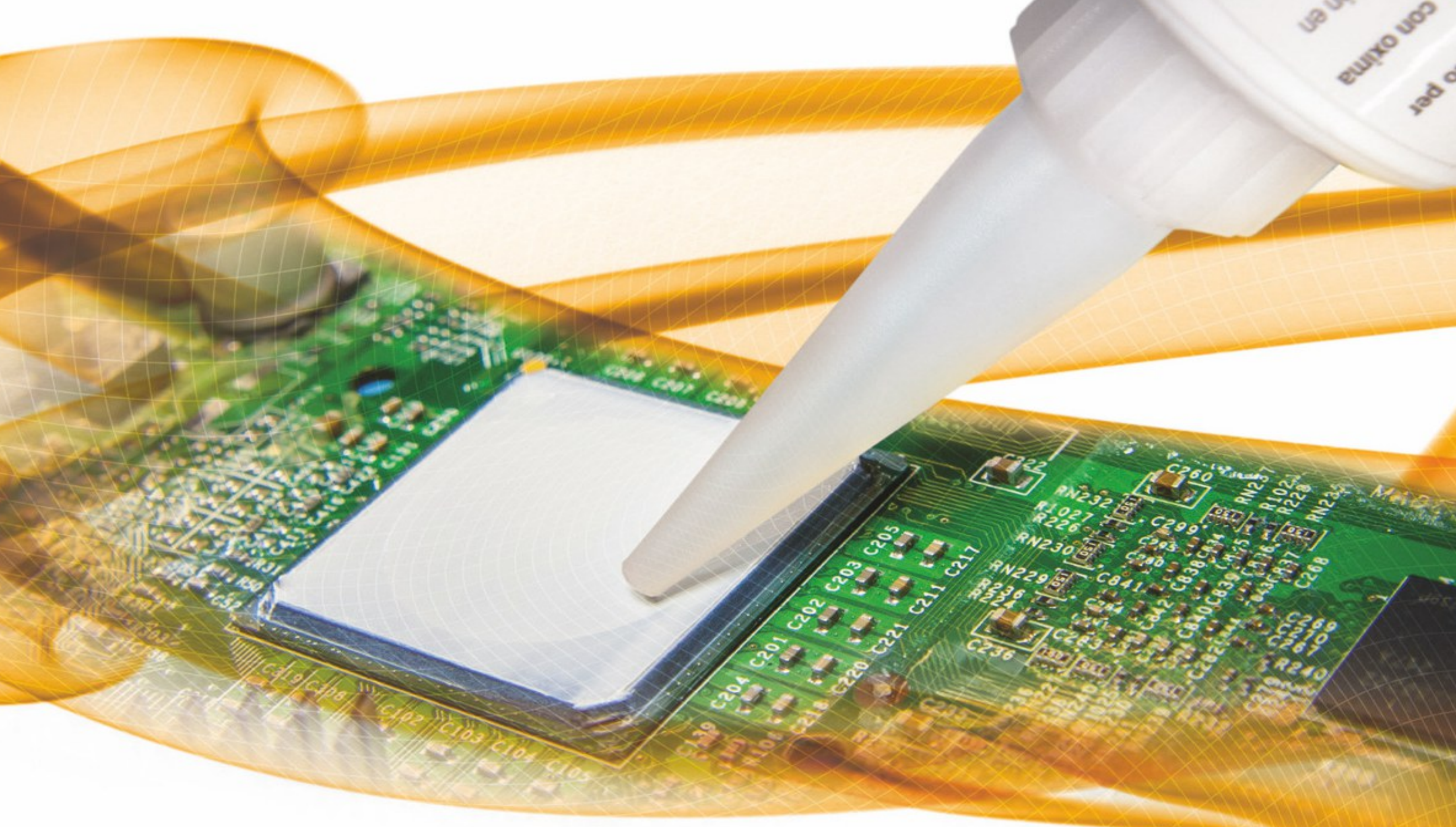

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Neves: For some of the lower-speed stuff, if we're having a soft month, we'll do that project. Today, we're pretty selective. If we do a project for a company, I tell them that I'm one of the managers, and that includes their people. If one of their engineers points fingers, usually, I chew their head off publicly. I tell everybody ahead of time, "You're responsible for everything. There's no, 'He didn't tell me.'" These are high-risk, difficult projects, and if you're not the SEAL Team 6 of SI, then excuse yourself from this project because you're just not good enough.

For example, when we do projects with companies, we use our own layout resources; we won't use that company's resources. If they insist on using their own layout, then they can find somebody else to do the work. It sounds arrogant, but if you do a bad job where you don't get the layout, it kills the momentum of the project in terms of profitability and scheduling. Imagine doing a big project in your house; let's say you're going to put a pool in. If they run into a big problem that stops the project, it kills the momentum, and your costs go way up. There's a hole in the ground. Your house is a mess. The contractor doesn't like it. You can't enjoy the pool. It sucks the momentum out of the project, and your risk goes through the roof.

Shaughnessy: What advice would you give a designer or engineer about ways that they could help make the designs were more profitable?

Neves: Let me put it in terms of music. When friends of John Coltrane went to visit him in New York, if they walked up to the house and didn't hear a sax playing, they knew he wasn't home. He was a master musician. "Giant Steps" is a gorgeous piece of music, but how much time did he invest in music? He practiced all of the time. Everything in life is about personal investments.

I've heard engineers say, "I don't get to go to DesignCon." I'll say, "What do you mean you 'don't get to go?'" They will say, "My management didn't give me permission to do that." My response is, "Did you need permission from your boss to pick your spouse, car, or house? This is your career, not your manager's career." I recommend that people tell their managers, "If you're not going to fund it, I'm going to take my vacation days and attend." For years, I paid for my own trip to DesignCon when I was a consulting contractor.

First, it's a good thing to do because it keeps you in the game. When I lived in the Bay area, I took many Berkeley classes. It's no different from playing music. You have to stay current. If an engineer in my organization said, "I come in, do my job, and leave," they would be gone. Second, insist on good project management. Take political risks. Bet your job on that. If you get laid off, so what? That's a path.

Shaughnessy: I agree. I've been laid off before. That's why I'm here.

Neves: Me too. A year later, I realized it was the best thing that happened to me. Sometimes, it's worth taking risks and jumping on opportunities. If an EDA company has a boot camp, go. I went to a day-long boot camp on power delivery and SI. I run a company. Don't you think I have better things to do than sit in a boot camp all day?

Shaughnessy: We can't place all of the blame on management or the individual when things go off the rails. Everyone has to stay on their game.

Neves: Exactly. You have to keep your skills sharp, but you have to have good management if you want to stay profitable.

Shaughnessy: Thank you for speaking with me. It's always a pleasure.

Neves: This was a good discussion. It's been great talking to you. DESIGN007

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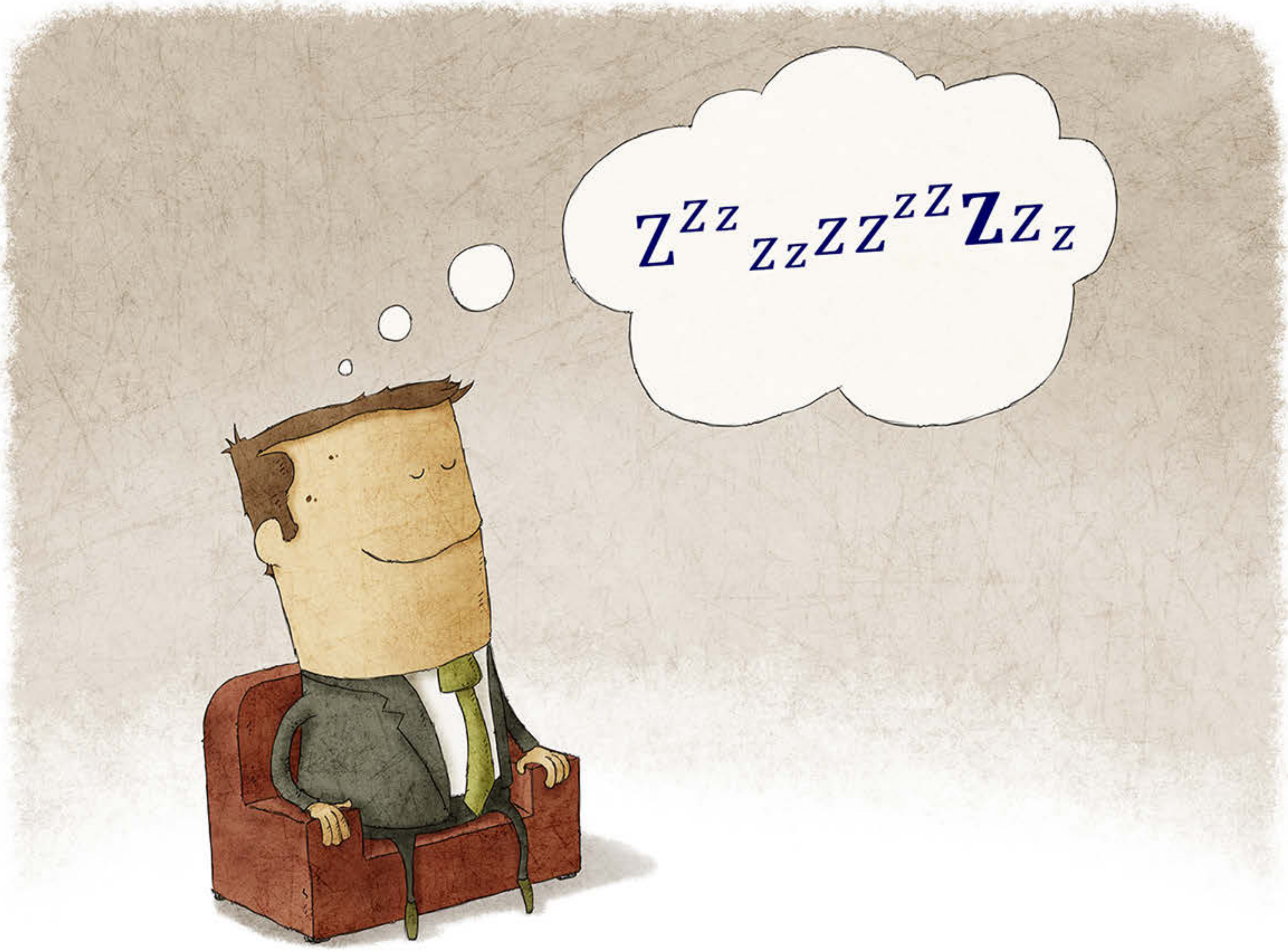

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The Seven-year Etch

Connect the Dots

by Bob Tise and Matt Stevenson, SUNSTONE CIRCUITS

As many of you probably already know, PCB etching seems like a simple task on the surface—the selective removal of material using an etching agent. However, quite a few things can go wrong during this process, such as over-etching, copper areas that detach from the board, issues with etching solution, and even accidental removal of critical components. Considered by many to be somewhat of an art form, PCB manufacturers work hard to create a better etching process (remember acid traps?). Adhering to best practice and continuous improvement is a must to help avoid issues with your finished board. In this column, we share our design tips for a better etching process.

Figure 1: New copper for plating.

Etching Process Overview

Once all of the layers are laminated together, the through-holes are drilled, the copper is plated (both electroless and electroplated), and the outer layer images are applied, it is time to physically create all of the traces and pads for a circuit board via the etching process (Figure 1).

Etching defines the distinctive routes of a PCB. It is also the process that tests the quality of a design by answering the design questions that will determine its functionality. Did you leave enough space? Are your traces wide enough?

PCB manufacture etching is a reductive process, not an additive process. The board starts with a consistent layer of copper throughout, and the etching process removes all unwanted copper. Now, if you think that sounds wasteful, don't worry; the copper removed during etching is easily captured and recycled.

Remember that we start the PCB process with a fully copper-clad panel. After coating it in a light-sensitive polymer, we project high-intensity UV through an image of the PCB design that you carefully composed. A photoresist layer covers the areas where we want to remove

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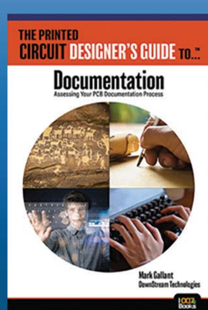

This book, written by Mark Gallant of DownStream Technologies, explains how an automated documentation solution like BluePrint-PCB® can eliminate post-processing errors and speed up time to market.

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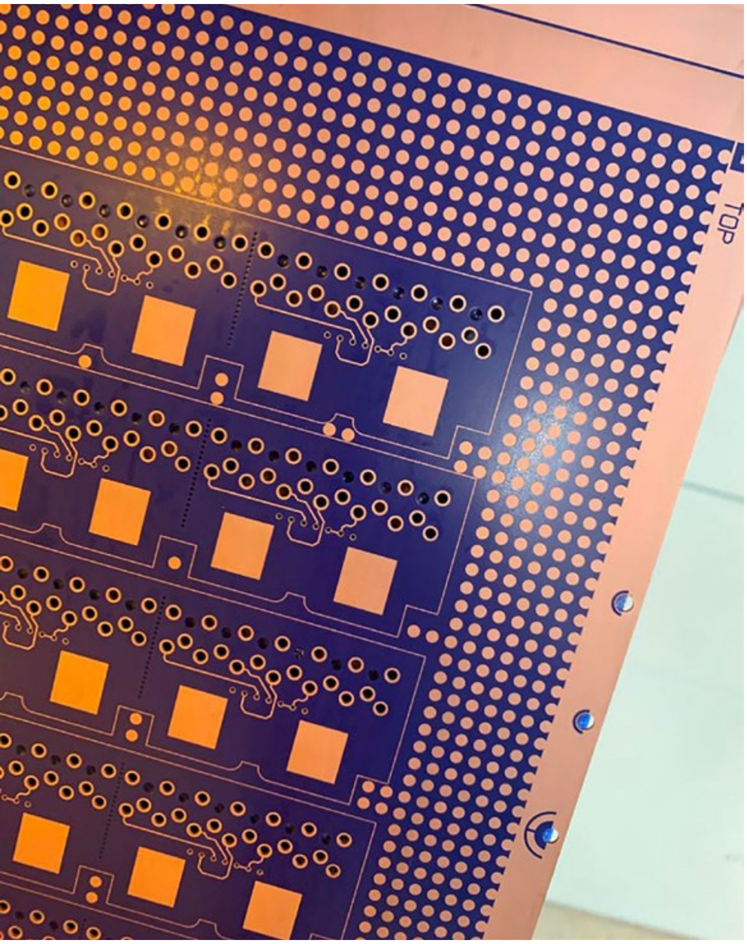

Figure 2: Before etching.

the copper. It is a photo negative of the traces you want to keep.

Before etching, copper (approximately 1–1.2 mils) is plated on exposed traces, pads, and through-holes (Figure 2). We plate about 0.3 mils of tin on top of that copper, which will protect the wanted copper from the etching chemical.

The photoresist is then chemically removed from the surface of the panel to expose the unwanted copper, and it is time for the etch. There are a few different chemicals used for etching copper, but the most common is an ammoniacal (ammonium chloride). The chemistry behind its reaction to copper in the etching process is quite complex. We won't go into the details here, but if you are interested, there are several good write-ups online to satisfy your chemistry cravings.

The equipment we use for the etching is equally complex. The board passes through carefully controlled spray chambers at a carefully controlled speed. The ammonium chloride dissolves all the copper not protected by the tin we plated on the PCB design pattern. Getting it right requires precise conveyor speed, pressure, pH, and specific gravity (Figure 3).

Even with all this precision, etching is more of an art form, especially when a design is dense or impedance-controlled. Though there are starting point settings for almost every combination of copper thickness and line width, the final tweaks needed to ensure that each job is etched properly requires an understanding of all of these variables and how they interact during the process.

On a complex PCB design, the initial etch panel is processed for first article inspection using a standard process. Critical traces and impedance measurements are then taken, and the etcher is fine-tuned to get the line widths and impedance centered in its range.

Once the panel is etched, we use a chemical process to remove the tin protecting the desired copper. The result of this process is generally a fully electrically functional PCB. Other

Figure 3: Etch machine.

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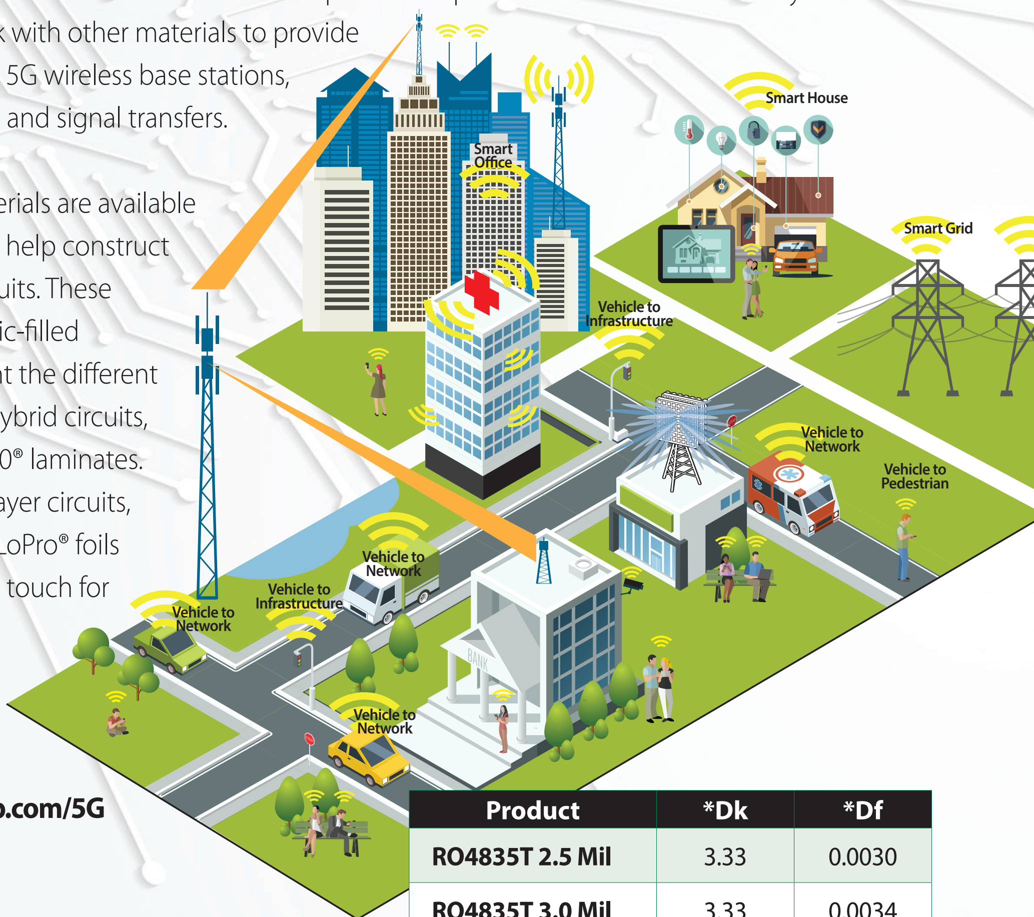

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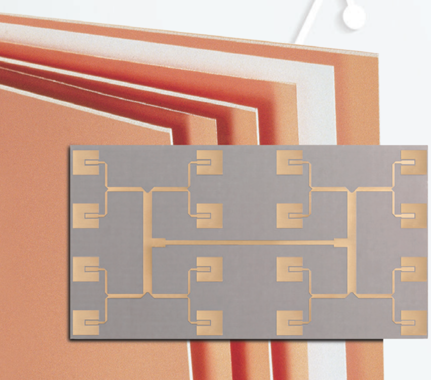

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steps need to be taken to protect the copper at assembly and prevent oxidation, but all of the nets should be defined and operational at this point. We have etched our way to a functional electrical part!

Design Tips for a Better Etching Process

As with the copper plating portion of manufacturing, some design decisions can have an impact on the manufacturability of the PCB at the etch process.

Etching is an exercise in getting fresh etchant chemistry in contact with the copper and sweeping away the byproducts as quickly as possible. Isolating critical traces on your design without much copper around it can lead to over-etching (i.e., etching more than the traces that are surrounded by copper) of these traces.

Critical traces embedded in copper pour with limited space can have the opposite problem. Replenishing the etchant solution becomes more challenging. These traces can exhibit mild under-etching.

For every half-ounce of copper, a good design has 8–10 mils of space between the trace and the embedded plane. Adding copper thieving around isolated traces helps to maintain the intent of the trace and provides a bit more space, keeping all of the features etched close to their nominal values. **DESIGN007**

Bob Tise is an engineer at Sunstone Circuits, and **Matt Stevenson** is the VP of sales and marketing at Sunstone Circuits. To read past columns or contact Tise and Stevenson, click here.


Bob Tise


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Bringing the Green Revolution to Electronics

Researchers are investigating how to make electronic components from eco-friendly, biodegradable materials to help address a growing public health and environmental problem: around 50 million tonnes of electronic waste are produced every year.

Less than 20% of the e-waste we produce is formally recycled. Much of the rest ends up in landfills, contaminating soil and groundwater, or is informally recycled, exposing workers to hazardous substances like mercury, lead and cadmium. Improper e-waste management also leads to a significant loss of scarce and valuable raw materials, like gold, platinum and cobalt.

For example, there is widespread interest in developing organic field effect transistors (FET), which use an electric field to control the flow of electric current and could be used in sensors and flexible flat-panel displays.

Researchers are especially keen to find biocomposite materials that work well in resistive random access memory (RRAM) devices. These devices have non-volatile memory: they can continue to store data even after the power switch is turned off. Biocomposite materials are used for the insulating layer sandwiched between two conductive layers. Researchers have experimented with dispersing different types of nanoparticles and quantum dots within natural materials, such as silk, gelatin and chitosan, to improve electron transfer. An RRAM made with cetyltrimethylammonium-treated DNA embedded with silver nanoparticles has also shown excellent performance.

"We believe that functional devices made with these fascinating materials will become promising candidates for commercial applications in the near future with the development of materials science and advances in device manufacturing and optimization technology," the researchers conclude.

(Source: ACN Newswire)

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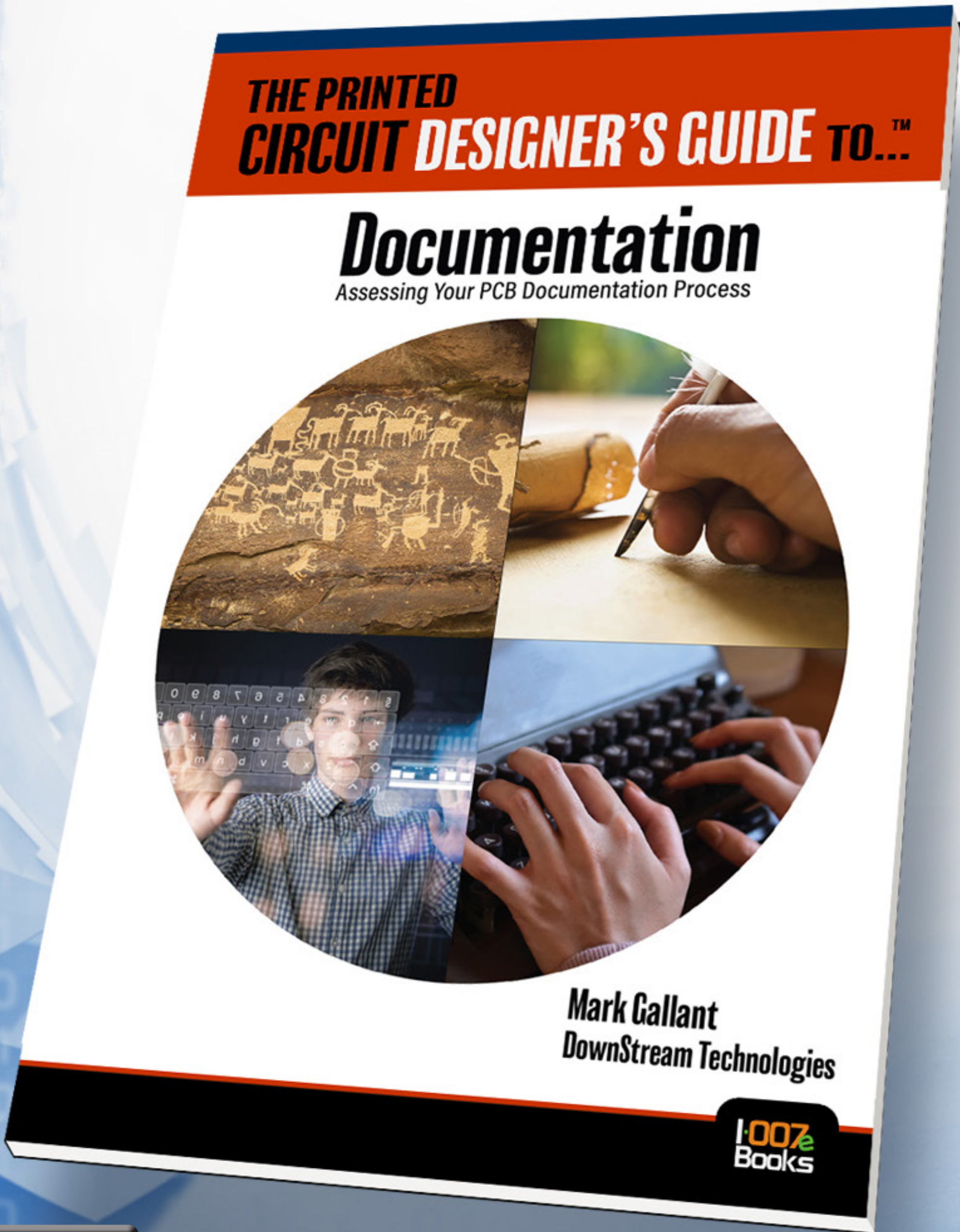

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Mentor: Managing Small Problems for Profitability

Todd Westerhoff

Feature Interview by Andy Shaughnessy
I-CONNECT007

At DesignCon, I met up with Todd Westerhoff, product marketing manager for high-speed design at Mentor, a Siemens Business, to discuss common design profitability issues and cost-aware PCB design. He explains how simple problems can "slip through the cracks" and cause delays, what you can do, and how first-order analysis can make simulation accessible to designers who wouldn't simulate otherwise.

Andy Shaughnessy: Tell us about how the "small stuff" can get you in trouble. You say that we, as designers, take care of the big challenges pretty well, but projects get held up anyway.

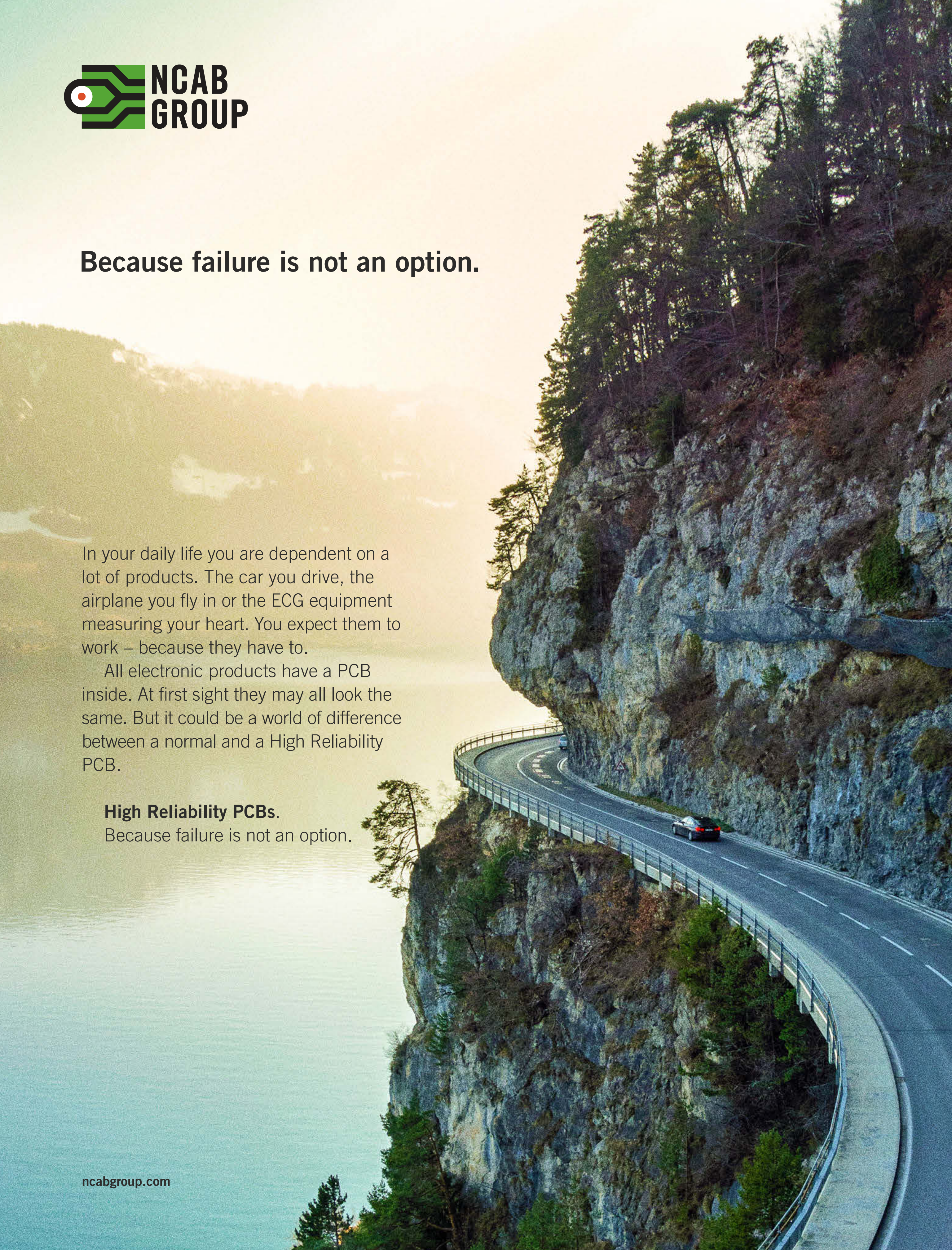
Todd Westerhoff: Lifecycle Insights ran a study about a year ago that I find to be quite telling. They asked companies questions, such as, "How much simulation do you use in your process? Do you hit the mark in terms of your time, budget, or release date?" The two most interesting findings had to do with schedule and budget. They found that only one in four projects gets delivered on time and on budget (in other words, according to plan).

Shaughnessy: Even that may be optimistic.

Westerhoff: You're right. Digging deeper, 30% of projects were delivered on time, but only by pulling in additional staff, 28% were delivered late, and 17% of projects were canceled entirely (quite possibly as a result of resources pulled to bail out other projects). The bottom line is that design projects had a 25% success rate, and that's a problem.

Why does this happen? Consider all the different requirements designers are trying to accommodate: SI, PI, EMC, mechanical clearances, vibration, reliability, and so on. Designers live in a world where all of these things have all become specialties or have expert domains. Designers have a network of specialists around them, whose time and input they need to move their design forward. The problem is that each specialist looks at a different slice of the design, but how does all that input get integrated and turned into a holistic view that guides design trade-offs? How do those decisions get made? Does the designer understand enough of each of the specialist's inputs to make the right trade-offs in the design of the board? The answer, based on the success rate, is perhaps not.

Another fascinating thing was when we asked our customers about the challenges they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have faced, they said, "It isn't the hard stuff, like 112 Gb/s serial links or DDR5 interfaces, that we need help with. Those are big challenges, but we know to focus on those, and we solve them. It's the simple stuff that we're not focused on that often nails us."

Most SI/PI experts have a collection of different tools that they use with a unique flow they've developed themselves. Their flow is a complex series of steps that usually only they can run because it's been designed for their own use. Experts are solving demanding problems, by definition, and their focus is on solving those problems, not creating paths for others to follow. Add to that the fact that none of us seems to have enough SI experts in our organization, and you end up with a design analysis bottleneck.

Experts are solving demanding problems, by definition, and their focus is on solving those problems, not creating paths for others to follow.

We all manage scarce SI resources the same way. We identify interfaces based on risk and priority, and only the toughest problems get expert attention. Thus, there's an increasingly small percentage of designs that experts look at, and everything else gets designed and verified to manufacturer guidelines or industry best practices (rules of thumb). How do those interfaces get verified? You got it: good old-fashioned manual design reviews.

Shaughnessy: And most design review meetings are slightly more enjoyable than torture.

Westerhoff: That's right. Let's face it: Manual design review meetings are long, boring, and tedious. About 20 years ago, we asked EMI specialists at Sun Microsystems how they signed off boards for EMC, and they said, "We look at the layout layer by layer." I was amazed at the time, wondering how they kept from going blind. The truth is, 20 years later, this is still what people are doing for most of their designs, and not just for EMC.

If 10% of the design is getting expert attention, 90% of the design is just getting eyeballed. Designers and their peers are reviewing the design and hoping for the best. Given the complexity of modern designs and how repetitive the process is, it's not surprising that stuff gets missed. We have a product called HyperLynx DRC that encodes domain-oriented design rules (SI, PI, EMC, analog, safety) and automatically checks the design to identify possible problems. Note that I said possible problems, not just problems, and that's a key point. You can think of this as a "design rule scanner." It quickly identifies areas for a designer to review, making a decision about whether the design is okay, definitely needs to change, or requires detailed analysis to investigate. The important points here are that checking is quick and spans domains and that analysis can be performed by the designers directly.

Shaughnessy: Right. The designer doesn't want a tool that requires a Ph.D. to operate.

Westerhoff: Absolutely, but there's a balance between simplicity and usefulness. We all want everything to be simple so that we can use it with no training and get useful information out of it. With DRC, in particular, it's definitely a case where the more you tell it, the more useful the output becomes. When I use DRC to check a design for decoupling cap placement, it needs to know what the metrics are. It needs to know which pins on ICs are power pins, how to identify decoupling caps, and what the maximum allowable distance from an IC to decoupling cap is. That's not hard, but I still have to perform a level of setup to get useful output, and that's a mixed bag. There's a class of people who will do that without hesitation and swear by it, and there's another class of people that won't put even that level of effort in. The latter tend to say, "If it takes extra work, I don't have time, and I'm not going to do it."

Shaughnessy: We run into designers who confuse DRC with DFM; they run a DRC and think of it as DFM.

Westerhoff: That's understandable, as both are essentially rules-based automated checks. DRC tends to focus on design functionality; if you don't change that, the design won't function. DFM tends to be more about the ability to manufacture in volume, but there's certainly some overlap.

I think another area of confusion comes after DRC identifies a potential issue. What then? DRC doesn't always find hard errors. Sometimes, it flags things that need further consideration; they might be a problem, or they might not. Those issues need review by a designer, and we find they tend to fall into one of three categories: obvious problems, with no need to analyze in more detail that need to be fixed; obvious non-problems, with no need to analyze in more detail that can be marked as such; and unclear problems where models and simulations are required to determine what needs to be done.

The good news here is that the first and second outcomes take the issue off the table without placing any burden on those scarce SI resources we talked about, and they improve the quality of the design as well. The third outcome is the most interesting; most of the time, the only option is to pass the problem to experts for analysis and wait. Of course, if the experts are too busy, you make your best guess and hope for the best.

But what happens if you don't need expert-level simulation to resolve the issue? We have been working with our customers to put simulation directly into designers' hands in a simplified way. We let designers see simulation results daily while the board is being routed with the goal of being able to find problems and correct them while layout is in process. We want to avoid finding problems only after layout is complete because that's when changes to the design are the most difficult and time-consuming.

But how? There aren't enough experts to go around. The trick is that we don't need to do the same level of accuracy, signoff quality simulation that an expert would normally do. We can do something far simpler because we're looking for things that are obviously out of whack (excessive ringing, excessive crosstalk, bus delays don't match). We call this first-order analysis. We model interconnect accurately using 3D EM solvers, but we don't do the same level of model setup and post-processing as signoff analysis because we're looking for outliers.

Shaughnessy: Designers typically haven't wanted to simulate in the past. Why would they want to start now?

Westerhoff: The traditional approach has been to go get more experts and more sophisticated tools, but we have reached a breaking point. The percentage of SI/PI experts in the design community continues to shrink, and design complexity continues to increase. Many designers have avoided picking up SI tools because the learning curve was too steep, and it's only getting steeper. We have reached a point where we think we need an expert to do anything, but they're too busy, so now what? Here's a weird question: How many homeowners people can patch a wall or replace a light switch anymore?

Shaughnessy: I can, but I have to. I'm a landlord.

Westerhoff: How about an outdoor faucet? Last winter, I forgot to drain one of my outside faucets. When it got down to 2°F, the water inside the head expanded and cracked it. It was so frozen that it didn't leak immediately, but as the weather warmed up, it created a nice, frozen waterfall on the backside of my house. Here's the point: The faucet itself was worth $10, but it cost me $250 to have a plumber fix it because I didn't have the tools or skills to do that kind of repair myself.

I think SI is in a similar situation. Designers are bottlenecked waiting for expert opinions and reviews, even when a first-order analysis would have allowed them to proceed. The truth is that the experts don't want to be bothered with simple problems any more than designers want to wait for the expert's opinion, so why not break the logjam?

We have found that combining DRC and first-order simulation can be incredibly effective. We use DRC to scan the design and locate areas of interest, and then use first-order simulation to see how that part of the design behaves. It turns out not to be about the details of the I/O behavior, but about how the interconnect behaves because that's what system designers are really designing anyway. The exact details tend to vary from case to case, but the consistent focus is on identifying a suspect area of the design, using the right level of EM modeling to capture particular types of effects, and then utilizing simulation to excite and observe the area's behavior as simply as possible. We have been able to create entirely automated processes for customers this way. A PCB designer checks in a board at the end of the day and a set of simulation results are waiting the next morning.

Shaughnessy: On a different note, do your customers come to you with demands for cost-aware design capability? We ask people if they know the total cost of their designs, and they usually have no idea.

Westerhoff: I think most designers don't have good, reliable access to cost information. In most companies, those details live in some other department, and by the way, costs change with time, so the cost to build a board when I design it probably isn't what it costs in production. If you're talking about total cost, including engineering costs and other overhead, I don't think designers see that at all. The bits and pieces of that data are all over the company, and by the time it all gets pulled together, it's probably only shared at the executive level.

What does it mean to design products for extreme volume manufacturing? Chances are the people who designed my fitness tracker had a pretty good idea of what production costs were going to be because they expected volumes in millions, and a fraction of a penny mattered. The people who designed my laptop probably had a different idea of volumes and cost sensitivity. In my "big iron" networking days, the first revision of a design was about functionality, performance, and getting to market; cost reductions came later because volumes were lower and the product lifetime was much longer.

Let's look at this from the standpoint of an SI person and consider the case of a popular consumer product. Volumes are high, and design cost is critical. One rule of thumb for high-speed design is to provide a clean return path by routing signals on a ground plane. However, adding ground planes—if it comes to that—costs money, and your cost target may not be able to support that. There's a strong incentive to bend the rules, reference traces to power, ground shapes on the same layer, or something else. The trick is that it raises the modeling and simulation bar significantly. To make sure the design will work, you'll need to model signal return paths explicitly, something we call power-aware simulation. That will let you take cost optimization to a whole new level, but I don't see a lot of people going there yet. I wish we heard more about this because I think it's fascinating.

Shaughnessy: It seems like this could be a real brass ring for managers looking to reduce board costs for high-volume design.

Westerhoff: I agree. We'll see where this goes.

Shaughnessy: This has been great, Todd. Thanks for speaking with me.

Westerhoff: Thank you, Andy. DESIGN007


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EMA: Early Access to Data Is Key to Cost-driven Design

Chris Banton

Feature Interview by Andy Shaughnessy
I-CONNECT007

How can designers and design engineers be sure that they're cutting any excess cost from their designs? According to Chris Banton of EMA Design Automation, providing designers the data they need early in the design process is a big part of making cost-effective design decisions. I sat down with Chris at DesignCon to discuss some of the ways designers can make their designs and final products more profitable.

Andy Shaughnessy: It's good to see you again, Chris. Can you give us a quick background about what EMA does?

Chris Banton: Sure, Andy. Thanks for chatting with me. We know engineers are being tasked with more and more responsibilities within the design cycle and have shorter time-to-market deadlines. Our mission is to help engineers design reliable products quickly through software solutions catered specifically to our client's design and to-market goals. EMA is a design automation company focused on the electronics and high-tech industries for over 25 years. We've been doing this for over 25 years, primarily on PCB design analysis. For the bulk of that time, we have been a Cadence channel partner, where we focused on helping Cadence customers within their entire design ecosystem.

Shaughnessy: Earlier, we were talking about designing for cost and profitability. You have a few thoughts on this topic.

Banton: It's an interesting topic because engineers don't necessarily get a chance to do that. While engineers can have a huge impact on the cost and profitability of a product, I also believe we don't really empower them with the information they need to be able to do that. We started doing some work with SiliconExpert, a leader in the supply chain world; they are focused on helping supply chain engineers make sure they're picking the right parts and have stock in everything. Through this collaboration, we found that, oftentimes, an engineer will design something with the data they have, which is not necessarily the data they need.


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Next, it goes to the supply chain, and they say, "Cross that off. No, change that," and/or, "You can't buy that because it's obsolete. This won't work," and then they kick it back. Then, the engineer has to go back and change it; it's a horrible cycle.

With SiliconExpert, we thought, "What if we brought that data into the design phase?" If engineers have the data, they can make the right decisions. It's all about helping them to work smarter, not harder. When you know a part is going to go obsolete in three years, and you have a five-year product life expectancy, or there's low stock so they can't buy enough, then you're going to make decisions based on this data.

Shaughnessy: Sure. It does seem like a lot of designers are forced, because of the time-to-market constraints, to make decisions early on when they don't necessarily have all of the data.

Banton: Agreed. However, sometimes, that's because the data is not made accessible to them. We were interested in working with SiliconExpert because they have the data engineers need—it's what they do. Give it to the engineers and let them be able to access it when they make their selections.

Recently, we conducted a little experiment where we said, "Here are four parts based on this standard data, as well as the electrical functionality and price. Which one of these would you pick?" Every engineer picked the cheapest one. Their thought process was, "We're going to save the company some money." Afterward, we said, "What if we told you that the cheapest is out of stock, there won't be any more for six months, and it's going obsolete in three years?" Their answer then changed, and they picked the one that was a little bit more expensive. Ultimately, we asked ourselves the question, "How can we help an engineer have the information they need to make a cost-driven decision?"

Shaughnessy: Are your customers expecting you to help them make cost-aware design decisions?

Banton: Yes. As you mentioned, they have schedules to meet. They don't have time to scour the web to figure this stuff out. They need the data packaged and delivered to them in a way where they can continue to design, but also have that additional information available.

That is what we focus on. How can we automate all of this and take away tasks that engineers get stuck in that really aren't productive? Software can do that much faster, so the engineer can focus on what they really need to be thinking about. Does this product work? Is it going to accomplish our goals?

Shaughnessy: Right, that's what it's all about. This could also help designers and engineers avoid over-constraining their boards and making them reliable but more expensive than necessary.

Banton: Right, and, obviously, we're very focused on the software. Customers don't have much time, and they're being asked to do a tremendous amount. Some engineers will take a known-to-be good design or circuit and keep using it. Even though you may be able to shave some space off, if you do that, you have to requalify it, and that's when simulation and analysis really help there. Capacitors are a pretty common and basic example of over-engineering. You'll have a design, and on the last page is just a pile of capacitors.

Shaughnessy: The shotgun approach.

Banton: Exactly. Sometimes, they just spray capacitors everywhere; often, they're pretty cheap, so it's not that big of a deal, but if you think about the volume you might be producing and the board space you might save, then those can become meaningful if you can quantify that ahead of time. What if you had some software that can help you identify the optimal placement for capacitors? We have a product that will help you optimize decoupling capacitor placement based on your design. It can run thousands of scenarios very fast and come back to you with the ideal way to place them.

Shaughnessy: It's funny. In almost every interview, it all comes back to data, whether we're discussing an EDA tool or an SMT line. The customers are usually happy with the tool, but they can't get all of the data they need, or they can't get it in the best format for them to be able to use it effectively. They can't get the data right away, or they can't make sense of it. We have all of this data, but it's not always in a useful format.

Banton: For the most part, if the engineers are presented with the right data, they can make an informed, intelligent decision, but if they only have half the picture, then you're asking them to try to figure out and guess an awful lot. At the end of the day, you want to cut some costs, but the priority is a working product. You're probably going to err toward what you know is going to work.

Shaughnessy: Make it work first, and then try to trim some costs off it, which isn't always the best way to go.

Banton: And that can lead to its own problems. It's that waterfall effect where every decision piles onto the next decision. It's hard to say, "We'll just swap this part out." How many decisions have you already made because you picked that part?

Shaughnessy: Do you have any advice that you would offer designers and engineers as far as reducing costs and making the board more profitable?

Banton: It boils down to advocating for themselves. As we keep saying, electronics are pervasive; they are the brains of all these great things that we take for granted more than we should. How do you get more say in the organization that what you're doing has a tremendous amount of value to that company?

If you can show that you can cut costs in the design process, it tends to raise some eyebrows in the higher levels of your organization. You have to wrap your mind around the idea that you can help save the company money and be more efficient.

Shaughnessy: It's like Rick Hartley says: You have to be your biggest advocate in the company. If the company doesn't know that you know what you're talking about, that's your own fault.

Banton: Look at simulation tools. With simulation, you could tell your manager, "We took a layer out of the board, and I was able to verify that the board is still going to work, and that's going to save us this much money." The benefit then becomes tangible. Whereas, if you say, "I made sure it's going to work," that's your job. Or if you look at reliability and sensitivity analysis, we usually talk about it in terms of overstressed parts and making sure those are okay so that they don't blow up, but look at the other side of it. Maybe you can identify some understressed parts you could then swap with cheaper ones because you know it's still going to operate within the parameters that you set. That saves money.

Shaughnessy: We ask designers and CAD managers how much each design costs the company, and a lot of times, they don't know. I thought designers would know.

Banton: Some of it boils down to this: How do you map that out when you're working on four projects simultaneously? Some of this involves the constant change going on from other departments giving input. Then, you go to manufacturing, and that's kind of out of your control. It's not a simple thing to model, but the first step is identifying in the engineering domain the things that we can improve on and ensuring that we're effective from a design perspective.

Shaughnessy: How often is cost one of the big criteria that your customers are worried about? I know it varies from segment to segment.

Banton: It goes to your previous comment about how they're not sure what the total cost is. It's hard for them to think, "Let's get better at this thing that we don't really understand." However, we've seen that with the right information early in the process, engineers make the most electrically sound, cost-effective decisions; they're not trying to spend money just to spend money.

Shaughnessy: Good point. Is there anything else you'd like to add?

Banton: Designing for profitability is an interesting topic. You need to be able to show your company, "This is the material impact we're having, not only because we're building this, but also because we're doing it in a way that's making the company more profitable." That can help the engineering organization be more of a value center inside the company. It's funny because a fabricator can tell you how much it costs to build 10,000 of these boards, but it's much harder for a designer to do that.

Shaughnessy: Thanks for your time, Chris. It's always a pleasure.

Banton: Thank you, Andy. DESIGN007

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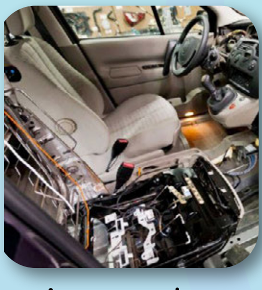
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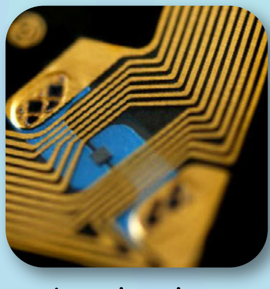
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Transmission Line Termination

Beyond Design

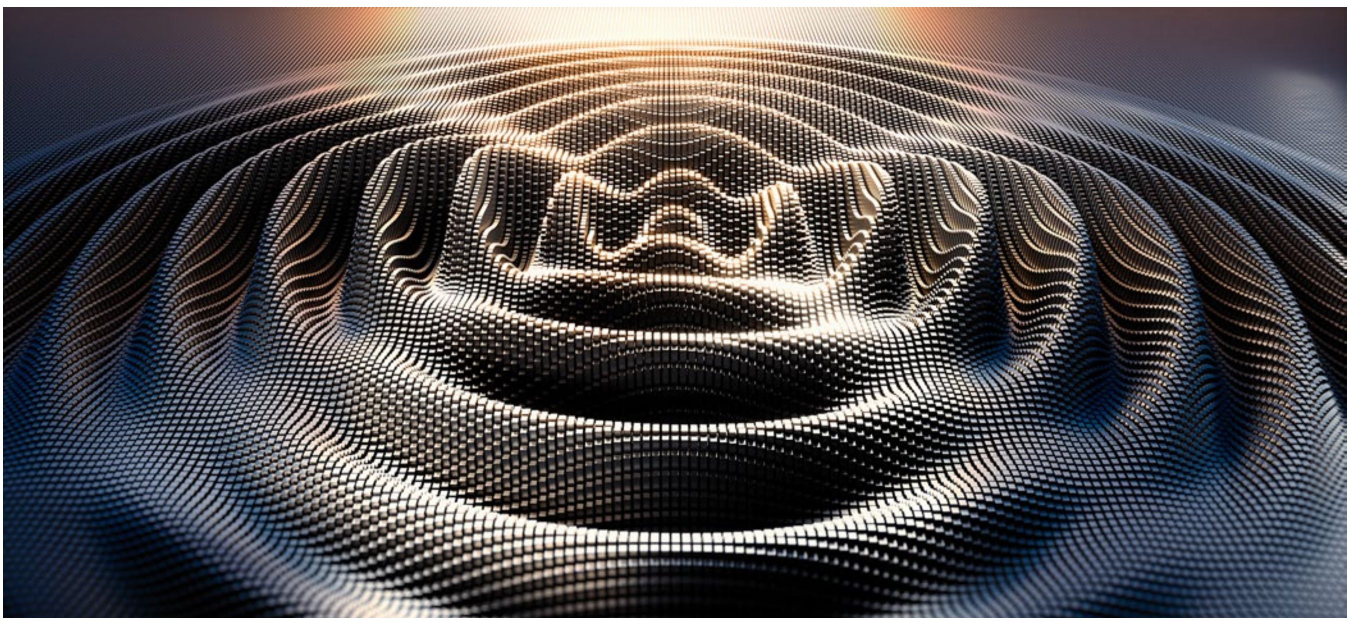
by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

In a previous column "Beyond Design: Interconnect Impedance," we saw that the impedance of the interconnect is the most critical factor in high-speed PCB design. Unfortunately, the source impedance of a digital IC driver is typically lower than the impedance of the transmission line (10–35 ohms). This is far from the ideal situation for the perfect transfer of energy, and, in most cases, results in reflections and electromagnetic radiation if not addressed.

Whenever a signal meets an impedance variation along a transmission line, there will be a reflection, which can seriously impact signal integrity. By understanding the causes of these reflections and eliminating the source of the mismatch, a design can be engineered with reliable performance. In this month's column, I will look at how to effectively terminate transmission lines.

In an ideal world, the energy emanating from an IC output driver would travel through the PCB transmission line and be totally absorbed by the load. However, if energy is not completely absorbed, then the residual will be reflected back along the interconnect, reaching the original source of energy at the output driver. Reflected energy acts like a standing wave and adds or subtracts to the original signal, causing ringing. Resonance can develop at a signal's fundamental frequency or harmonics resulting in multiple bounces and emission of radiation. This situation only occurs when the round-trip delay of the interconnect exceeds the signal rise time.

Even if the multilayer PCB has been designed with controlled impedance in mind, impedance discontinuities can still occur due to input gate capacitance, branches, stubs, or test pads; variations in dielectric materials; a neck-



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down in a via field; skew in a differential pair; or a gap in the return signal path. Generally, the reflected noise level should be kept below 10% of the voltage swing, but this depends on the noise budget. In more conservative designs, the noise budget may be as low as 5%.

There are numerous ways to terminate transmission lines, but the most common methods fall into three categories:

1. Series termination
2. End termination
3. Differential pair termination

1. Series Termination

Series termination (aka source termination) is excellent for point-to-point routes—one load per net. It works well for traces that are electrically short and is used to fan out multiple loads radially from a common source (star routed) without affecting other circuits in the network (Figure 1).

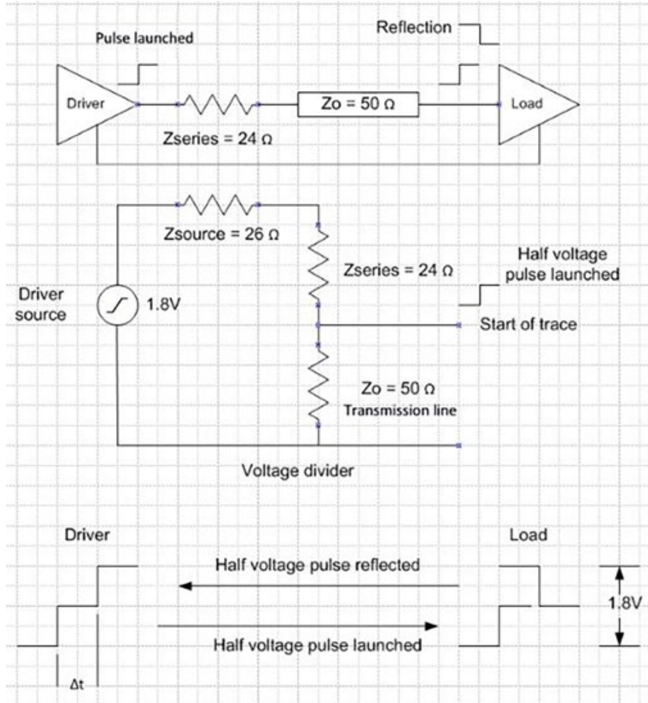

Figure 1: Series termination (back-matching).

Impedance back-matching slows down the rise and fall times and reduces the ringing (over/undershoot) of clock drivers. A pulse is launched from the source, but due to the voltage divider network formed by the source impedance, series terminator, and the transmission line, only half the amplitude appears at the transmission line. As this half voltage pulse reaches the load, it is instantaneously reflected back along the trace. This reflected

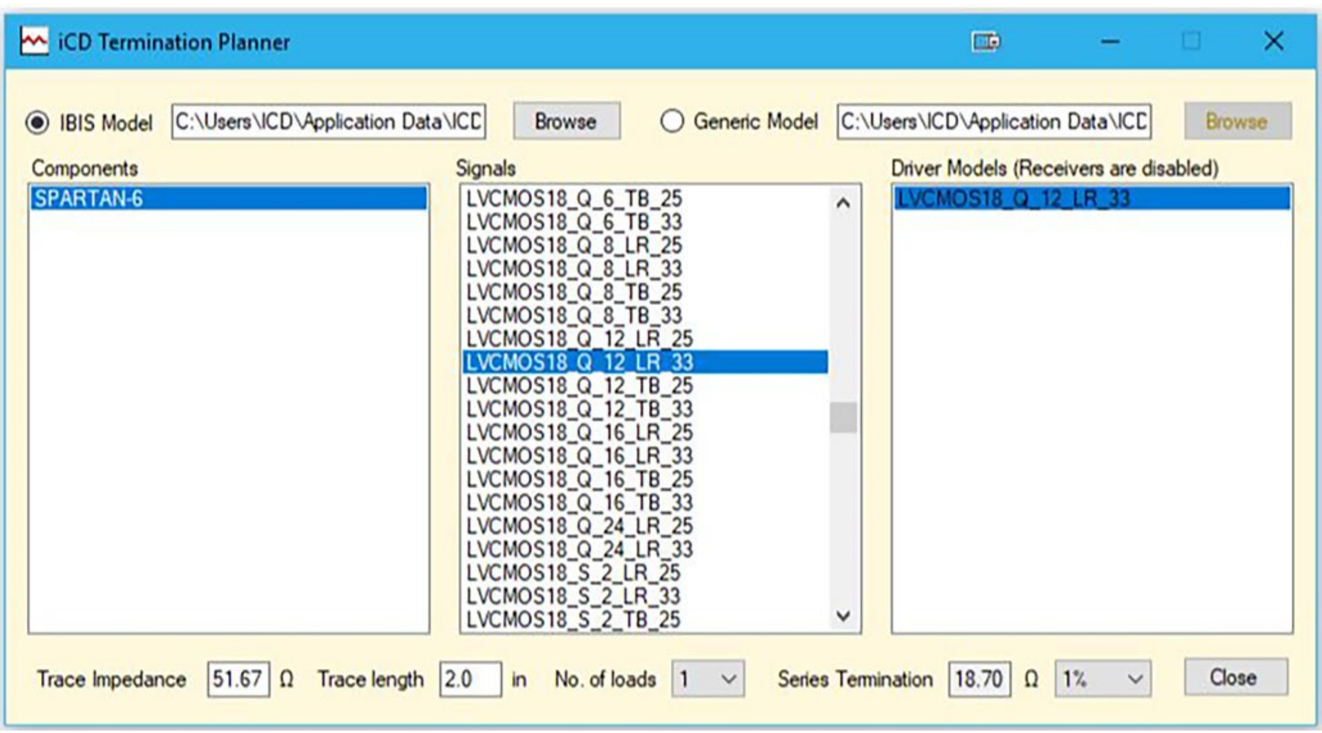

Figure 2: Matching the Spartan 6 driver to the transmission line (iCD Termination Planner).

pulse adds to the initial pulse to form a full voltage wave, so we get the signal we want at the load.

The reflected pulse travels back to the source. When it reaches the series terminator, it sees the series resistor (24 Ω) plus the source impedance (26 Ω) totaling 50 Ω. Since the transmission line is also 50 Ω, there is no discontinuity of impedance; therefore, there will be no reflection. The signal will be totally absorbed by the terminating resistor and the source impedance, preventing further ringing.

A receiver located at the very end of the trace will see an almost perfect signal edge. But a receiver in the middle or near the resistor will first see a 50% signal and then a 100% signal. Because of this, series termination is only used when there is only one receiver/load, and that receiver must be located at the very end of the transmission line.

To determine the value of the series terminator, the source impedance must be extracted from the IBIS model of the driver IC. Subtracting the source impedance from the trace characteristic impedance gives the required series terminator value (Figure 2).

In the previous example, using a 12 mA LVCMOS 1.8V driver of a Spartan 6 FPGA, an 18.7-ohm series resistor is required to match the driver to the 51.67-ohm trace on the outer layer. This is automatically derived from the IV curves of the Spartan 6 IBIS model by the iCD Termination Planner.

Figure 3 illustrates the ringing (red) in an unmatched transmission line. This ringing, which is also represented by over/undershoot (right), is dramatically reduced by terminating the transmission line with an 18.7-ohm series resistor (blue).

2. End Termination

Multi-drop bus topologies require parallel or end termination, which prevents reflections from being formed at the transmission line ends. With DDR3/4 memory devices, for instance, the fly-by address, control and command (ACC) signals should be routed as close as possible to the memory device pins and the parallel termination placed at the end of the line (Figure 4). The resistor values are twice that of the transmission line as they are in parallel from an AC perspective. Short stubs can be used to connect the passing signal to each memory device in sequence, but the longer the stubs, the higher the capacitance. This stub capacitance, along with the parasitic input capacitance of the receiver pin, creates an imperfection in the termination network.

Figure 4 illustrates a typical DDR3 fly-by topology with the termination at the very end of the final load. Also, the passing address signal trace goes directly to the receiver pins with no stub. This is the ideal scenario. In this case, there are no reflections from the termination, which can be seen from the waveforms.

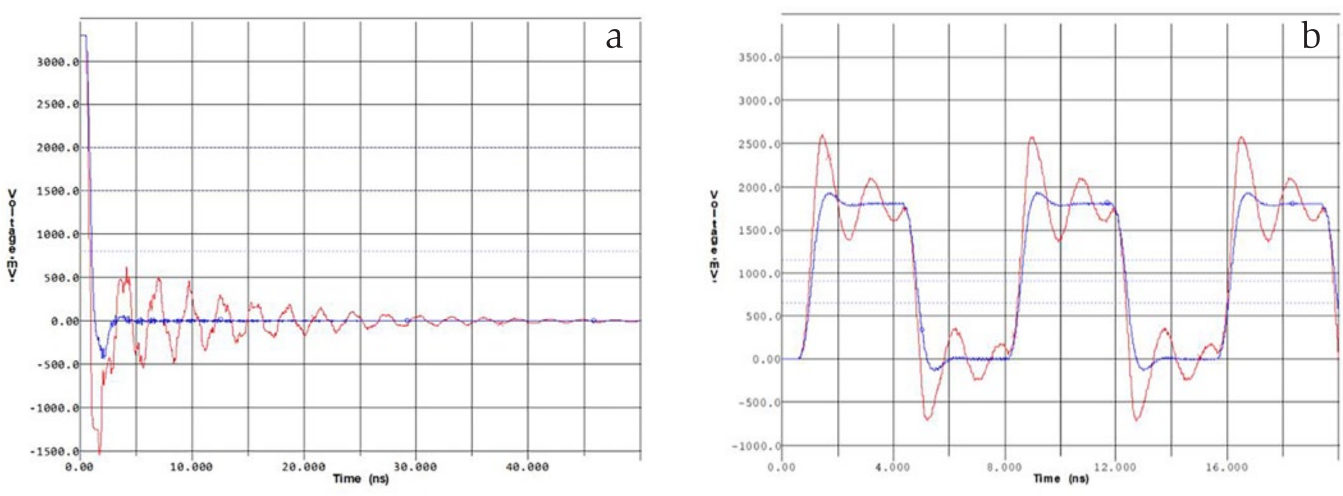

Figure 3a and 3b: Ringing is reduced dramatically by adding a series terminator (simulated in HyperLynx).

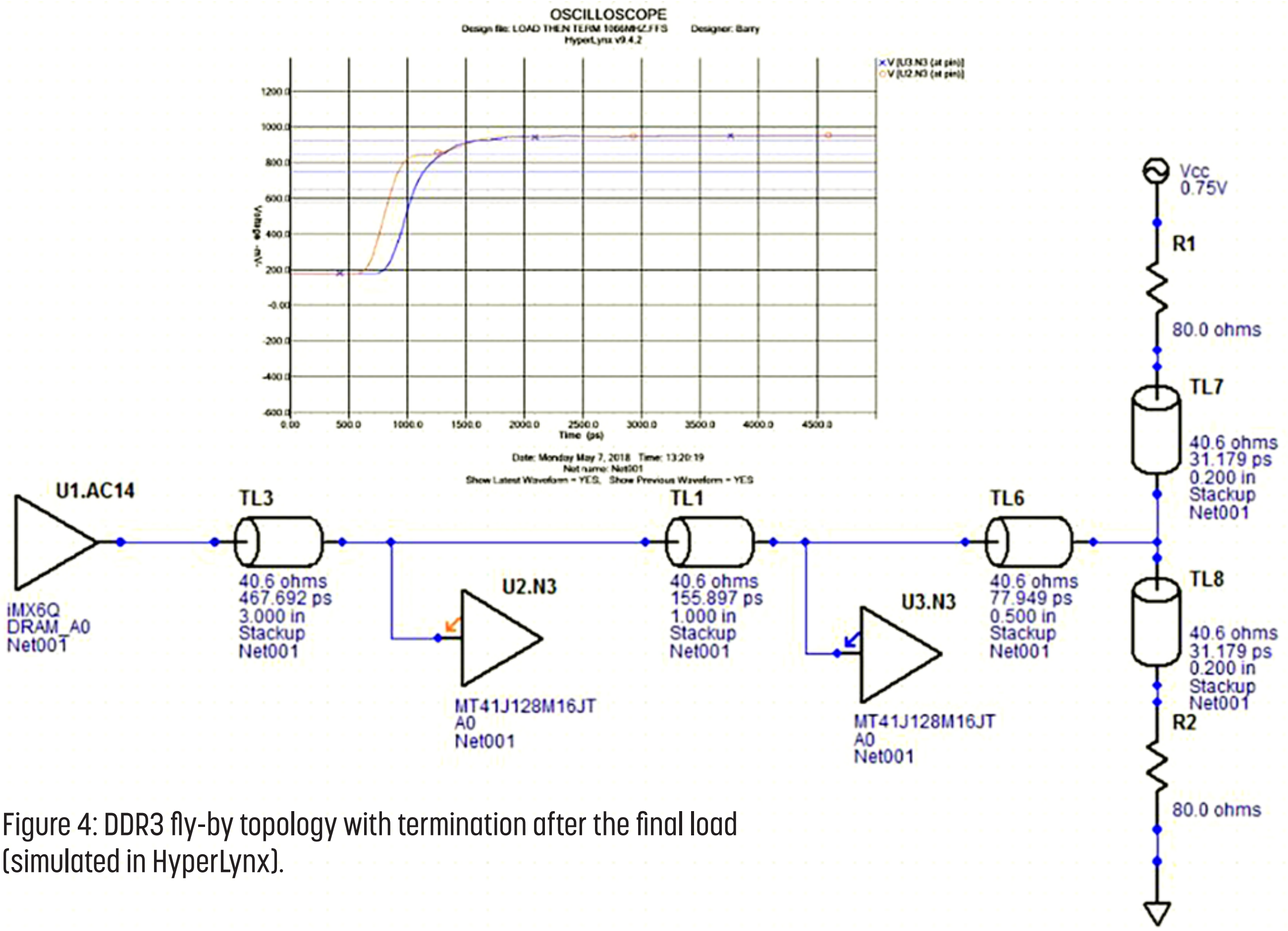

Figure 4: DDR3 fly-by topology with termination after the final load (simulated in HyperLynx).

3. Differential Pair Termination

When a differential signal reaches the open end of a differential pair, it will see a high impedance, and it will be reflected. A common method of reducing these reflections is to place a resistive load at the end of the pair, which matches the differential impedance of the transmission line.

However, the single resistor differential termination (Figure 5a) only terminates the differential mode signal—not the common-mode signal. Any transient common-mode signal moving down the differential pair will see a high impedance at the end of the pair and reflect back to the source. The noise created can be seen at the top and bottom of the eye diagram. The common-mode signal, having the same voltage between the two signals, will not see the termination. Depending on the impedance of the driver, the common-mode signals created will bounce back and forth down the transmission lines. And because the termination resistor never perfectly matches the driver impedance, there is always a fixed offset. Any asymmetry in the differential pair will convert the differential signal into a common-mode signal.

Whereas the differential center tapped termination (Figure 5b) terminates both differential and common-mode signals, note the nice clear eye. It is best used when you have a low impedance driver on a long transmission line. This strategy introduces less DC offset. The DC blocking capacitor is for level adjustment of DC balanced circuits, such as clocks, 8B10B coding, etc.

When Do We Need a Termination?

If the transmission line is short, reflections still occur but will be overwhelmed by the rising or falling edge of the signal and may not pose a problem. But even if the trace is short, termination may still be required if the load is capacitive or highly inductive to prevent

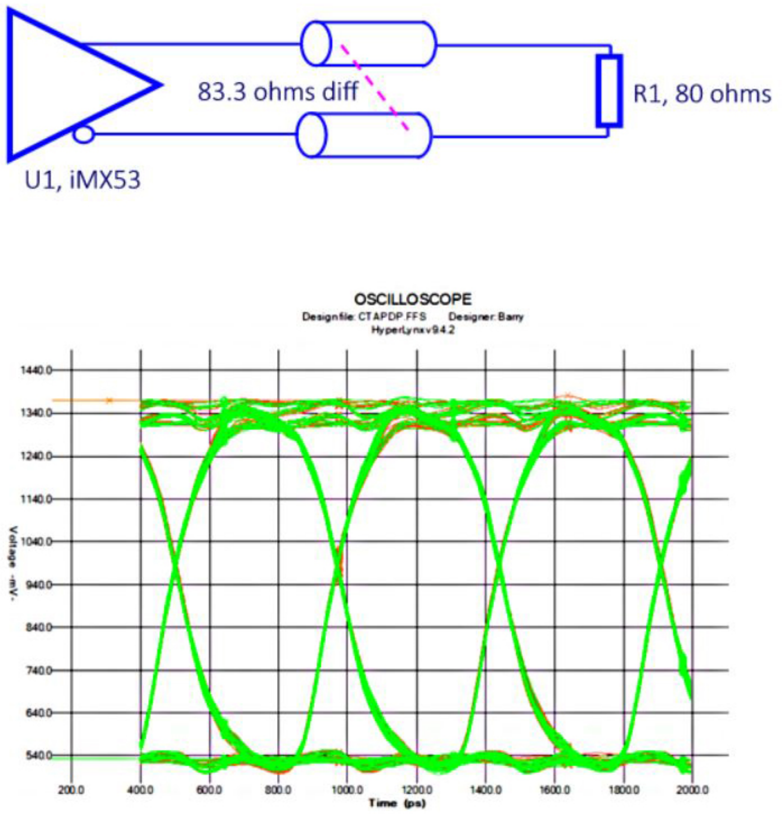

Figure 5(a): Single resistor differential termination.

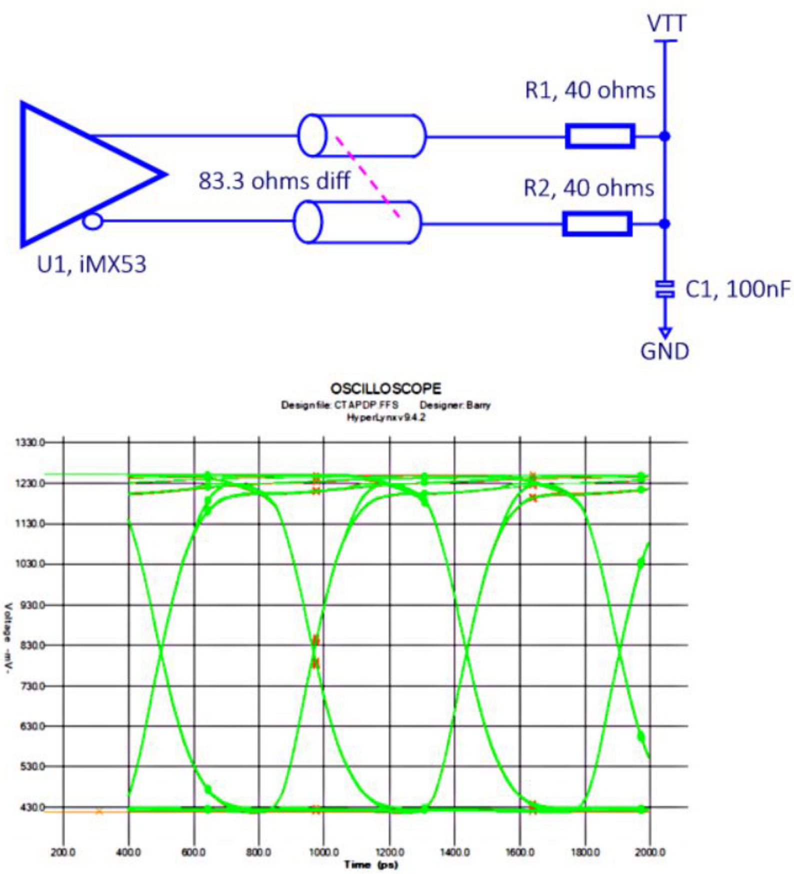

Figure 5(b): Differential center tapped termination.

ringing. Generally, when the trace length exceeds one-sixth of the electrical length of the rising edge rate, then termination is required. Regardless, it is always a good policy to keep critical signals and return paths as short as possible.

Key Points

- The source impedance of a digital IC driver is typically lower than the impedance of the transmission line. This results in reflections and electromagnetic radiation if not addressed
- Whenever a signal meets an impedance variation, along a transmission line, there will be a reflection which can seriously impact signal integrity
- Impedance discontinuities can also occur due to input gate capacitance, branches, stubs, or test pads; variations in dielectric materials; a neckdown in a via field; skew in a differential pair; or a gap in the return signal path
- Series termination is excellent for point-to-point routes, one load per net. It works well for traces that are electrically short and is used to fanout multiple loads radially from a common source
- Impedance back-matching slows down the rise and fall times and reduces the ringing (over/undershoot) of clock drivers
- Series termination is only used when there is only one receiver/load, and that receiver must be located at the very end of the transmission line
- Subtracting the source impedance from the trace characteristic impedance gives the required series terminator value

- Multi-drop bus topologies require parallel or end termination, which prevents reflections from being formed at the transmission line ends
- The end termination resistor values are twice that of the transmission line as they are in parallel from an AC perspective
- A common method of reducing reflections from differential pairs is to place a resistive load at the end of the pair, which matches the differential impedance of the transmission line
- The single resistor differential termination only terminates the differential mode signal—not the common-mode signal
- Depending on the impedance of the driver, any common-mode signal created will bounce back and forth down the transmission lines
- The differential center tapped termination terminates both differential and common-mode signals. It is best used when you have a low impedance driver on a long transmission line
- If the transmission line is short, reflections still occur but will be overwhelmed by the rising or falling edge of the signal and may not pose a problem **DESIGN007**

Further Reading

- B. Olney, "Impedance Matching–Terminations," *The PCB Design Magazine,* October 2013.
- B. Olney, "DDR3/4 Fly-by Topology Termination and Routing," *Design007 Magazine,* June 2018.
- B. Olney, "Beyond Design: The Fundamental Rules of High-Speed PCB Design, Part 2," *Design007 Magazine,* October 2018.
- E. Bogatin, *Signal and Power Integrity: Simplified,* Prentice Hall, 2008.
- H. W. Johnson & M. Graham, *High-Speed Digital Design: A Handbook of Black Magic,* Prentice Hall, 1993.

Barry Olney is managing director of In-Circuit Design Pty Ltd. (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at icd.com.au. To read past columns or contact Olney, click here.

Sweat Sensor Detects Stress Levels: May Find Use in Space Exploration

If someone asked you how stressed you are right now, what would you say? A little, a lot, or you don't know?

Those are all valid responses, but they are not especially useful to researchers and medical professionals because they are subjective and not easily quantified. Nonetheless, in lieu of a better method of measuring stress, the common method for years has consisted of a stress questionnaire. The main alternative to the questionnaire, a blood test, can provide quantitative data but requires a trained professional to draw the blood, and the stress of the procedure itself—being poked with a large needle—can skew the results of a lot of people.

But something better might be right around the corner. Wei Gao, assistant professor of medical engineering at Caltech, has produced a wireless sweat sensor that can detect levels of cortisol, a natural compound that is commonly thought of as the body's stress hormone. In a new paper appearing in the journal *Matter,* Gao and his fellow researchers demonstrate how they designed and made the mass-producible device, how it works, how it is effective at detecting cortisol levels in near real-time.

The development of an inexpensive and accurate device for measuring cortisol could allow for more widespread and easier monitoring of stress but also of other conditions including anxiety, post-traumatic stress disorder, and depression—all of which are correlated with changes in cortisol levels.

(Source: Caltech)

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The Foundation of the PCEA Is Being Laid

The Digital Layout

by Stephen V. Chavez, MIT, CID+, PCEA

In this month's column, I highlight the Orange County Chapter's recent meeting and their transition from IPC to PCEA affiliation, recent PCEA activities, and the evolution of this column, including introducing Kelly Dack, CID+, PCEA's new communication officer.

Chapter Spotlight

by Scott McCurdy

PRESIDENT OF THE ORANGE COUNTY CHAPTER

The Orange County Chapter is doing very well in Southern California and has been active for 18+ years now. We are proudly the largest active chapter in existence based on the attendance at our quarterly meetings. We average 50–65 attendees at our meetings, and occasionally have 80+ people in attendance. In our most recent meeting, held January 21 in Irvine, California, we had an outstanding crowd with 80 people in attendance to hear the educational presentation by Gerry Partida, field application engineer with Summit Interconnect.

Gerry Partida

The main topic for this meeting was "Microvias: Have You Designed for Reliability? How to Detect Weak Microvias and Avoid Costly Assembly Defects and Customer Field Failures." As component pin densities get tighter with each passing year, designers have been pushed to use HDI with more microvias and

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Mike Creeden

blind/buried via structures. As a result, tighter via densities and signal integrity requirements in printed boards have revealed reliability concerns with microvia structures in high-performance products. Avoiding post-fabrication microvia failures is critical to the success of your products, and there are details that designers need to know.

Gerry's presentation reviewed concerns and reliability testing relating to microvias. He provided an overview of the HDI processes and presented the use of current test methods and the superiority of testing with the IPC-D-coupon and IPC-TM-650 test methods 2.6.7.2 and 2.6.27. Gerry also discussed the warning statement in the forthcoming IPC-6012E: Qualification and Performance Specification for Rigid Printed Boards.

If you're interested in learning from an industry subject-matter expert like Gerry Partida, attend and become a member of a local PCEA chapter in your area.

We also had Mike Creeden, Insulectro's technical director of design education, provide an overview of the new PCEA that included its inception details, the PCEA purpose/mission, and the advantages of membership. Mike's presentation was received extremely well with lots of interest and engagement by all in attendance.

At the end of the meeting, we opened the floor for discussion, as we always do. The main discussion this time was on the PCEA topic and the Orange County Chapter's future. When considering whether to affiliate with IPC or the new PCEA in an earlier chapter leadership meeting leading up to the chapter meeting, our chapter officers unanimously voted to become a PCEA chapter. In the chapter meeting, chapter leadership (and Mike Creeden) let members know our new direction going forward and the decision to leave the umbrella of IPC. The chapter's leadership decision and the new direction for the chapter were widely accepted with great enthusiasm and eagerness to move forward as part of the collective of PCEA.

I hope to see you at our next "lunch 'n learn" event under our new chapter name: Printed Circuit Engineering Association—Orange County Chapter (PCEA-OCC).

PCEA Activities

There has been and continues to be a lot of activity going on as PCEA's foundation is being laid. Several legacy IPC chapters have already made the decision to affiliate with PCEA, like the Orange County Chapter's actions. In early February, we held an executive board meeting. The overall structure of PCEA is forming nicely with executive board member elections wrapping up. The newly elected Executive Board members will be introduced in April's column.

Also, PCEA's website is up and running, but is still in its early stages of creation. It is our hope to have our official website released later in March. I encourage everyone to check out the website and sign up to receive more details of PCEA as we unfold in the industry.

In the coming months, we will expand the number of chapters while realizing a steady growth of our membership. If you're interested in joining or starting a chapter in your area, please feel free to participate and join the many professionals who are the backbone of our industry. Again, visit our website and contact us for more information.

The Evolution of 'The Digital Layout'

I have been writing this column for over a year now. It has been a huge success so far because it has been a team effort in getting all this put together month to month, not just my efforts alone. My main objective for this column was, and still is, to help promote continued globalization of knowledge sharing and education for any and all involved in the design, fabrication, assembly, and test of printed circuit boards. Getting people to communicate more and not just within but outside of their box is important. That is why I decided to be a contributor—for the betterment of our industry.

With that said, my evolution as a column writer will be evolving as I take on a leadership role within PCEA as chairman. In doing so, I will be passing on the oversight of this column to a renowned colleague and dear friend of mine, Kelly Dack, CID+. I will still share my thoughts through a "message from the chairman" section within the column, but Kelly will serve as the PCEA's communication officer and assume oversight of this column. I wish Kelly well and encourage everyone to contribute to the ongoing success of this column. We very much appreciate your readership.

Professional Development and Events

Here are some up-and-coming industry events to look out for in 2020. I hope you have the opportunity to attend one or more.

- April 7–8: **Cadence Live 2020** *(Silicone Valley, California)*
- April 27–30: **Zuken Innovation World Americas 2020** *(Coronado, California)*
- May 12-14: **IPC High-Reliability Conference** *(Baltimore, Maryland)*
- June 9–10: **PCB2Day—SMT Assembly Boot Camp** *(Austin, Texas)*
- June 11–12: **PCB2Day—Design Essentials for PCB Engineers** *(Austin, Texas)*
- June 14-20: **IPC SummerCom 2020** *(Raleigh, North Carolina)*

Kelly Dack

- June 22–25: **Realize LIVE 2020** *(Las Vegas, Nevada)*
- October 7–9: **AltiumLive 2020** *(San Diego, California)*
- September 8–11: **PCB West** *(Santa Clara, California)*
- November 11: **PCB Carolina** *(Raleigh, North Carolina)*

As always, if you have any local or regional industry event coming up in your area and would like to announce it, please feel free to submit the details to be listed in an upcoming column. For 2020 CID and CID+ certification schedules and locations, contact EPTAC to check current dates and availability (dates and locations are subject to change). DESIGN007

Stephen Chavez, MIT, CID+, is a Master Instructor of PCB Design for EPTAC, an SME in PCB design for a major aerospace corporation, and a member of the Printed Circuit Engineering Association (PCEA). To read past columns or contact Chavez, click here.

Cadence Helping Users to Save Time, Money With Automation

Brad Griffin

Feature Interview by Andy Shaughnessy
I-CONNECT007

During DesignCon, I spoke with Brad Griffin, the group director for product management for the system analysis group at Cadence. We discussed some of the areas where PCB designers can cut costs and how EDA companies can help these designers by automating certain time-consuming tasks. As Brad says, "The 'A' in EDA is for automation, right?"

Andy Shaughnessy: Good to see you again, Brad. We were talking a few minutes ago about ways that designers can design for profitability by adding profit and cutting waste during the design cycle. Tell us your thoughts on designing for profitability.

Brad Griffin: When you think about what Cadence can bring to the table for designing for profitability, it's about being efficient. We are one of the few companies that you can come to and get design tools and analysis tools. Historically, the idea is that you have designed something, throw it over the wall to somebody else, who analyzes it and says you made a bunch of mistakes; then, they throw it back. There's this iteration back and forth. Maybe you build a prototype and find out it doesn't work. All of that makes the design cycle get very long, and that's certainly not the way to profitability. The more you can make that efficient, the more profitable that you're going to be able to make your product and product line, and, ultimately, the more you're going to be able to build new products because you're going to get products out the door.

Our thinking is that we can guide a user toward in-design analysis; while they're designing a product, they're thinking about SI and PI. They're bringing up engines that are the same engines that their expert is going to use to sign off on later, but they're presented in a way where they don't have to be an expert. You can do a quick review of your power plane and make sure that you haven't created too many places where you're going to lose voltage and not going to be able to deliver power to certain components of the board. If you can quickly review that without having to bring a PI expert in, it's going to make you a better de-

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signer, and it's going to shrink that design cycle. Anything we can do to help the designer produce a better board before it goes to an SI or a PI expert will reduce that design cycle and improve the overall profitability of the design.

Shaughnessy: We keep hearing that 80% of the cost of manufacturing the board is determined in the design cycle.

Griffin: I agree. In 2012, we acquired Sigrity, a company known for SI and PI. It has been our mission ever since we acquired them to embed those engines into our PCB design tools, both Allegro and OrCAD. Now, inside of Allegro, we have some in-design analysis capabilities that look for impedance discontinuities, nearby signals that are coupled more than others, and it looks at return path quality. All these are using Sigrity engines underneath, but the designer doesn't know it. They say, "Perform an impedance check," and it scans the board and gives them a list of where the outliers are.

We recently announced a new product called Sigrity Aurora, which bridges the gap between the design tool and the ultimate SI and PI analysis that you need for signoff. The difference between Sigrity Aurora and Allegro is that we provide additional workflows that assume the user has some SI and/or PI experience. The user is going to ensure that drivers and receivers have IBIS models assigned and that for PI, our PowerTree utility is applied to assign all the voltage sources and sinks so the user can run AC and DC analysis. The same Sigrity engines embedded into Allegro for impedance and coupling screening are now available for traditional SI and PI analysis in Aurora on top of the Allegro user experience. You're adding another layer of sophistication onto that level of analysis. In addition, we have made it a seamless transition to the advanced SI or the advanced PI analysis using the same engines and models. It's a nice, continuous flow.

Shaughnessy: Is it always running in the background, or is it on-demand?

Griffin: So far, our strategy is to make it on-demand. With all the things that they have to do with area fill checks and changing shapes, we don't want to steal any of that CPU power that they need. We have an on-demand check to use when they're ready and think, "Let me go do an impedance check before I get laughed at by the SI expert. Oh, I see a bunch of things I can fix." It's meant to be a useful tool to reduce iterations but not take any power away from the layout tool.

Shaughnessy: How do you get designers to use the new functionality? Some of them are so old-fashioned; they would rather take longer to hand-route a design than use an autorouter. It's like they're proud of doing things the old way.

Griffin: My perception is that when I do speak to PCB designers, they fit into one of two categories. One, they've been running Allegro for 25 years, and they're not going to change. They know every feature in it. You give them a new feature, and they say, "No, I'm good with what I have." But there's a new, younger class coming in because a lot of those designers are retiring. But the younger ones are used to apps on their cellphones, and they want things to be much more push-button. Honestly, they're probably looking at what we've done with in-design analysis, where they want it to run in the background. We're in that transition stage right now, where we're serving both the hard and true diehards out there and the new people coming on board.

Shaughnessy: Recently, we've asked designers if they have any idea how much each design costs and what the total cost of a design is. Some of the managers say, "We know how many hours we spent on it." You all know who your users are; do they track the average cost of a design?

I-Connect007 editor Andy Shaughnessy (right) talks with Brad Griffin of Cadence.

Griffin: That's a big thing that's happening in PCB design right now. Again, it's not necessarily my area of expertise, meaning the product lifecycle management tools, where they're checking the work in process, and managers have a dashboard so that they can see how much time people are spending and what parts they're choosing. Are they choosing the most cost-effective parts? There's a lot of tie-backs into corporate databases. Look at materials. A lot of engineers at DesignCon will have to make tough decisions. If they're going to go to 56G or 112G, what materials do they need to use? Some of the costs of advanced materials are significantly more expensive. Do you need those materials, or can you get by with something cheaper?

That's another area where design for profitability comes into play: when you want to use the lowest-cost materials, but you still want to be on the leading edge because you can't be at a competitive disadvantage where your competitors are going twice as fast as you. Your SI expert has the expertise to look at materials and look at signal quality with a less expensive choice. They can make all those trade-offs and say, "I've found some ways that we could reduce the cost of this board by five bucks." They're going to produce a million of them, so that makes a big difference.

Shaughnessy: Are your customers asking you specifically for more cost-aware design functions, or do they want more data up-front in the design process, which can wind up helping them save time and thus cut costs?

Griffin: Yes. Here's another example. We have this technology called PowerTree; it's a technology that we brought to market originally after working with Cisco. The people who created the schematic didn't know how many decoupling capacitors they were going to need. Thus, they would spray a bunch of decoupling capacitors down on the design and wouldn't necessarily make it easy to figure out which component the decoupling capacitors were associated with. Another big issue was that sometimes you're starting with one voltage, but then you have to break that voltage down to meet all the requirements of all the different components.

Now, if you do that in any design tool and go through a filter component, what ends up happening is those nets on the output of the filter may be named all by the tool, not by the designer. But those nets are important nets that you have to analyze if you're a PI engineer. The people at Cisco spent so much time at the end of the design identifying all of the nets they need to analyze before running PI analysis. We said, "Okay, let's fix this problem because we have the schematic, the layout, and the analysis tools." We put this feature called PowerTree upfront. Now, at the schematic level, they can trace out the source to every component that consumes power and see how the voltage is getting broken down.

PowerTree provides a graphical visualization of each power path, plus it captures the names of all those internally named nets. We have all that setup information. With the PowerTree, anyone at any point in the design cycle can just apply the PowerTree, and everything is set up for PI analysis. You can run an analysis from the schematic. While that has limited value because you have no metal, you can make sure that all of the setup is there. Later in the design, instead of spending days trying to set up for analysis, the process is in place to just apply the PowerTree and run the analysis. It saves a lot of time and energy.

Shaughnessy: A few days here and there, and pretty soon you're talking about serious time and money saved.

Griffin: Exactly. It's so competitive. You give up any possibility of being efficient if you say, "This is the old way that we've always done it." We owe it to our customers to make sure that we're providing them the different levels of innovation that can become more and more automated. In EDA, the "A" is for automation, right? We need to provide the automation to make that process easier. We're bringing all of this together, starting from the silicon and going through the whole system. Again, we owe it to our customers to make their process more efficient, which saves them time and money.

Shaughnessy: Very good. Thanks for speaking with me, Brad.

Griffin: I enjoyed it. Thanks. DESIGN007

MIT President Reif Testifies Before Congress on U.S. Competitiveness

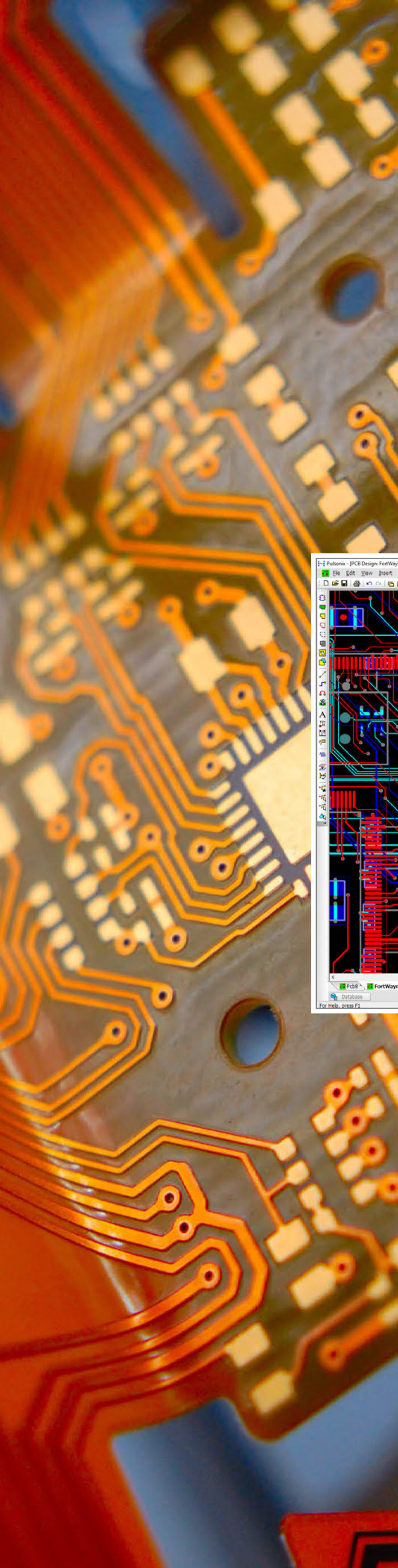
No U.S. strategy to respond to competition from China will succeed unless it includes increased investment in research, a concerted effort to attract more students to key research fields, and a more creative approach to turning ideas into commercial products, MIT President L. Rafael Reif said in congressional testimony on February 26.

Reif spoke at a hearing of the House Ways and Means Committee on U.S.-China trade and competition. "Whatever else the U.S. does to counter the challenges posed by China, we must increase our investment in research in key technology areas, and we must enhance our capacity to get the most out of that investment," he told the panel. "U.S. strategy is unlikely to succeed if it is merely defensive; to stay ahead, the U.S. needs to do more to capitalize on our own strengths."

Reif's Capitol Hill appearance came immediately after he delivered an opening talk at a National Academy of Sciences (NAS) event, commemorating the 75th anniversary of "Science: The Endless Frontier," a 1945 report to U.S. President Harry S. Truman that is seen as the founding document of the post-World War II research system in the U.S. The report was written by the late Vannevar Bush, who had a long career at MIT, including service as the Institute's VP and dean of engineering.

At both the NAS and on Capitol Hill, Reif called for a "visible, focused, and sustained" federal program that would increase funding for research and target the increase at key technologies, such as AI, quantum computing, and advanced communications. "The U.S. lacks an effective, coordinated way to target research toward specific areas, and funding has fallen far behind what's needed to stay ahead of our competitors," Reif told Congress.

(Source: MIT News)



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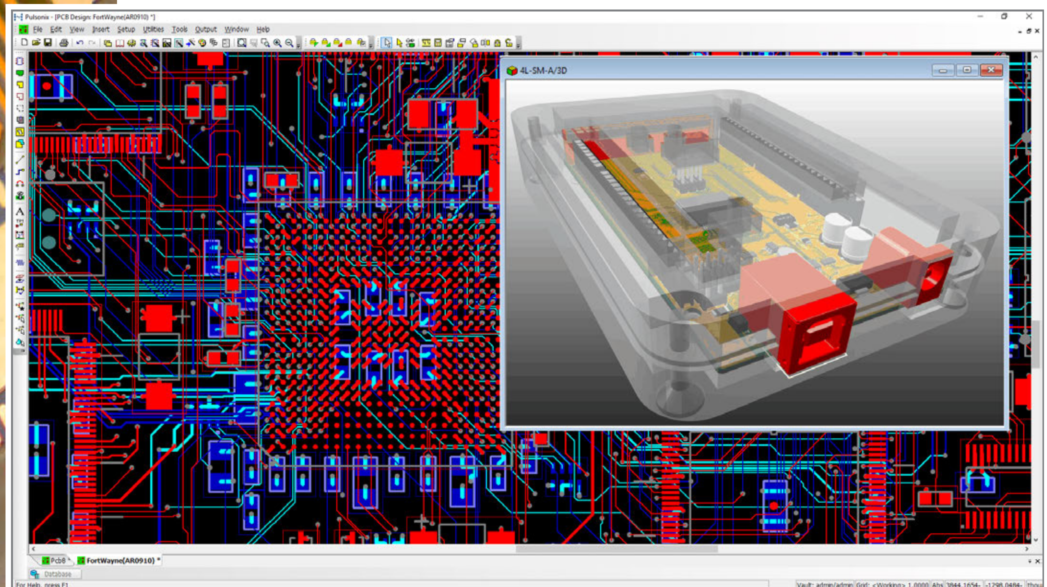

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PCB007 Highlights

I-Connect007 Publishes Third Annual *Show & Tell Magazine* All About IPC APEX EXPO 2020 ▶

This special publication is a supplement to our other monthly magazines and brings you exclusive, in-depth coverage of the recent event. These pages are packed with tons of great content, including event photos, video interviews, attendees' thoughts, reviews from our guest contributors and I-Connect007 editors, interviews with award winners and other industry experts, and coverage of another successful IPC STEM Student Outreach Program.

Punching Out! Down to 199 ▶

According to the database at Tom Kastner's firm, the number of PCB companies in North America is now down to 199. This is a psychologically significant number for the industry. Tom unpacks this number, provides insights on trends, and shares his firm's predictions for the future.

Not All Plating Lines Are Created Equal ▶

Barry Matties and Happy Holden met with CEO Michael Ludy and CMO Sarah Großmann from Ludy, a company specializing in galvanic plating equipment for PCBs. This interview gives an overview of Ludy and its latest advancements in PCB plating equipment.

It's Only Common Sense: Embrace Change, Embrace Success ▶

Oh, that dreaded word "change." Great fortunes have been made in times of great change by those who were flexible enough to adapt. Dan Beaulieu shares six ways that you can inspire change in your own organization from a book by Mac Anderson and Tom Feltenstein.

IPC Honors TTM Technologies Inc. and Continental Automotive With Corporate Recognition Awards ▶

IPC bestowed its highest corporate honors on two IPC member companies: TTM Technologies Inc. and Continental Automotive. During a luncheon at IPC APEX EXPO 2020, the Peter Sarmanian Corporate Recognition Award was presented to TTM Technologies Inc., and the Stan Plzak Corporate Recognition Award was presented to Continental Automotive.

Sunstone Circuits Now Offering ITAR on Limited Review PCBs ▶

Sunstone Circuits, the leading PCB prototype to production solutions provider, announced that ITAR controlled PCB jobs can now be ordered through its "limited review" products (PCBExpress and ValueProto).

Elmatica CEO Approved Member of the Swedish Cyber Defense and Export Control Groups ▶

Elmatica announces that CEO, Didrik Bech, is an approved member of the Swedish Cyber Defense and Export Control Groups.

DuPont and SCHMID Announce Partnership for New PCB Plating Applications ▶

DuPont Electronics & Imaging and SCHMID Group have announced that they have entered into a nonexclusive joint development agreement to explore new PCB plating applications to bring advanced innovations to their global customers. The partnership will benefit high-end PCB manufacturers by delivering next-generation interconnect products and metallization processes that can create faster, smarter, and more reliable devices for the 5G era.

While others struggle just to keep pace, we stay ahead of the curve by constantly investing in the equipment, people and resources needed to be the best total PCB solutions provider in the industry.

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Resins: Five Tips for Potting and Performance

Sensible Design

by Alistair Little, ELECTROLUBE

In recent columns, I have outlined various resin properties and how they relate to particular types of circuit protection, seen how to apply these resins in a production environment by deciding on which mixing and application techniques are appropriate to specific production needs, and explored various resin subtleties, such as how best to achieve a satisfactory cure. Nevertheless, readers continue to ask, "Does thicker coverage achieve better performance? What is the best advice for manual potting? We chose an inappropriate resin, so how will this affect our application?" In this column, I will explore these and other issues based upon frequently asked questions from Electrolube's customers.

In no particular order, here are five questions that raise a number of technical issues allied to resin applications, together with my responses. Hopefully, it will provide useful background information to help you with your own resin-related activities.

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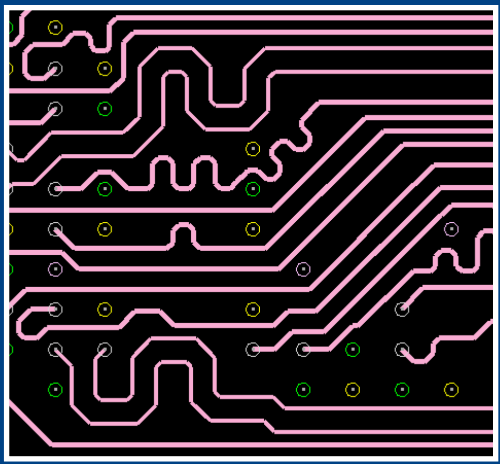
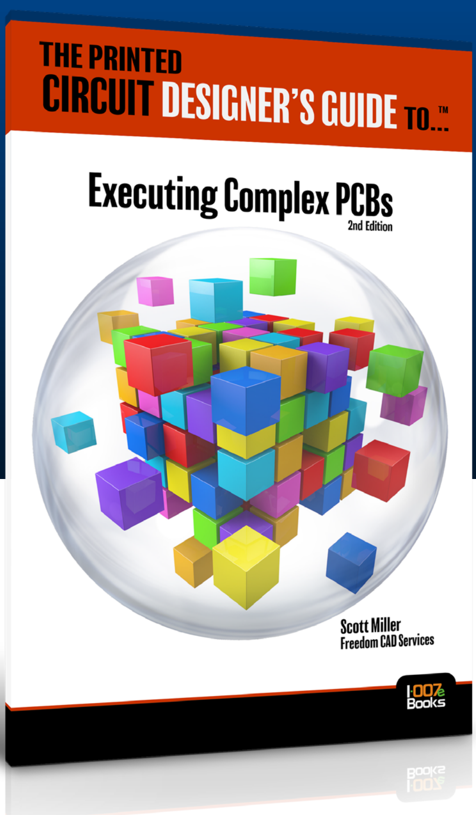
Today's PCB designs require more diligence in order to meet the requirements of today's high-speed microprocessors. At higher data rates, insertion loss becomes more critical. This results in signal length limitations due to insertion loss, very tight impedance matching, short stub lengths and the use of higher performance PCB laminates.





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1. What are some examples of a critical application, and how do these differ from non-critical?

Normally, the phrase "critical application" is used when referring to safety-critical systems. These are applications that will not only seriously impact on the user and their organization but also potentially result in serious environmental damage, injury, or loss of life if they malfunction. Examples of critical applications include aircraft; automotive and railway operating and control systems; emergency lighting; burglar and fire alarm systems; medical equipment required by doctors, nurses, and surgeons; as well as power grid systems and first responder communication systems. Non-critical applications are normally where if a failure occurs, lives are not immediately at risk. If we look at potential malfunctions within automotive applications, the brakes would be considered critical, and climate control would be considered non-critical.

2. I have heard mention of some resins containing glass beads (or similar). Why would these be required and offer some potential applications?

Glass beads are added to resins for a number of different reasons. They can be used as a filler to produce a low density, chemical resistant resin, which is good for weight critical applications. They also control the minimum resin thickness that can be applied. Aesthetically, glass and/or plastic beads can be used to provide a matt surface to resins or, in the case of optically clear resins, a diffused effect when light is passed through. An example is the UR5635 two-part, flexible polyurethane potting compound, which has been formulated to provide a light-diffusing effect for LEDs. It offers a unique light diffusion effect thanks to its cloudy appearance and has been used to great success as an LED potting compound for both decorative and protective applications.

3. What are some key pointers to remember when manually potting?

Think about the amount of resin that you are going to need and across how many units. If there are a large number of units, and a large amount of resin required, it is often better to use a number of small-sized resin packs, as you will have better control over the potting process. If a large resin pack is used, then due to the volume of material, once mixed, the resin will start to cure over a shorter time-scale compared to a small volume pack. Consider where to place the resin so that it can flow around and under the components. With thixotropic resins, it is more critical, as the resin is purposely designed to have a low flow when applied.

4. Does thicker coverage equal better performance?

The simple answer to this is yes. In general, they do perform better; however, there will be a point at which increasing the resin thickness will not offer any significant gain in performance. This heavily depends on the specifics of the application and the resin used. Generally, a thicker resin layer is better if high levels of chemical resistance are required, particularly in the case of long-term immersion or for high voltage systems to increase long-term performance. Considering the variation in height of components on a PCB, the thinnest coating thickness needs to be taken as being representative across the entire unit rather than the average. In the case of physical shock, a thicker layer of resin can help to protect the components and dissipate forces better than a thin layer. The major downside with increasing the resin thickness is the increase in weight and volume occupied by the encapsulated board.

5. What are the potential issues to be faced by selecting an inappropriate resin for a particular application?

Okay, there's no dancing around the issue here; the simple answer is a premature fail-

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ure. Choosing the correct resin is not as easy as it may seem, as there are so many variables to consider, such as typical operating conditions, expected extremes, the size and geometry of the units, the need for repair, the expected service life, etc. If the resin is too brittle, it can crack during operation and expose the electronics to potentially harmful chemicals. If the unit is expected to undergo cyclic thermal shock during its service life, then a flexible resin would be advised, but it depends on the maximum and minimum temperature expected. There is a lot of difference between –60 to +60°C and +40 to +160°C; both are a 120°C temperature difference, but for one, a polyurethane resin would be recommended, while for the other, epoxy would be better.

Conclusion

If ever in doubt, refer to the technical data sheets (TDS); these can be a great help when you embark on a new design or production schedule with new components and resins. However, if you do anticipate any glitches with matching resin types to your production procedures and find it hard to resolve this from the TDS, please contact your supplier's technical support team for further advice. Next time, I will take an in-depth look at some of the most frequently asked questions fielded by our Technical Support Team and explore options to fully address these enquiries. **DESIGN007**

Alistair Little is the global business technical director of the resins division for Electrolube. To read past columns from Electrolube, click here. Download your free copy of Electrolube's book, *The Printed Circuit Assembler's Guide to... Conformal Coatings for Harsh Environments,* and watch their micro webinar series, "Coatings Uncoated".

IPC Design: The Newly Launched Program

Judy Warner gets the update on IPC Design, the newly launched program, from Teresa Rowe and Patrick Crawford. They also discuss the impact on designers, the scope and cost of the program, how it will work, and where you can get more information. **Click image to view video.**

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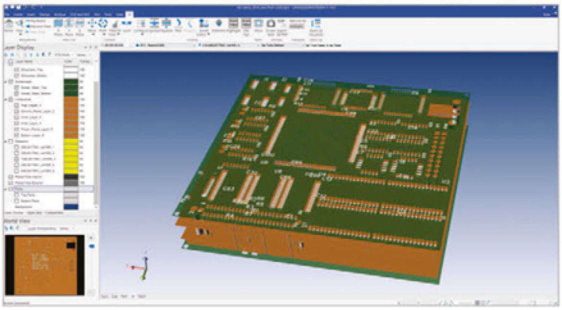

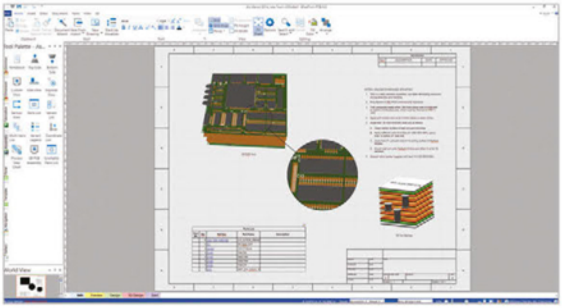

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MilAero007 Highlights

Burt Rutan's Keynote: SpaceShipOne ▶

In this video clip from his presentation, Burt Rutan discusses some of his aircraft's revolutionary flights that drew the most public attention, including SpaceShipOne, which flew three of the five manned space flights launched by man in 2004. He also explains the benefits of working with Microsoft's Paul Allen, who agreed to fund SpaceShipOne based on a simple handshake.

Defense Speak Interpreted: The Missile Defense Agency ▶

The Missile Defense Agency (MDA) has its roots in the Strategic Defense Initiative (SDI), known as "Star Wars" in the 1980s, as proposed by President Ronald Reagan. In this column, Denny Fritz provides an overview of how the MDA operates and describes types of missiles and phases.

What It Takes to Be a Milaero Supplier, Part 1 ▶

The decision to pursue military and aerospace (milaero) certification impacts every facet of the organization, and not every shop is prepared to make this transformation. This is the first article in a four-part series, breaking down what it takes in sales and customer service, engineering and CAM, purchasing and quality, and manufacturing. Anaya Vardya starts by exploring sales and customer service.

DOD Releases Fiscal Year 2021 Budget Proposal ▶

On February 10, 2020, President Donald J. Trump sent Congress a proposed fiscal year 2021 budget request of $740.5 billion for national security, $705.4 billion of which is for the Department of Defense (DoD).

Bell Textron Teams up With Sumitomo Corporation and Japan Airlines to Explore Air Mobility ▶

Bell Textron Inc., a Textron Inc. company, announced a signed memorandum of understanding with Sumitomo Corporation and Japan Airlines Co. Ltd. to explore mobility-as-a-service (MaaS) and foster the required infrastructure and regulatory environment.

Parrot Chosen by the Swiss ARMY for the Supply of Micro-drones ▶

Parrot, Europe's leading drone Group, has been chosen to equip the Swiss Armed Forces with micro-drones as part of the Swiss Mini UAV Program (Swiss MUAS) call for tender against major civilian UAV players.

BAE Systems Wins Two Awards to Support the U.S. Navy with Enhanced Radio Communications and C5ISR Capabilities ▶

The U.S. Navy's Naval Air Warfare Center Aircraft Division has awarded BAE Systems Inc. a prime position on a $212 million contract to integrate and sustain its critical communication systems. The company will design, acquire, integrate, and test radio systems for newly constructed guided-missile destroyers (DDG) and other U.S. Navy and U.S. Coast Guard ships.

DARPA Selects Aerojet Rocketdyne to Develop Propulsion Technology for the Hypersonic Defense Program Glide Breaker ▶

Aerojet Rocketdyne has been awarded a contract worth up to $19.6 million by the Defense Advanced Research Projects Agency (DARPA) to develop enabling technologies for an advanced hypersonic defense interceptor known as Glide Breaker.

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Carey Burkett

Flexible Circuit Technologies: 'We Do it All'

Flex007 Interview by Dan Beaulieu

During IPC APEX EXPO 2020 in San Diego, Carey Burkett, VP of Flexible Circuit Technologies, sat down for an interview with Dan Beaulieu. The two discussed the company's expansive growth, the current flex and rigid-flex landscape, and FCT's drive to provide complete solutions from rigid and flex circuits through box build.

Dan Beaulieu: Good morning. Today, I'm pleased to talk to my friend Carey Burkett from Flexible Circuit Technologies in Minneapolis, Minnesota. Carey, thanks for being with me today.

Carey Burkett: Thanks for having me, Dan.

Beaulieu: This is a very interesting company that I've gotten to know in the last few months and one of the fast-growing success stories in North America. You're a global company; I want to learn a little more about that. Carey, what can you tell me about your company?

Burkett: First of all, Flexible Circuit Technologies is a supplier of flexible circuits, rigid-flex, flexible heaters, and membrane switches, and then we also do specialized EMS assembly services all the way to complete box builds. We do it all.

Beaulieu: Is it true that your company started out doing just flexible circuits?

Burkett: Yes. In fact, that's very important in today's marketplace. Flex and rigid-flex are growing extremely rapidly. Engineers are being forced into those technologies due to a wide array of topics, whether it's miniaturization,

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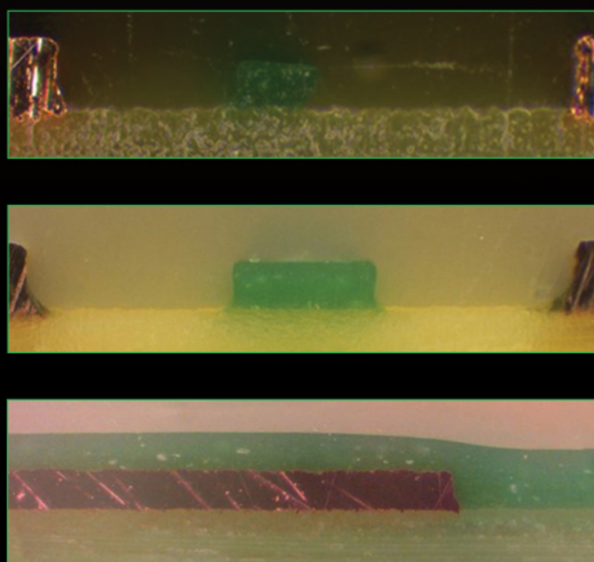

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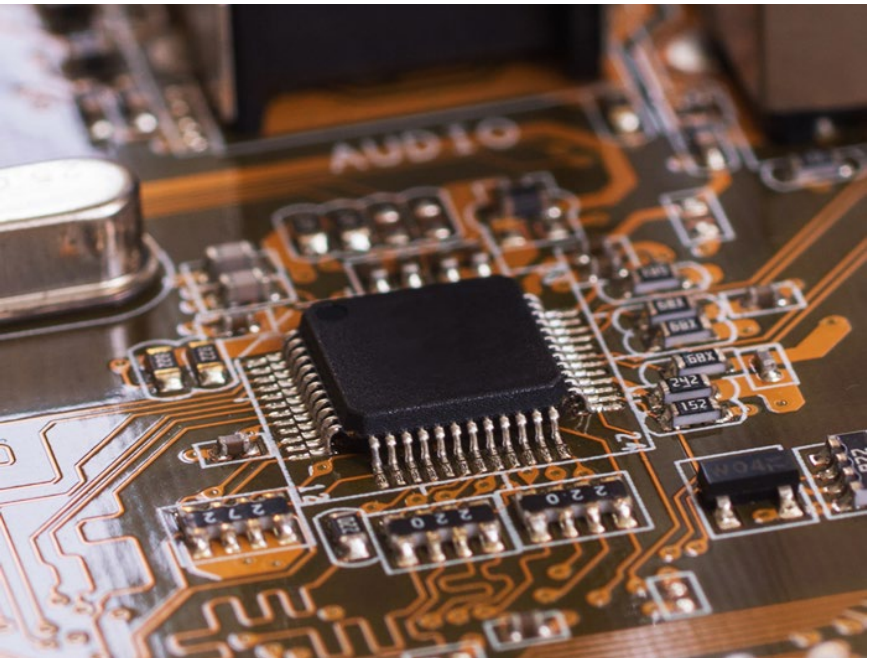

mobility, or connectivity. There are all kinds of reasons. Engineers across all markets are being driven to flexible solutions. One of the things that's interesting is that it's growing so rapidly that there are many new entrants into that market. Unfortunately, there's a lack of true design talent in the industry.

Beaulieu: Correct. That's a fact.

Burkett: One of the things that is unique about us is the application engineering support that we provide to our customers. We're led by Mark Finstad. Mark co-chairs the IPC Flex Circuit 2223 Design Committee. He's well known and the lead educator, along with another gentleman, at IPC events. Mark is also a noted columnist and one of the foremost experts on the globe, and yet it's not just Mark. Our entire team of application engineers offers from 25 to 35 years of experience in designing flex and rigid-flex. It's so important in helping customers get to cost-effective designs that are going to perform within the challenging applications that these circuits are typically used in.

Beaulieu: To talk to the audience a little bit, I've been doing this for a long time, and I can remember when there were only a handful of companies in the United States that did flex, particularly rigid-flex, when you get into bookbinders and stuff. And there's been a rejuvenation in the last few years in the United States to the point where there are better flex products. I talked to designers 10 years ago who didn't even want to design it in, even in applications where flex should be, like in automobiles. They didn't even want to put it in because it was too hard to buy, or it was too hard to find. You have changed that, but what I find intriguing is that you do it all.

Burkett: When you look at the customers or OEMs today, one of the challenges has to do with the overall supply chain. You're trying to manage this massive supply chain. Often, they were set up at one time—maybe they were transactional relationships; today, we're seeing most customers want more. They want partnerships and suppliers that can take on more. And when you look at the advent of the growth of CMs and EMS companies, they do a great job in supporting customers.

We have responded. We started with flex, rigid-flex, and shipping. Bare boards led us to assembly, so we're shipping assemblies. Now, we've moved on all the way to complete box builds. Probably the unique thing about us is that when you look at a CM, they're almost like the general contractor. They're getting components and parts from everybody to put this product together.

But with us, we're starting with the heart of the product. Typically, that's going to be the circuit board or the flex circuit. We're using design experts to get a cost-effective solution so we can get high yields. We can perform the EMS, and we're specialized in that area. Often, EMS companies are used to placing components on rigid boards. To do that on flex takes different techniques, special fixturing, and a lot of special knowhow to be proficient at it. We're experts at assembling flex, and that's very important.

Beaulieu: You're providing what I would call a synergistic smooth solution with all three genres of design, fabrication, and assembly, all the way to box build, which is critical. I've worked with both assembly companies and board shops for a long time. That way, the designers think of the fabrication, and the fabricators think of the assembly, so it works together as one smooth process. Companies are looking for that. In the old days, they were OEMs and had us there. They did it themselves. Now, they look for us for development, like your company.

Burkett: Exactly, and we always say we're customer-driven. That's very important. It started with flex and building our expertise there. We have done that for many years. Then, we got into the assembly side of this. But once you're building assemblies now to get to a box build, it's like, "What's the housing? What does this need to go into?" Packaging and all of our production are Asia-based, but we have the medical ISO 13485 certification and automotive certification. Also, our box builds are FDA registered.

When you're doing those types of box builds, you're talking about having robust quality systems in place and the traceability that's required. The other thing is we do work with a lot of CMs and EMS customers. The fact that we have expertise in this arena helps us better serve them because we know the issues and challenges that they deal with in dealing with flex and doing assembly with flex.

Beaulieu: They need your intelligence. Also, although you're a global company, the "brain trust" is in Minneapolis.

Burkett: Minneapolis is our headquarters, and out of there, we support our U.S.-based and European customers with high-end application engineering support, helping with the design. We have our program managers, and customer support resources are there. We're the ones helping manage the process and working with our company, doing the communications, and leading the prototyping efforts. Once we go

into production, there are different ways. We have a production blanket team that will manage that process with a customer. We also have inventory, stocking programs, and warehousing to help make sure that we can take care of the customers, including just-in-time manufacturing.

Beaulieu: You offer a global solution with the ease of working with a domestic source.

Burkett: Exactly.

Beaulieu: How is the show going for you so far?

Burkett: The show has been good. It's a great venue. Everybody in the industry is at the show.

Beaulieu: One last thing as we wrap up. How do people get a hold of you?

Burkett: They can go to our website at flexiblecircuit.com or call us directly.

Beaulieu: Carey, thanks for being with me today. I appreciate it.

Burkett: Thank you, Dan. **FLEX007**

Click here to watch the full video.

Flex007 Highlights

American Standard Now Offers Bookbinder Rigid-flex PCBs ▶

American Standard Circuits is now offering high-technology bookbinder rigid-flex PCBs. Bookbinder rigid-flex technology is a special rigid-flex design where the outer flex layers are increased in length, compared with the inner layers, by enough to keep them from interfering with each other and buckling.

Catching up With Flexible Circuit Technologies ▶

Dan Beaulieu catches up with Troy Koopman, president and co-founder of Flexible Circuit Technologies (FCT), and Carey Burkett, the company's VP of business development. FCT is a full-service flex and rigid-flex supplier.

Flex Talk: Additive PCB Technology for Next-generation Electronics ▶

Semi-additive PCB processes help to enable very fine features, with trace and space down to 25 microns and below, significantly reducing space and weight for next-generation electronics. Tara Dunn speaks with Todd Brassard and Meredith LaBeau from Calumet Electronics about how the company is the first domestic PCB manufacturer to license Averatek's A-SAP™ process and will be presenting information on the industrialization of this process at this year's IPC APEX EXPO.

Flexible Printed Circuit Boards Market—2026: Industry Growth, Opportunities, Applications, Trends, and Revenue Strategies ▶

FPCBs are widely used across applications, such as LCD displays, mobile screens, connectivity antennas, and flexible circuitry used in rechargeable batteries. The growth in the demand for consumer electronic goods, the increase in the popularity of Internet of Things (IoT), and the adoption of FPCBs in automotive applications drive market growth.

SEMI-FlexTech Launches Six New Projects to Accelerate Flexible Hybrid Electronics Innovation ▶

SEMI-FlexTech announced the launch of six projects to accelerate sensor and sensor system innovations for new applications in industries including healthcare, automotive, industrial, and defense. In collaboration with the U.S. Army Research Laboratory (ARL), FlexTech, a SEMI Strategic Association Partner, will provide more than $2.3 million in funding for the projects aimed at maturing the flexible-hybrid electronics (FHE) technology ecosystem.

HON-Flex Selects MKS Flex PCB Laser Processing Solution ▶

MKS Instruments has announced that HON-Flex Xiamen Hongxin Electron-tech Co. Ltd. (also known as HON-Flex) has selected the ESI RedStone system for its high-volume flex PCB processing. The ESI RedStone system provides HON-Flex with the capability to deliver high-volume processing of through vias, with the added versatility to address their requirement for blind via processing.

NextFlex Honored With FLEXI Award for Its FlexPro Professional Development Education Program ▶

NextFlex, America's Flexible Hybrid Electronics (FHE) Manufacturing Institute, was awarded the FLEXI Technology Leadership in Education Award for its FlexPro program yesterday at the SEMI Flex Conference in San Jose, California.

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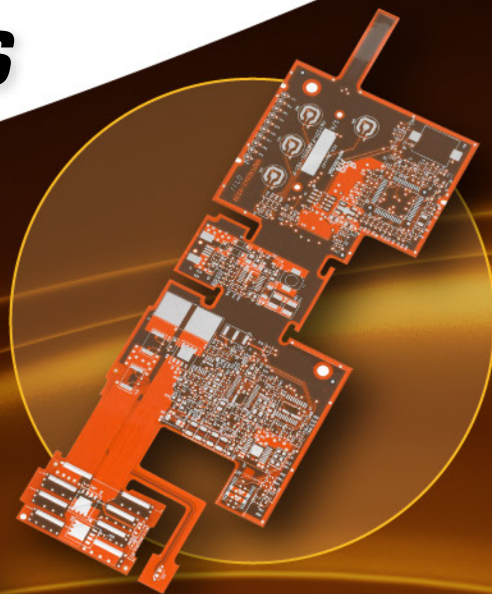

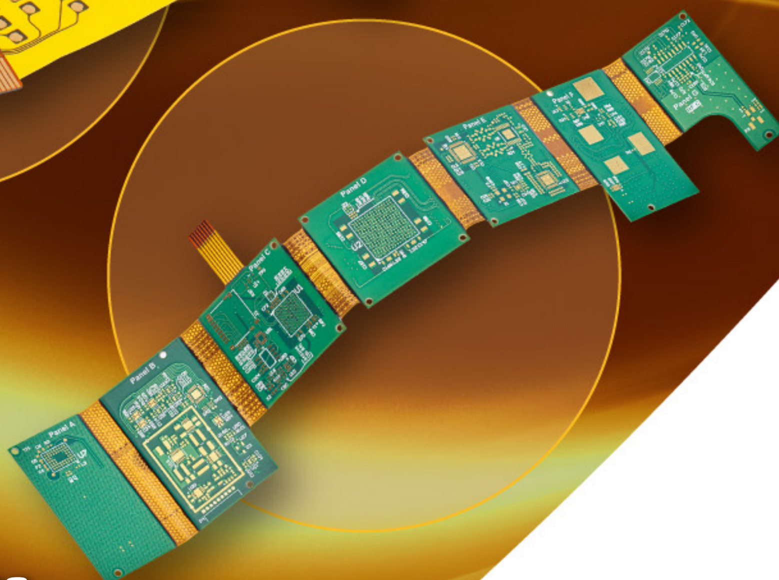

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Profitability: A Vital Design Requirement

Flexible Thinking

by Joe Fjelstad, VERDANT ELECTRONICS

Designers have, from the earliest days of the printed circuit industry, been under-appreciated. PCB designs were typically simple, single metal layer affairs, and design activities were considered a mundane (and even boring) task of "connecting the dots;" thus, they were given little respect.

Much has changed over the years, as integrated circuit technology has advanced, and data rates and processor speeds have climbed. Over recent years, I have found myself often saying that designers are arguably the most important people in the development of electronic products. The decisions they make will impact virtually every manufacturing step in the fabrication and assembly of electronics products. The designer's role is so vital that, over the years, multiple touchstone guidelines have been added to the mix that seek to address myriad concerns that are all part of meeting the goal of producing the best possible products.

"Design for" Guidelines

The first order of concern for any design is that it simply meets the functional goals of the product. This can be accomplished in many ways, but beyond clearing the bar of "Does the product work?" there are many other litmus tests that are being more frequently applied to the evaluation of a completed design. These include design for manufacturing (DFM), design for assembly (DFA), design for testing (DFT), design for the environment (DFE), design for reliability (DFR), design for excellence (DFX), and there are doubtless other "design for" guidelines for other aspects that are deemed important to an individual types of products. All these guidelines provide important considerations relative to the product design in review. When applied, all of these "design for" guidelines combine to create products that can be made both reliably and profitably.

Designing for Profitability (DFP)

Good product design is arguably the cornerstone of every profitable product. Make a product that results in a loss or less than optimal return, and you are either headed for bankruptcy or irrelevance. It is possible to make unprofitable products as one climbs the learning curve or to gain or control market share (many governments subsidize products for this purpose). However, you must nevertheless offer the user

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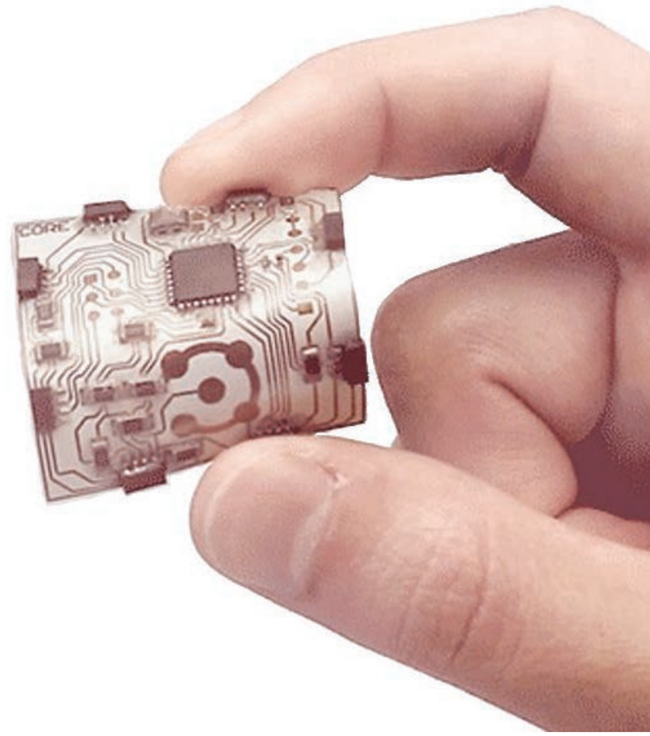

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In this regard, it is important that designers work collaboratively with those who will be tasked with manufacturing their designs. Too often, designers work in isolation and do not have a full appreciation of the impact of the choices they make. The products they design are fabulously innovative, but if they cannot be built, and built profitably, what value is there in their effort?

Engage Others in the Design Process Early

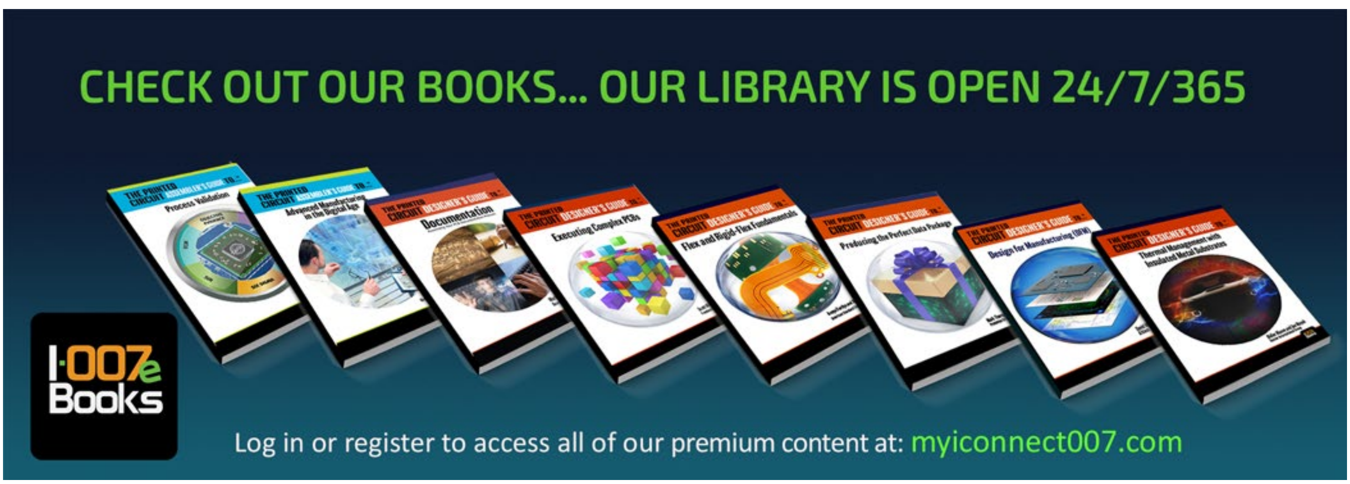
How do we overcome this? Make sure all stakeholders involved in the manufacturing and testing of the product have input. Such input need not be tapped for every new design if the design is very similar to a past product design, but it does not hurt to have a checklist similar to that used by pilots before every flight. It may seem unnecessary, but an experienced pilot only needs to miss one item on the checklist to cause a potential disaster. "Design for" guidelines can help one to create such a checklist to ensure profitability.

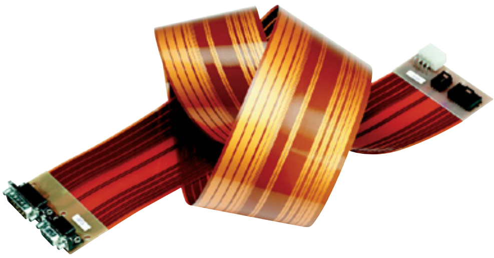
Finally, there is a need to make sure that the guidelines are followed. Societies have laws and rules for numerous reasons, but perhaps the most important is that they provide for the continuity of the societies themselves. (If not for traffic lights and stop signs, we would likely need to have either hospitals or cemeteries at every intersection.) Guidelines are different than laws, but the impact of not having them could be similarly troublesome. However, rather than a stringent set of dos and don'ts, allow some discretion, depending on the product and its application. Advances in technology and innovation could be stifled if the designer is not allowed to explore the limits from time to time.

Summary

Designers are definitely "at the controls" at the beginning of every new product launch. Their decisions will impact everything that follows their efforts, including the ultimate profitability of the final product. The use of established "design for" guidelines will serve them well in their work to ensure a smooth transition from concept to product and the future well-being of their company, client, or customer. As I have found myself saying with ever-greater frequency in recent years, we must all first do the right things, and then do those things right. It all begins with design. **FLEX007**

Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185 patents issued or pending. To read past columns or contact Fjelstad, click here.





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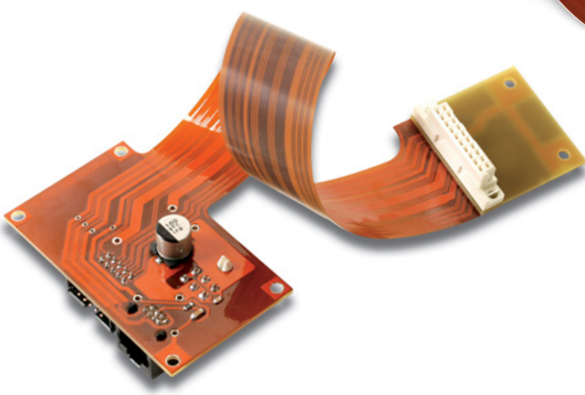

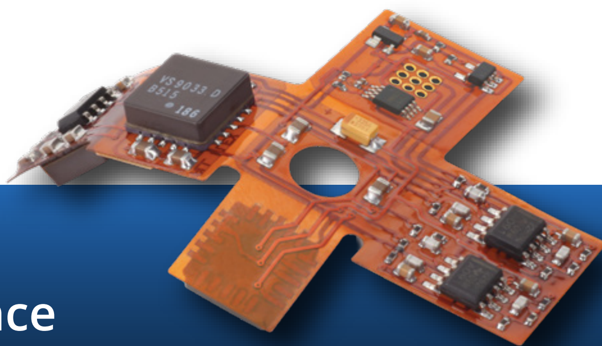

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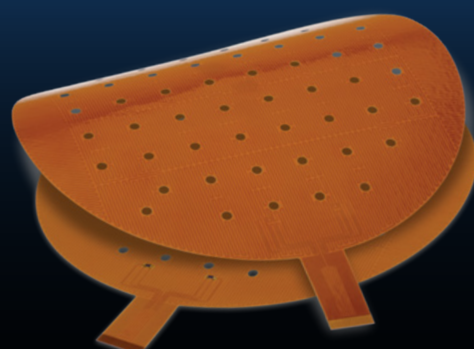

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Are You Unintentionally Adding Cost?

Flex Talk

by Tara Dunn, OMNI PCB

Nobody designs a PCB, rigid or flex, without regard to cost. There is a continuing series of choices and trade-offs, some with greater cost impact than others. That topic alone could easily fill an entire issue of this magazine. For this specific column, let's focus on flex and rigid-flex and discuss a few things that can easily be overlooked when putting together the puzzle pieces of a design and that may have an unintended impact on the overall cost.

Size

The cost of a flex or rigid-flex board is a derivative of the overall panel cost. Fabricators use varying panel sizes, with the most common panel sizes being 12" x 18" and 18 x 24". Piece price is the panel price divided by the number of parts manufactured on that panel. Manufacturing processes require a 1" border on the outside of the panel, leaving 10" x 16" and 16" x 24" of usable space. This is fairly straightforward in rigid designs. Most are squares or rectangles.

Flex designs, on the other hand, often have unusual shapes, and how those shapes are "nested" on the production panel can have a big impact on cost. Most often, if you are requesting a flex as a single piece, your fabricator will place the parts on the panel in the most cost-effective manner. Arrays can be much trickier and present an opportunity for unintentionally increasing the cost. For example, a flex shaped like a "T" or and "L" are prime candidates to "reverse nest" on the panel and flip parts around to better utilize the space. With an array, it may not be ideal to "reverse nest" for assembly reasons, and a fabricator is less likely to employ this strategy. It is highly recommended that you engage with your fabricator early in the process to discuss how to best utilize the production panel and drive out unnecessary costs.

Another example is the overall length. Many flexible circuits are designed with a service loop. Depending on size, even 0.250" can make


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a significant impact and result in a reduction in the number of parts per production panel. A flex design that is 4.1" in length can be significantly more expensive than a flex that is 3.8" in length. That is a generalization and depends on other factors of the overall size, but the takeaway is to always keep your fabricator's panel sizes in mind and, if given the opportunity, best utilize the production panel to reduce cost.

Materials

When looking at trade-offs and decisions, materials can fit squarely in that category. Sometimes, there is no choice; a certain dielectric type, dielectric thickness, or copper thickness is required. These requirements may lead to minimum lot costs for your fabricator, driving up overall cost and often also driving leadtime. But, if there is flexibility in material selection, it is recommended to work with your fabricator for the stack-up. Giving the fabricator the ability to use commonly stocked materials will keep materials cost as economical as possible.

Flex With Stiffener vs. Rigid-flex

The terminology for these two products is often confused. Using FR-4 stiffeners to support a heavy component or dense area of components on a flexible circuit is highly recommended. This provides mechanical support for the component but does not require an electrical connection between the flex and FR-4 layers. Meanwhile, rigid-flex also provides support for dense component areas, but most often also has routing layers in those FR-4 layers and requires an electrical connection between all layers.

Rigid-flex construction requires a much more complex fabrication process and will be more expensive. This is often necessary, especially if there are dense component areas on both sides of the circuit, and can resolve complex routing and packaging challenges. However, it is worth reviewing to be sure that flex with a stiffener approach will not suffice before beginning a rigid-flex construction.

Technology Roadmap

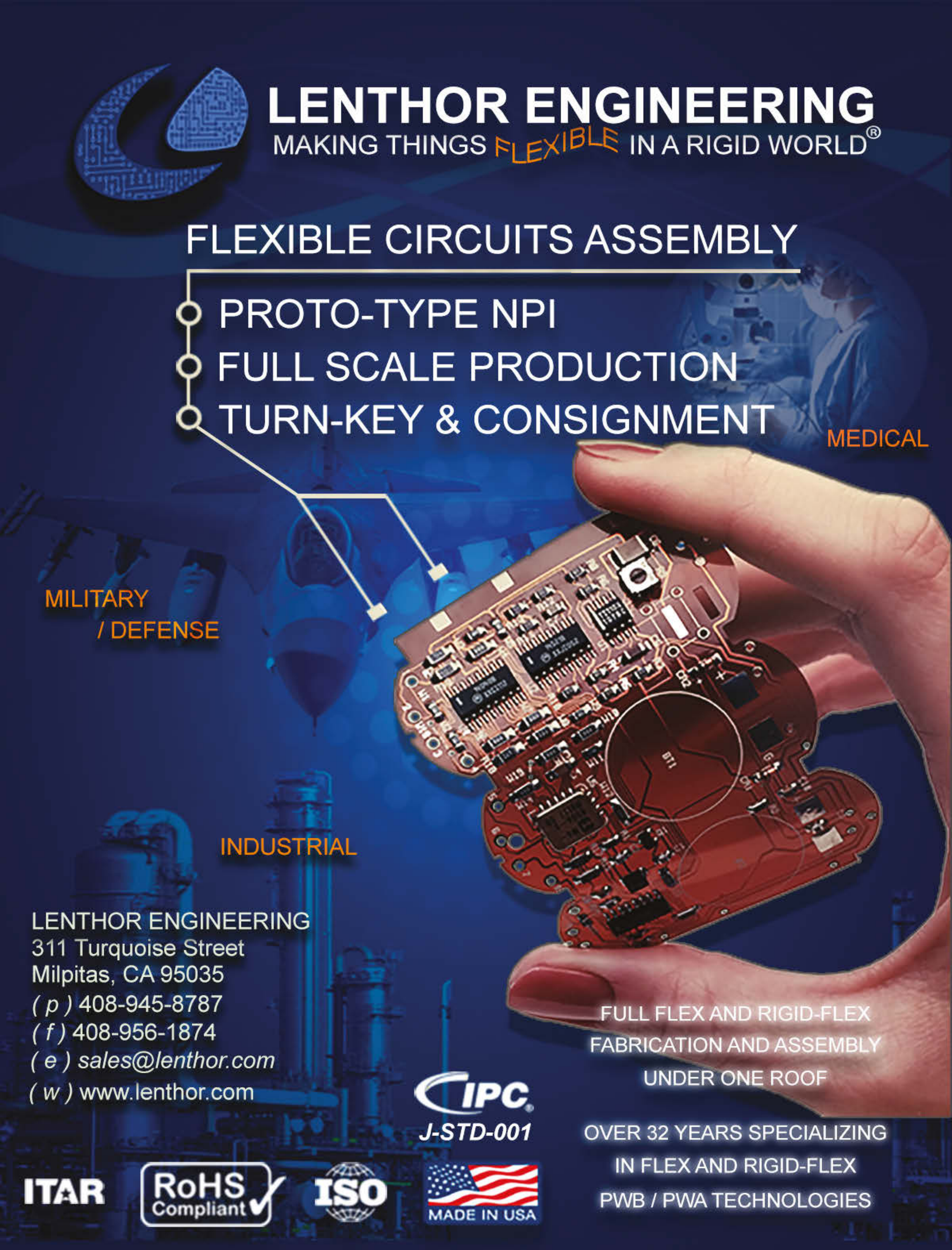
Understanding your fabricator's technology roadmap is extremely important when looking for ways to be as cost-effective as possible with flex design. Typical technology roadmaps have categories for standard, advanced, and emerging technology. It stands to reason that if standard technology costs less than advanced, and advanced costs less than emerging, common sense would dictate designing to your best ability within the standard category. It also stands to reason that as a design attribute moves along the continuum, there will be associated yield impacts and increased costs.

What may not be so intuitive is that when a design pushes multiple areas of technology, the yield loss, and associated cost impact can be exponential. The phrase "everything but the kitchen sink" is not a good thing with flex design, at least in terms of pricing. It is fine to push the limits of trace width and space, the hole size, or the drill-to-copper distance, but pushing all of these in one design will certainly increase the cost. It is recommended to work closely with your fabricator to help navigate the trade-offs and yield impacts to be certain that the impacts of pushing the limits in the design are fully understood, especially with flexible materials.

Conclusion

This list is by no means intended to be an all-inclusive discussion of items to be aware of when trying to navigate the cost impacts of the many design challenges and trade-offs, but I hope this will be a place to start. As is often recommended, the common theme with flex and rigid-flex is to work with your fabricator early in the design; take advantage of their expertise because they are always willing to support their customers and share their knowledge. **FLEX007**

Tara Dunn is the president of Omni PCB, a manufacturer's rep firm specializing in the PCB industry. To read past columns or contact Dunn, click here.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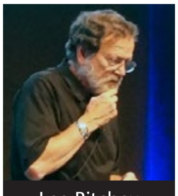
1 Avoiding EMI Problems With Lee Ritchey ▶

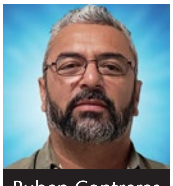

Lee Ritchey

The I-Connect007 team met with design expert Lee Ritchey to pick his brain on EMI problems and what can be done to minimize them. Lee explains the issues are almost always tied to power delivery, as well as the abundant amount of misinformation surrounding this topic.

2 Eric Bogatin Looks at EMI Root Causes and Solutions ▶

The I-Connect007 team recently spoke with design instructor and author Eric Bogatin about the EMI challenges facing PCB designers today. Eric is a "signal integrity evangelist" with Teledyne LeCroy, as well as an adjunct professor at the University of Colorado Boulder and the technical editor of the Signal Integrity Journal. In this interview, Eric explains why EMI is so prevalent and what designers and design engineers can do to avoid EMI from the start.

3 Fresh PCB Concepts: Controlled Impedance—Design to Testing ▶

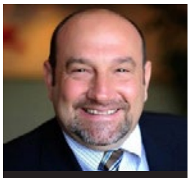

Ruben Contreras

Ruben Contreras often gets questions from customers on one of his favorite subjects in PCB design: controlled impedance. Ruben explains how controlled impedance is a science, which is why he likes it; therefore, it must be designed and tested comprehensively.

4 Connect the Dots: Design Tips For Layout ▶

As a PCB manufacturer, Sunstone Circuits receives hundreds of PCB layouts represented in Gerber format every week. As you might expect, they're not all created equal. Some of the layouts check every box and roll straight into manufacturing, while others need work before they can be sent to the production floor. Bob Tise and Matt Stevenson share some best practices.

5 Insulectro: Educating Designers About High-Speed Materials ▸


Ken Parent

In this video interview from IPC APEX EXPO 2020, Ken Parent, Insulectro's VP of sales and product manager, speaks with Kelly Dack about the company's efforts to educate engineers and designers about materials and their options and availability. Insulectro has held a series of PCB design classes and plans to keep educating designers about these high-speed materials.

6 Altium Accelerates IoT and AI Hardware Development through Geppetto and Seeed Collaboration ▸

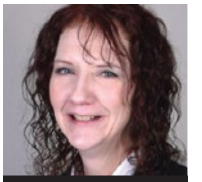
Altium announces that Seeed, the IoT hardware enabler, has embedded the Geppetto electronic design application into its Seeed platform. Seeed users can now go straight from creating a design to manufacturing a working PCB in just one session.

7 Elementary, Mr. Watson: Eating the Elephants of Your PCB Design ▸


John Watson

After being in the PCB industry for 20 years, John Watson, CID, has had the opportunity to work with some of the best PCB designers and engineers in the field. He shares some of the traits PCB designers need, and how you can implement them into your design process to become a great designer.

8 IPC Designers Council Has a New Name: IPC Design ▸


Teresa Rowe

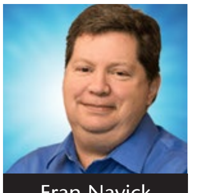
Yes, you read that right. The IPC Designers Council is now known as IPC Design. Many of you have heard secondhand stories about what this change will entail, so Andy Shaughnessy asked IPC to shed some light on this subject. He recently spoke with IPC's Teresa Rowe and Patrick Crawford about what's changing, what's not, and IPC's plans to provide improved infrastructure for PCB design content and curriculum.

9 Joe Clark Says DownStream Is Ready for More Growth in 2020 ▸


Joe Clark

Joe Clark, co-founder of DownStream Technologies, gives Kelly Dack an overview of the company and their innovative product line, which serves to smooth the bumps that can occur between source design output and manufacturing line input. As Joe explains, 2019 was a great year for the company, and he expects that trend to hold through 2020.

10 Global Technology: The Importance of Laminate CTE in PCB Design ▸


Eran Navick

All material expands and contracts with temperature change, which is called the coefficient of thermal expansion (CTE). Eran Navick explains where and how the laminate expands effects the operation of the printed circuit in different ways.

PCBDesign007.com for the latest circuit design news and information.
Flex007.com focuses on the rapidly growing flexible and rigid-flex circuit market.

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- Working knowledge of PADS, Altium, Cadence, Genesis, CAM 350, impedance modeling, SPICE, and thermal modeling tools
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- Maintenance and scheduling of calibrations.
- Be a liaison to our facility in India regarding customer related issues.
- Customer contact with RMA and corrective action.

Process/Quality Engineer
- Develop and document new processes and technologies.
- Review existing processes for improvement opportunities.
- Assist in identifying and addressing manufacturing issues.
- ISO internal auditing and process related audits.
- Set-up and monitor process controls through manufacturing.
- Maintain regulator compliances.

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- Strong follow-through skills
- Grammar and editing skills
- Knowledge of basic photo editing
- Knowledge of HTML a plus

Attitude

- Ability to work remotely, often with only "virtual" supervision.
- Discipline to keep regular hours, communicate with team and deliver on deadline.
- Curious, investigative nature and interest in technology.

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Key Qualifications

- EXPERT knowledge of Allegro 16.6/17.2
- Passionate about your PCB design career
- Skilled at HDI technology
- Extensive experience with high-speed digital, RF and flex and rigid-flex designs
- Experienced with signal integrity design constraints encompassing differential pairs, impedance control, high speed, EMI, and ESD
- Experience using SKILL script automation such as dalTools
- Excellent team player that can lead projects and mentor others
- Self-motivated, with ability to work from home with minimal supervision
- Strong communication, interpersonal, analytical, and problem solving skills
- Other design tool knowledge is considered a plus (Altium, PADS, Xpedition)

Primary Responsibilities

- Design project leader
- Lead highly complex layouts while ensuring quality, efficiency and manufacturability
- Handle multiple tasks and provide work leadership to other designers through the distribution, coordination, and management of the assigned work load
- Ability to create from engineering inputs: board mechanical profiles, board fabrication stack-ups, detailed board fabrication drawings and packages, assembly drawings, assembly notes, etc.

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Eagle Electronics is seeking a CAM engineer specific to the printed circuit board manufacturing industry. The candidate should have a minimum of five years of CAM experience and a minimum of two years of experience in Frontline InCAM software. The candidate should also be fluent in PCB and CAM language pertaining to customer and IPC requirements. The ideal candidate has experience with scripting Frontline InCAM software.

This is a first-shift position at our Schaumburg, Illinois, facility; this is not a remote/off-site position. Any offer would include relocation costs to the Schaumburg, Illinois, area along with competitive salary and benefits.

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Key Qualifications

- EXPERT knowledge of Xpedition VX 2.x
- Passionate about your PCB design career
- Skilled at HDI technology
- Extensive experience with high-speed digital, RF, and flex and rigid-flex designs
- Experienced with signal integrity design constraints encompassing differential pairs, impedance control, high speed, EMI, and ESD
- Excellent team player who can lead projects and mentor others
- Self-motivated with the ability to work from home with minimal supervision
- Strong communication, interpersonal, analytical, and problem-solving skills
- Other design tool knowledge is considered a plus (Altium, Allegro, PADS)

Primary Responsibilities

- Design project leader
- Lead highly complex layouts while ensuring quality, efficiency, and manufacturability
- Handle multiple tasks and provide work leadership to other designers through the distribution, coordination, and management of the assigned workload
- Ability to create from engineering inputs, board mechanical profiles, board fabrication stackups, detailed board fabrication drawings and packages, assembly drawings, assembly notes, etc.

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Required Education and Experience:

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Thank you, and we look forward to hearing from you soon.

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- Participate in multifunctional teams

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- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:
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- Los Angeles

Experience:
- Candidates must have previous PCB sales experience.

Compensation:
- 7% commission

Contact Mike Fariba for more information.

mfariba@uscircuit.com

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Career Opportunities

Zentech Manufacturing: Hiring Multiple Positions

Are you looking to excel in your career and grow professionally in a thriving business? Zentech, established in Baltimore, Maryland, in 1998, has proven to be one of the premier electronics contract manufacturers in the U.S.

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IPC Master Instructor

This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.

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"A comprehensive tour through the world of thermal management. Required reading for designers and end users wishing to understand the science and practice of using insulated metal substrate materials."

Alun Morgan
Chairman, EIPC

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Written by Didier Mauve and Ian Mayoh of Ventec International Group, this book highlights the need to dissipate heat from electronic devices.

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Events Calendar

LOPEC Exhibition and Conference ▶
March 24–26, 2020
Munich, Germany

SMTA Atlanta ▶
April 16, 2020
Peachtree Corners, Georgia, USA

IMAPS CICMT Ceramic Interconnect ▶
April 22–24, 2020
Albuquerque, New Mexico, USA

JPCA Show ▶
May 27–29, 2020
Tokyo Big Sight, Japan

Atlantic Design & Manufacturing ▶
June 9–11, 2020
New York City, New York, USA

PCB West ▶
September 8–11, 2020
Santa Clara, California, USA

AltiumLive 2020 ▶
October 7–9, 2020
San Diego, California, USA

Printed Electronics USA 2020 ▶
November 18–19, 2020
Santa Clara, California, USA

Additional Event Calendars

IPC
SMTA
iNEMI
flex007
pcb design007

Coming Soon to *Design007 Magazine*

April 2020: Design Economics

Next month, our experts delve into the economics of PCB design: the total cost of each design, a variety of methods for controlling costs at each stage, metrics that help designers and engineers track costs, when it's time to outsource a design, and much more.

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