THE pcb design MAGAZINE

October 2017

an I·Connect007 publication

Signal Integrity: The Experts Weigh In p.12

SiSoft Preparing for DDR5 Simulation Next Year p.46

Insulectro Teams with Isola to Address Signal Integrity Needs p.50

Much More!

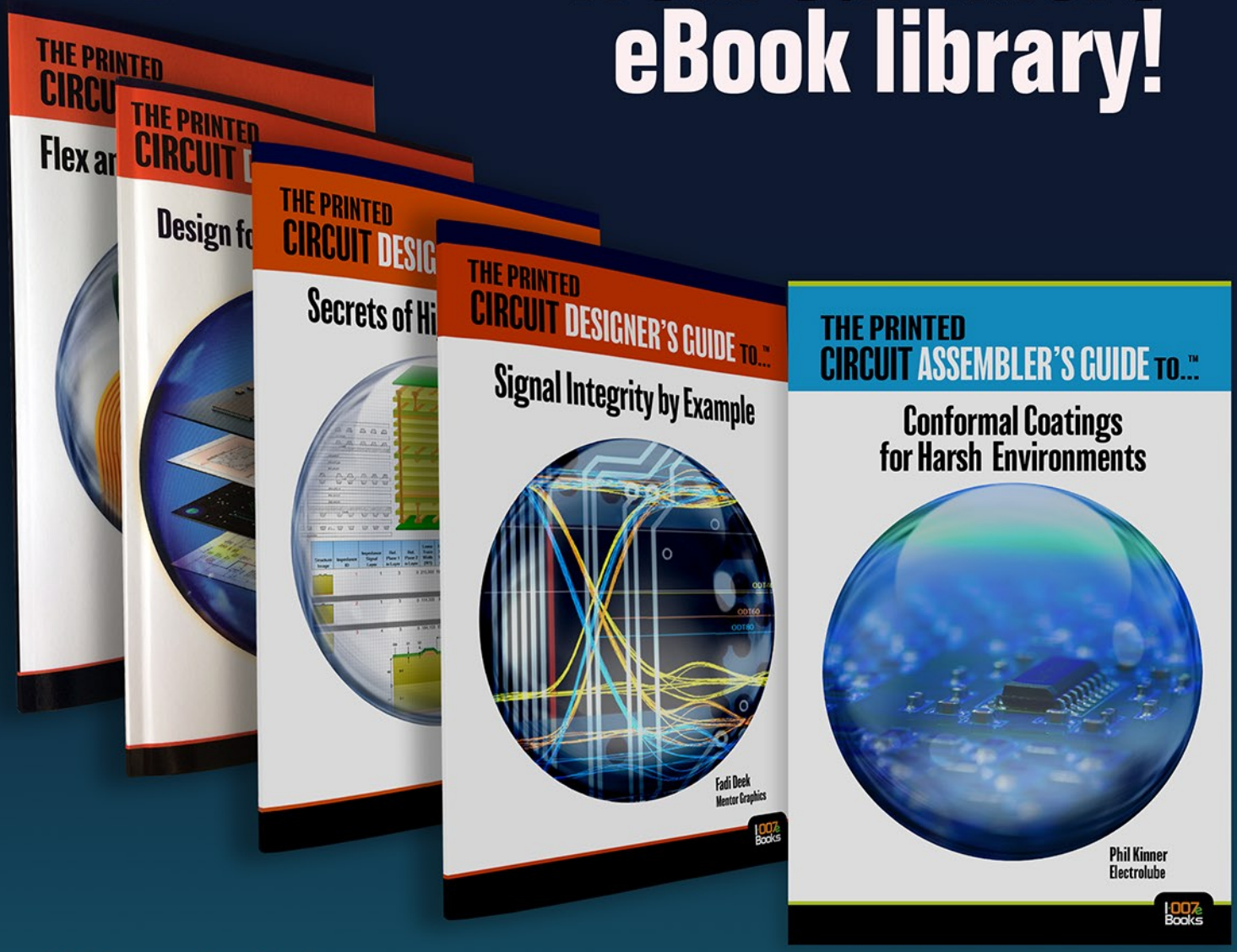
Signal Integrity

The insider's viewpoint

isola
The base for innovation

my Premium Content

Download free books from our micro eBook library!



Written by industry experts, these free micro eBooks each contain valuable information on relevant topics in an easy-to-read format.

Log in or register to access all of our premium content at: myiconnect007.com

my I·Connect007 GOOD FOR THE INDUSTRY

“ If you care about signal integrity, you are sure to pick up a few nuggets of insight from this new eBook. ”

Eric Bogatin
Dean, Signal Integrity Academy
Teledyne LeCroy

This FREE micro eBook, written by signal integrity engineer Fadi Deek of Mentor, A Siemens Business, will benefit anyone interested in identifying the problems, root causes, and solutions surrounding electronic transmissions.

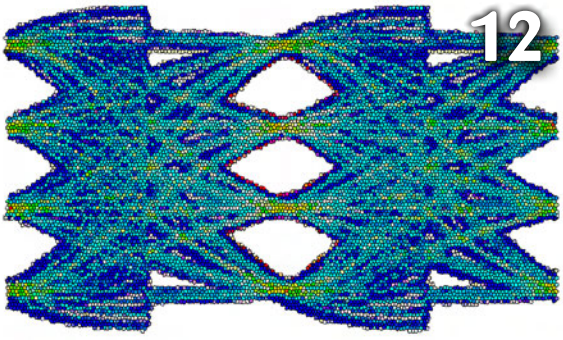
Free Download

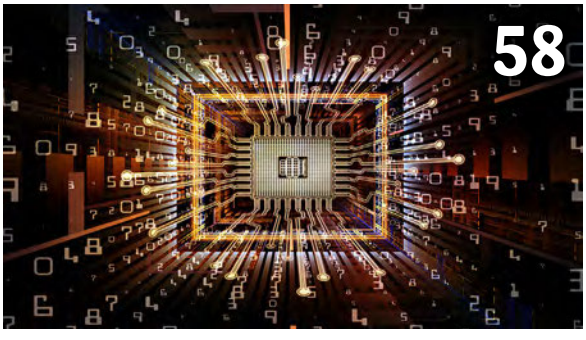
I-007e Books

THE pcb design MAGAZINE

October 2017

Featured Content





Signal Integrity

You've heard it before: "If you don't have signal integrity issues, you will." New low-loss materials are constantly being rolled out to help with signal integrity, and most EDA companies now offer some flavor of tool that can design high-speed, high-frequency boards. But signal integrity continues to perplex PCB designers and design engineers.

12 **Signal Integrity: The Experts Weigh In**
by the I-Connect007 Team

46 **SiSoft Preparing for DDR5 Simulation Next Year**
Interview with Walter Katz

50 **Insulectro Teams with Isola to Address Signal Integrity Needs**
Interview with Chris Hunrath & Norm Berry

FEATURE COLUMNS

20 **When Do Traces Become Transmission Lines?**
by Barry Olney

26 **Practical Modeling of High-Speed Backplane Channels**
by Bert Simonovich

36 **Casual Power Plane Models**
by Istvan Novak

54 **The Impact of Final Plated Finishes on RF PCB Performance**
by John Coodrod

58 **Tangential Thoughts: Loss Tangent Values**
by Martyn Gaudion

productronica
Visit us in Hall B3 Booth 471

High Thermal Reliability

185HR

High-Tg
Low Z-axis
CTE Material

185HR laminate and prepreg materials are manufactured using Isola's patented technology, reinforced with electrical grade glass fabric. This system delivers a 340°C decomposition temperature, a lower Z-axis expansion and offers lower loss compared to competitive products.

185 HR Laminates & Prepregs

For maximum thermal performance and reliability

FEATURES

High Thermal Performance
- Tg: 180°C (DSC) (Base Laminate)
- Td: 340°C (TGA @ 5% wt loss)
- Low Z-axis CTE for reliability

T260: 60 minutes

T288: >15 minutes

Lead-free Compatible and RoHS Compliant

UV Blocking and AOI Fluorescence
- High throughput and accuracy during PCB fabrication and assembly

Superior Processing
- Closest to conventional FR-4 processing

Industry Approvals
- IPC-4101E-WAM1 /98 /99/ 101 /126
- UL – File Number E41625
- Qualified to UL's MCIL Program

© 2017 ISOLA GROUP. ALL RIGHTS RESERVED.

AUTOMOTIVE MILITARY INDUSTRIAL MEDICAL NETWORK

isola

FOR MORE INFORMATION, CONTACT YOU YOUR LOCAL SALES REPRESENTATIVE.

Isola Group
3100 West Ray Road
Suite 301
Chandler, AZ 85226
Phone: 480-893-6527
info@isola-group.com

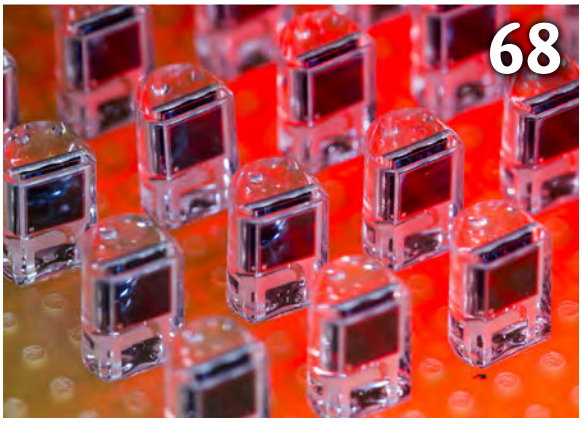
Isola Asia Pacific (Hong Kong) Ltd.
Unit 3512 - 3522, 35/F
No. 1 Hung To Road, Kwun Tong,
Kowloon, Hong Kong
Phone: 852-2418-1318
info.hkg@isola-group.com

Isola GmbH
Isola Strasse 2
D-52348 Düren, Germany
Phone: 49-2421-8080
info-dur@isola-group.com
Website: isola-group.com

THE pcb design MAGAZINE

October 2017

More Content



DdepartmentS

78 Career Opportunities

86 Events Calendar

87 Advertisers Index & Masthead

Columns

8 **Keeping an Eye on Signal Integrity**
by Andy Shaughnessy

68 **Thermal Management for LED Lighting Manufacturers**
by Jade Bridges

Highlights

44 **PCB007**

66 **MilAero007**

74 **Top Ten PCBDesign007**

Shorts

10 **Novel Circuit Design Boosts Wearable Thermoelectric Generators**

19 **Researchers Invent Breakthrough Millimeter-wave Circulator IC**

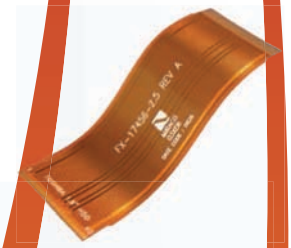
35 **Hybrid Biological Cell Separations Technology for Lab-On-Chip Medical Devices**

49 **Scientists Devolop Shape-Shifting 'Superhero' Robot**

53 **A Zero-Index Waveguide**

72 **Prototype Shows How Tiny Photodetectors Can Double Their Efficiency**

Engineering And Providing Balanced Interconnect Solutions



MIRACO

Miraco, Inc.
Manchester, NH
miracoinc.com
603-665-9449

...connecting technology

Keeping an Eye on Signal Integrity

by Andy Shaughnessy
I-CONNECT007

The temperature is starting to drop and that can only mean one thing: trade show season is in full swing.

I recently went on a productive road trip: PCB West one week and SMTA International the next. I conducted some great interviews at PCB West, and caught up with speakers like Rick Hartley, Susy Webb, and Mike Creeden. The show floor was sold out, and it drew a sizable crowd throughout the day. Remember when conventional wisdom dictated that one-day shows would never work? Now one-day shows, such as PCB West and the regional SMTA tabletop shows, are too valuable for exhibitors to pass up.

I spent the weekend playing tourist in 90-degree Chicago, and then SMTA International began. This show gets bigger every year; combining the IPC fall meetings with SMTAI has proven to be a good call. We interviewed dozens of technologists and managers for our Real Time with… SMTAI video program, and Patty Goldman, editor of the *The PCB Magazine,* conducted numerous audio interviews as well.

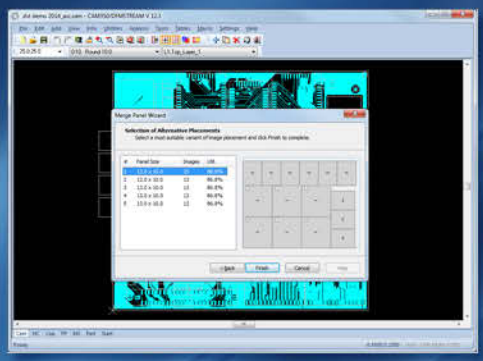
At both shows, almost everyone I spoke with was excited about our industry. A lot of companies are hiring, and many have open positions. Prototron Circuits just hired some new staff, and President Dave Ryder was still trying to fill one last spot. Are we approaching zero unemployment in the PCB world? It certainly sounds attractive, until you have open positions and no qualified workers to fill them. We see evidence of this every month when our magazines feature a half-dozen pages in our Career Opportunities section for PCB companies.

On the tech side, most of the designers and design engineers I spoke with were concerned

Solutions to Ensure PCB Manufacturing Success!

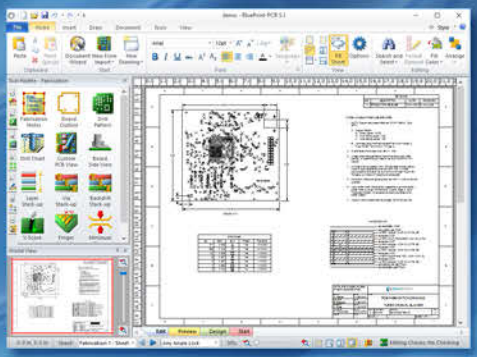
CAM350

Verify and Optimize PCB Designs for Successful Manufacturing.



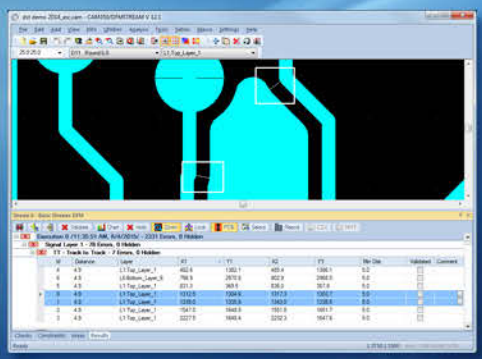
BluePrint·PCB

Create comprehensive documentation to drive PCB fabrication, assembly and inspection.



DFMStream

Verify Design and Manufacturing Rules Any Time During the PCB Design Cycle.



At DownStream Technologies we are committed to delivering comprehensive solutions and workflow process improvements for all your PCB design post processing needs.

For more information please visit downstreamtech.com or call 800-535-3226.

©2016 DownStream Technologies, LLC. All rights reserved. All trademarks and registered trademarks are the property of their respective owners.

DownStream Technologies

about one aspect of signal integrity or another. New low-loss materials are constantly being rolled out to help with signal integrity, and most EDA companies now offer some flavor of tool that can design high-speed, high-frequency boards. As the saying goes, "If you don't have signal integrity issues now, you will."

This month, we decided to delve deep into signal integrity. We kick things off with our experts discussion featuring Michael Steinberger of SiSoft, Mark Thompson of Prototron Circuits, and Yogen and Sunny Patel of Candor Industries, along with Happy Holden. This was one free-wheeling discussion! Learning about how fabricators and designers approach signal integrity challenges was a real eye-opener, to borrow a terrible pun.

Next, Barry Olney of In-Circuit Design looks into exactly when a trace becomes a transmission line. Admit it; you've wondered about that very point, haven't you? Bert Simonovich of Lamsim Enterprises discusses some new ways to model high-speed backplane channels. Then, Oracle's Istvan Novak explores ways to use causal models for your power delivery network to achieve more accurate results.

Marty Gaudion of Polar Instruments brings us a feature column on loss tangent values, and he explains how to use Svensson-Djordjevic modeling to predict loss tangent and dielectric constant. John Coonrod of Rogers Corporation discusses the impact of final plated finishes on RF PCB performance.

We also have a couple of interviews. Walter Katz, chief scientist for SiSoft, explains how SiSoft is preparing for the launch of DDR5 next year, and how AMI can be used to model DDR5 data transfers. Chris Hunrath and Norm Berry of Insulectro discuss their partnership with Isola, and their desire to educate PCB designers about selecting the right low-loss material for their signal integrity needs.

It's hard to believe we're winding this year up already, but we still have a lot to do. We'll be covering productronica in Munich, Germany, from beginning to end, and I'm excited to be attending my first productronica. I've never been to Germany, but I do know a lot of German nouns (mainly from watching "Hogan's Heroes").

Next month we take on HDI, so don't miss out. If you aren't already a subscriber, click here to sign up now! **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 18 years. He can be reached by clicking here.

Novel Circuit Design Boosts Wearable Thermoelectric Generators

Using flexible conducting polymers and novel circuitry patterns printed on paper, researchers have demonstrated proof-of-concept wearable thermoelectric generators that can harvest energy from body heat to power simple biosensors for measuring heart rate, respiration or other factors.

"The attraction of thermoelectric generators is that there is heat all around us," said Akanksha Menon, a Ph.D. student in the Woodruff School of Mechanical Engineering at the Georgia Institute of Technology. "If we can harness a little bit of that heat and turn it into electricity inexpensively, there is great value."

To overcome that, Menon and collaborators in the laboratory of Assistant Professor Shannon Yee designed a device with thousands of dots composed of alternating p-type and n-type polymers in a closely-packed layout. By placing the polymer dots closer together, the interconnect length decreases, which in turn lowers the total resistance and results in a higher power output from the device.

The new circuit design also has another benefit: its fractally symmetric design allows the modules to be cut along boundaries between symmetric areas to provide exactly the voltage and power needed for a specific application. That eliminates the need for power converters that add complexity and take power away from the system.

STRIVING FOR EXCELLENCE IN EVERYTHING WE SAY AND DO.

- Prototype to Production
- Time Critical Production
- Commitment to Customer Service
- Best Quality & Delivery Performance
- Fair and Competitive Pricing/Costs
- Rapid Response to Quote Requests
- Flexibility Scheduling
- Stock/Consigned Inventory Programs

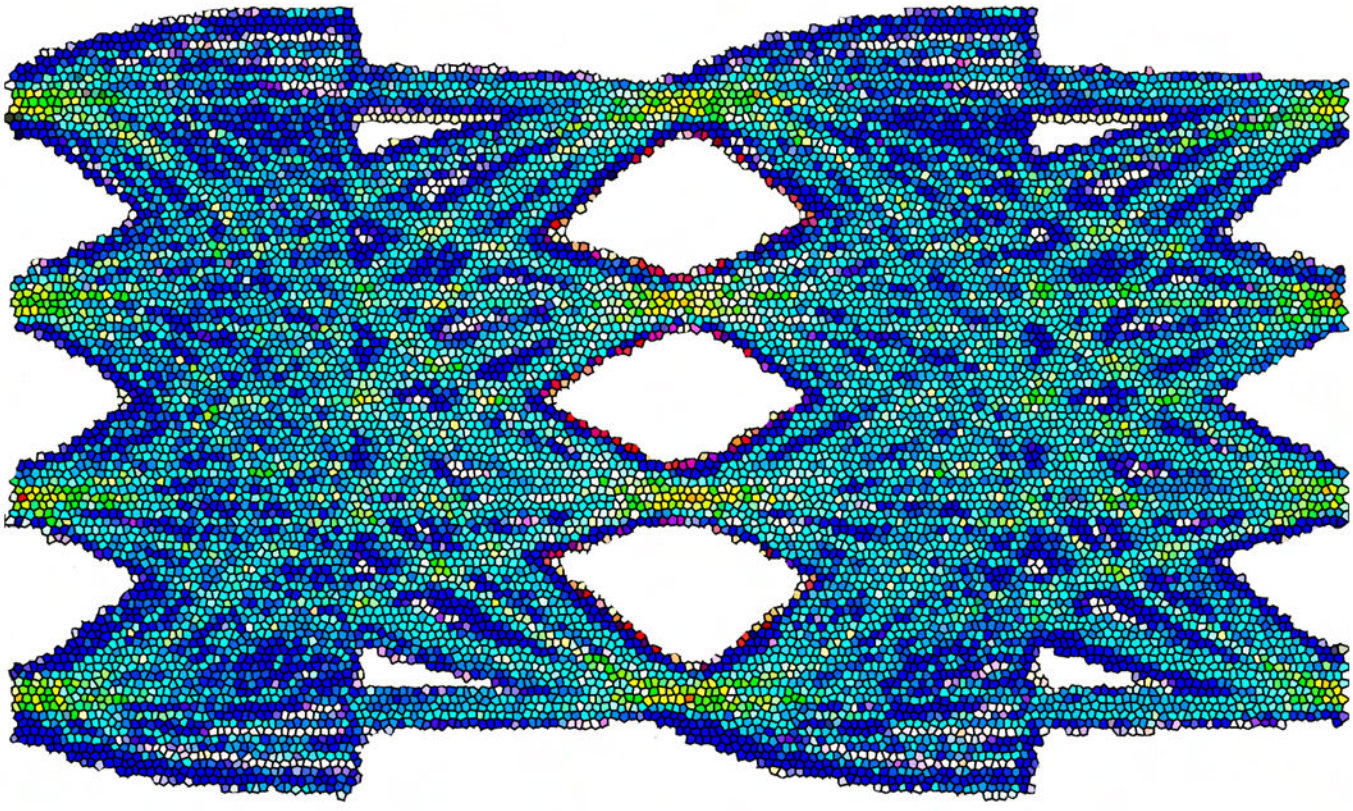
Review Our Advanced Capabilities Now

EAGLE electronics Inc.

MANUFACTURERS OF QUALITY PRINTED CIRCUIT BOARDS

The Absolute Best Value in High Technology Circuit Boards

847.891.5800 • www.eagle-elec.com



Signal Integrity: The Experts Weigh In

by the I-Connect007 Team

When we began planning this issue on signal integrity, we arranged a conference call with a variety of industry experts. Mike Steinberger of SiSoft, Mark Thompson of Prototron Circuits, and Yogen and Sunny Patel of Candor Industries joined editors Andy Shaughnessy, Patty Goldman, Happy Holden and Publisher Barry Matties on the call for a spirited discussion about the challenges related to signal integrity and some of the tricks of the trade for helping ensure SI.

From the Front End

Steinberger began by sharing two issues he's been studying, one large and one small. "The large point is in the analysis of error-correcting code performance on high-speed serial channels. When you look at the drive toward PAM4, it is absolutely essential that you bring error-correcting codes along. The fact of the matter is that, when you have a fair amount of margin, NRZ does better than PAM4; but when you start reducing the margin, the PAM4 bit error rate doesn't degrade as quickly as the NRZ bit error rate degrades. So when you're starting to get the minimum amounts of margin, then FEC is the way to go. But it's FEC operating in a condition where it's got a relatively high error rate. So error-correcting codes come as an essential technology along with PAM4.

"But I think that the benefits of error-correcting codes have been oversold, in that the performance analyses for error-correcting codes have been based on assumptions that are appropriate for radio channels, like where you have a lot of added noise—so a satellite channel or something like that. Therefore, the errors are completely uncorrelated. On high-speed serial channels, the errors are more correlated than that, and people have not done the performance estimate while taking this correlation of errors into account. I did some simulations and was able demonstrate that the correlation of errors is due to the inter-symbol interference.

Start Your Next Design with OrCAD

Don't let your budget limit the capability of your design software. Get your project started right with the industry leading PCB design technology in OrCAD® Capture and OrCAD PCB Editor. For a limited time, you can get a perpetual license of this fully scalable design solution for just the cost of maintenance.

Get OrCAD Free ›

OrCAD™
CADENCE PCB SOLUTIONS

EMA Design Automation®

Eventually, accurate estimation of error-correcting code performance on high-speed serial channels is going to become a thing in itself. I ran into someone from Cisco at DesignCon who was ready to have that conversation.

"A smaller thing, but also important: Suppose you have a transmission line that's going over a ground plane. It gets to a certain point and there's a cutout in the ground plane. What happens when the transmission line hits that discontinuity? There are return currents flowing in the reference plane and those currents have to go some place. Well, now, the return currents aren't going to flow all the way around this discontinuity to meet up at the other side. It turns out what the return currents do is transition to whatever the closest plane is, regardless whether you have a return via or not. So, you don't need ground vias to have this transition of the return current occur, and it turns out that there is a very simple formula for what amounts to an inductance that the return current goes through when it transitions from one reference plane to another. This is a piece of knowledge that all signal integrity engineers should understand, and basically none of them do. No, you're not going to get it from a 3-D field solver; you get it from closed-form equations.

"One other thing: We may be approaching a brick wall when it comes to throughput on serial channels. Back in 1995, I told a room full of people that they needed to be designing faster and faster high-speed serial channels and history supported me on that one. I'm going to take another chance here and say that there is going to come a limit, and we may be starting to get close to that limit."

Mark Thompson replied, "That's funny, because we've been spending so much time over the last 10 years beating up the material manufacturers, saying, 'Look, we need specific dielectric constants. We need specific loss tangents.' Now we're at a time that we're beating up the copper foil manufacturers for surface roughness because we're literally at a stage where 25 gig is the key, and at that stage any surface tooth or surface roughness is an issue. It's strange that we've gone from a situation where we beat up material manufacturers to the point where we're beating up copper manufacturers to get surface roughness down to a minimum."

Mark Thompson

"I think the conversation's going to change again," said Steinberger. "There was a paper given by Rogers at DesignCon two years ago that I found to be a mind-blower. Rogers observed that when they measured transmission losses for two different kinds of copper, rolled copper and electrodeposited copper, they found that all these roughness models that we've been using modeled the electrodeposited copper quite well and over-predicted the losses for the rolled copper, by a lot.

"So I wonder, going up to these higher frequencies, if people are really going to take this data from Rogers seriously, as I think they should. Maybe they'll start asking you for rolled copper instead of electrodeposited copper."

"We've had some customers ask for rolled annealed copper, as opposed to the electrodeposited variety," Thompson added. "We see less of that stuff than we did in the old days. Remember when people were asking for things like an 11-degree offset on a panel to minimize having to deal with having a structure sitting over the top of a knuckle or weave of the material? Or things like skin effect due to differential pairs that were dipped in deep gold that didn't have any solder mask over the top of them. We see less of that stuff."

Steinberger had an idea about why that might be. "Part of that is that people end up routing it at different angles anyway so you don't have these really long straight lines, or you shouldn't have these long straight lines, that they had on the test boards where they were measuring these effects to begin with. I never was really happy with

that whole discussion of weave effect, for two reasons. One of which was simply the emotional tone that got tied to the whole subject. I remember one phrase in particular from one particular author. In the middle of a DesignCon paper he said, 'Be afraid, be very afraid.' I'm sorry, but that phrase has no place in a professional discussion. In 2012, I wrote an online article that said, 'Oh, by the way, you can accept a certain amount of skew. You get a little bit of degradation but as long as you keep the skew within like an eighth of a wavelength at the maximum frequency of interest, the effects can be minimal.'

Sunny Patel

"Then a couple years later, Istvan Novak and his people at Oracle came in with a DesignCon paper where they actually tested in the lab what the acceptable level of skew was. Again, this is an equation that has not only a left-hand side but a right-hand side. So don't just take this 'ooh, scary' point of view. This is an engineering problem; let's work this as an engineering problem. There's a tolerance we can live with."

From the Fabricator's Viewpoint

Sunny Patel said, "We make boards for different technologies, and we can control the impedance to nearly 2%. We can talk about the challenges with keeping those tolerances that tight, like how the dielectric thickness and the etching characteristics in plating are really the key parts of the fabrication process."

"We know that most manufacturers control impedance close to 10% most of the time," added Yogen. "To control to under 5%, they charge so much extra money. There are three main differences between the conventional process, as we call it, and our process. First, our press is resistive-heating so the outer layer copper becomes a heater, and that's why we don't have to press at 350 PSI—we use 230 PSI—so the dielectric is very consistent across the whole panel. And then we drill, clean the holes, and panel plate copper over the whole board, which is the second difference. This makes for very consistent copper thickness over the whole panel and in the hole as well. And the third major difference is our positive-acting electrodeposited photoresist, where the areas exposed to UV light develop off. Then we etch in cupric chloride. In this way, we get very uniform conductors, and that's how we can control impedance to close to 2%."

"The main issue on the board fabrication side is consistent lamination, making sure that the board shop has a good, consistent way of measuring at different weaves and resin contents," Sunny explained. "If a PCB manufacturer is pulse plating, the consistency will be pretty good, but that's generally one of the areas where most will have difficulty—with copper plating and copper etching as well. So, people with more direct imaging and pulse plating technology, or our way of doing things, will get you finer impedance characteristics. But a lot of it comes back to the engineers themselves, discussing stackups and what they want in the end with their PCB supplier—having that thorough conversation with the engineer on the board side to ensure that what they want is what they're going to get with the stackup. Those are the two main things: The process has to be controlled and consistent, and there has to be a clear communication with the design engineers."

Mark Thompson had a similar viewpoint. "I agree with you guys as far as the negotiation process. If a customer approaches you before they have a design ready, and their engineer has just told them, 'I have 8-, 10-, and 12-layer boards, and I need to get a slew of impedances from you, and a dielectric stackup with effective dielectric constants for each of the subsections,' there are several questions that must be asked at that time. A lot of us come up with an impedance checklist that asks all those basics, such as: What's the material type? What's the cop-

per weight? Where will the impedances reside? What are the thresholds in tolerances (e.g., 100 ohms, 120 ohms, 75 ohms)? And what are the intolerances associated with it (2%, 5%, 10%, etc.)? At a stage where there has been no layout done and no actual artwork exists, it's difficult from a fabrication side to crawl into the customer's head and picture what it is he's trying to accomplish.

"But if you're dealing with a fabricator that has not dealt with CPWGs (coplanar waveguides) properly, they'll come back and say, 'Cosmetically, we want to route this thing out and don't want to see any burring, so we're going to hack back that launch pipe three or four thousandths,' which is doing a huge detriment to you as the end user. Obviously, in a coplanar waveguide, the launch needs to reside right at the part edge, and the end-user is well aware that the exposed copper there is really what you want to see. You really want to see it actually meeting with the Z-axis and you don't want to trim it back in any way.

"Even material manufacturers will play games with you from time to time. I remember when we had a situation where one of our material manufacturers was sending us very consistent material up until a point and then all of a sudden we got a mismatch in all of our numbers. All of our impedances were off, and it was all linear in one direction. We started doing some cross-sections, and we discovered that the 106, the 1080, 2113s, 2116s, 7628s of the world were all approximately 1 mil thicker than what we were previously predicting.

"Well, guess what? They made a change in their manufacturing process from Shenzhen to Guangdong and in the process, they went from a cure process that went from air drying cure to a heat drying cure, which resulted in a slightly different dielectric thickness. That was a problem for us, because they were sending it from two sources. We were getting prepreg materials and core materials from both Shenzhen and Guangdong, and how could I possibly be able to predict impedances for a customer when I couldn't even predict the dielectric impedances of the prepregs that were being used? That's something that happens from time to time, and something you need to be aware of."

Mike Steinberger

Barry Matties asked if a cutting-edge high-speed design would face many specific challenges downstream during the fabrication process.

"Oh, of course," Thompson replied. "All the things that these guys were just talking about: etching and plating, and coming up with techniques to actually minimize any loss off now that we're having to deal with a class 3 and AS9102 world. So, a lot of jobs that have things like blind, buried or epoxy-filled vias will require an additional wrap plate. That additional wrap plate means that I'm going to dig into your available space just that much more. Will that affect your impedances? Absolutely. That additional metallization, that additional plating, over the top of the trace for the wrap will indeed affect your impedances and it is definitely something you have to be aware of."

Signal Integrity Tips

"OK, guys," said Steinberger. "I've been listening to this discussion of impedance, and I understand what you're saying, and thinking about it from my old microwave days. Geez, if I could get a VSWR (voltage standing wave ratio) that was better than 1.2, I thought I was starting to do pretty good. That's a 20 Db return loss, and it meant I got my impedance within 20%, and by the time I was getting down to a 1.05 VSWR, meaning 5% impedance, I thought I was pretty well there.

When I think about the kinds of designs that I've been involved in, which is admittedly a small subset of the types of designs you get involved in, the vias and the impedance discontinuity of the vias become way more impor-

“A comfortable approach to the selection, implementation, and testing of protective coating processes.”

Dr. Helmut Schweigart
Technology Development Head,
Zestron Europe

This FREE micro eBook, written by Phil Kinner, Electrolube’s global business and technical director, will benefit anyone in the electronics industry who wants a better understanding of conformal coatings.

Free Download

I-007e Books

tant than exactly what the discontinuity was looking into the transmission line. So I start to wonder more about pad sizes, backdrill precision, and the fact that I can't get big enough anti-pads on my vias to get the impedance of my via to begin with. At least from my point of view, I'm used to thinking that those via discontinuities are by far a larger problem. Would you say yes or no, in the work you do, Mark?"

"Oh, absolutely, Mike," Thompson said. "You raise a good point. In fact, 10–15 years ago, all the fabricators removed any non-functional pads. Today, that is rarely ever done—mainly because of board geometries, because of what you're talking about, us cramming more and more stuff on any given area. Because we're ending up cramming more stuff on there, there's less room for error for us for removal of non-functional pads.

"If we do that same kind of a thing today, let's say you had 5,000 drilled vias on this particular board, and on a given internal signal layer you had only two terminations, two traces where you had terminations, everything else would be considered a non-functional pad. If I remove all those non-functional pads, have I not just created an absolute registration nightmare for myself in lamination? I've removed so much additional metal from the internal layer, that now I've created a mismatch and I'm setting myself up for registration problems."

Steinberger shared his thoughts on pads. "From my end of it, I'd like to remove all the pads. Every single one of them. If I could get away with a pad diameter equal to the drill diameter at my routing layer, where I actually did want to connect to the trace, I'd do it. It's just that you guys wouldn't exactly buy it."

"That's just technology in general which has yet to catch up to what we require," said Sunny. "The new type of layup, back straights, calculations, algorithms, is all trying to get back to what you're saying, to remove those non-functional pads and get that alignment to where we need it to be for perfect manufacturing."

Yogen Patel

Happy Holden mentioned a recent article he wrote that discusses landless via processes. "There are four different ways of doing it, one of which is the positive electrophoretic resist. But there are three other ways: the direct imaging machines, the Hewlett-Packard method that they got from the Japanese (which doesn't require any change in imaging registration), and then there's the Russian method. Anybody can use the Hewlett-Packard and Russian methods; they are free and no change of equipment or process is required—just a change in artwork. I've made more landless vias than everyone in the world put together, but the article mentions all four methods.

"Landless vias were never adopted by the IPC, though we (HP) have data that shows landless vias are 10–times more reliable than vias with lands. The landless via and its reliability blows a hole in Class 1, 2, and 3. HP did extensive testing: on different hole diameters, different thickness of boards and different sizes of vias; and we found out that our Japanese partners apparently knew a lot more than we did, and they were less subject to influence from the IPC. You needed a pad 50 years ago because we used to crimp actual leaded components, not to the whole barrel but to the pad, and because we've been doing it for 60 years, the industry thinks we have to do it forever, even though it's detrimental to reliability, density, and signal integrity. Hewlett-Packard used them exclusively once we discovered the secret, and nobody bothered to look at our boards closely enough to realize there weren't any lands on those vias. They're covered with solder mask, so you don't really see it."

The conversation then turned to IPC and its processes for creating and amending standards. Yogen wondered how much luck he would have getting IPC to officially recognize the landless via.

"Yeah, you won't get any at all," replied Holden. "Which is why HP and IBM ignored IPC standards, because they made our competitors less competitive. And we knew it was all propaganda. They didn't have any data to support any kind of use of lands, but we had data, and we traded it with IBM. They had the same data."

Steinberger said the standardization process itself is partly to blame for such impasses. "I do observe that, for those who have not been involved in a standardization process, they think that standards are extremely intelligent and extremely reliable. For those of us who have been deeply involved in the standards process, we know otherwise. Part of the problem with the standardization process is that not everybody in the committee has the same goal. So although you can get an informed debate, and there are some standards bodies in which people are responsible, the fact of the matter is that if people don't have the same goal, then what you get is not necessarily going to serve any one goal very well."

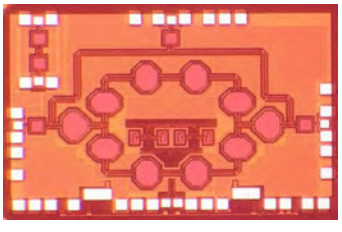
"And anybody can veto a standard and keep it from being published, until you water it down, until you finally get a consensus," added Holden.

"The problem with most of the standards is that they have been designed in early days," Yogen said. "And then nobody wants to challenge history again."

So, everyone agreed that signal integrity isn't just a problem for PCB designers and design engineers; today's high-speed, high-frequency boards with can wreak havoc downstream. It was an eye-opening conversation for everyone involved. Steinberger summed it up:

"One thing I can promise you is that, from this discussion, there are a couple of colleagues that I will ask about landless vias just to see what they know," said Steinberger. "Because I am working with some people who are actively designing a system at 28 gigabits and starting to plan for 56 gigabits, and it would be interesting to see what those people have to say." **PCBDESIGN**

Researchers Invent Breakthrough Millimeter-wave Circulator IC



Columbia Engineering researchers, led by Harish Krishnaswamy, associate professor of electrical engineering, in collaboration with Professor Andrea Alu's group from UT-Austin, continue to break new ground in developing magnet-free non-reciprocal components in modern semiconductor processes. At the IEEE International Solid-State Circuits Conference in February, Krishnaswamy's group unveiled a new device: the first magnet-free non-reciprocal circulator on a silicon chip that operates at millimeter-wave frequencies (frequencies near and above 30GHz).

Most devices are reciprocal: signals travel in the same manner in forward and reverse directions. Nonreciprocal devices, such as circulators, on the other hand, allow forward and reverse signals to traverse different paths and therefore be separated. Traditionally, nonreciprocal devices have been built from special magnetic materials that make them bulky, expensive, and not suitable for consumer wireless electronics.

The team has developed a new way to enable nonreciprocal transmission of waves: using carefully synchronized high-speed transistor switches that route forward and reverse waves differently. In effect, it is similar to two trains approaching each other at super-high speeds that are detoured at the last moment so that they do not collide.

The implications are enormous. Self-driving cars, for instance, require low-cost fully-integrated millimeter-wave radars. These radars inherently need to be full-duplex, and would work alongside ultra-sound and camera-based sensors in self-driving cars because they can work in all weather conditions and during both night and day. The Columbia Engineering circulator could also be used to build millimeter-wave full-duplex wireless links for VR headsets, which currently rely on a wired connection or tether to the computing device.

When Do Traces Become Transmission Lines?

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

At low frequencies, traces and components on a PCB behave simply as lossless lumped elements—as taught in Circuit Theory 101. But as the frequency increases, the copper trace and adjacent dielectric(s) become a transmission line, the skin effect forces current into the outer regions of the conductor and frequency dependant losses impact on the quality of the signal.

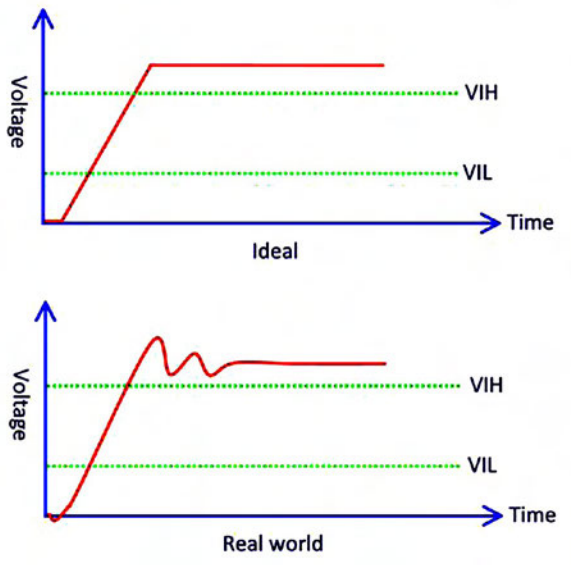


Figure 1: Ideal vs real-world rising edges.

The PCB trace now behaves as a distributed system with parasitic inductance and capacitance characterized by delay and scattered reflections. The behavior we are now concerned about occurs in the frequency domain rather than the familiar time domain. This is the real world of high-speed design.

Ideally, square wave signals are just that—perfect square waves with an evenly, sloping rising and falling edge. However, in the real world, things are quite different. Figure 1, illustrates the rising edge of a square wave, in the ideal case (low frequency), compared to the real world (high frequency). The transmission line effects create under and overshoot resulting in ringing in the signal. If this ringing crosses the voltage input high threshold (VIH), at the receiver, then it may cause false triggering.

The Fourier theorem states that every function can be completely expressed as the sum of sines and cosines of various amplitudes and frequencies. The Fourier series expansion of a square wave is made up of a sum of odd harmonics. Figure 2 shows the conversion of a square wave from the time domain to the frequency domain and the resultant amplitudes of the frequency components. If the waveform has an even mark-to-space ratio, then the even har-

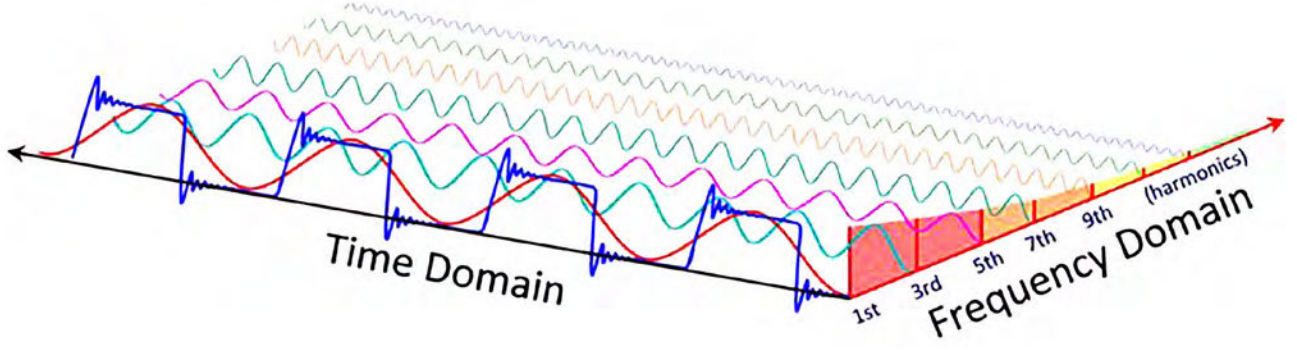
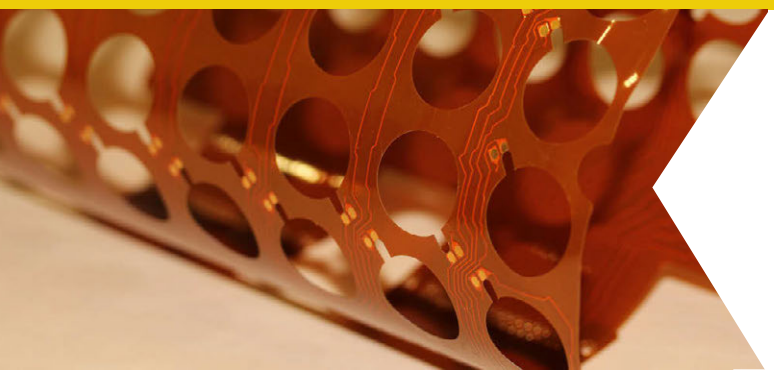


Figure 2: Harmonics of a square wave converted from the time domain to the frequency domain.

We deliver Advanced PCB Solutions!

Our unique processes enable us to create and deliver Advanced PCB Solutions that meet the needs of the demanding market at competitive prices!



Impedance Tolerance <5%!

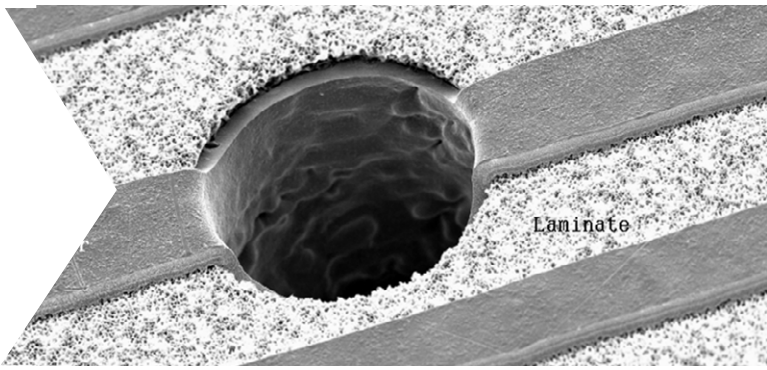
With our panel plating process combined with continuous foil lamination, our impedance tolerances are second to none!

CLICK TO LEARN MORE

Landless Via Technology

We're the only manufacturer in the world to have perfected a liquid photo-imageable resist (PiP) in electrolytic form, used for all our production.

CLICK TO LEARN MORE



Tensile Strength achieved with Candors Panel Plating

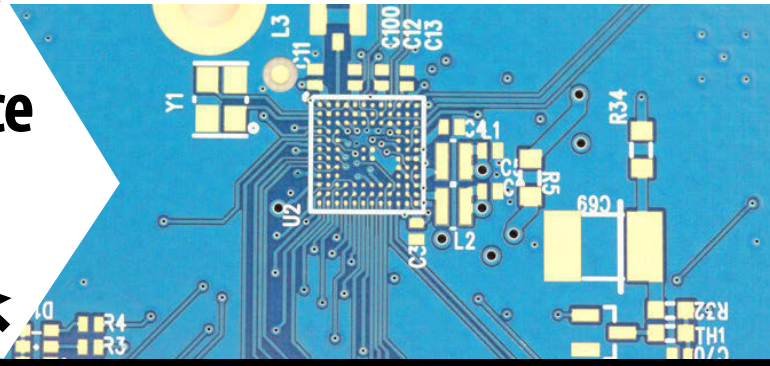
Practically perfect plating exceeds class 3A elongation, purity, and tensile strength

CLICK TO LEARN MORE

Fine line PCB, 2 mil line /space

We have developed a unique set of processes based on electro-depositable liquid photoresist.

CLICK TO LEARN MORE



CANDOR INDUSTRIES INCORPORATED
ADVANCED PCB SOLUTIONS

PHONE: (416) 736-6306

WEB: www.candorind.com
SALES: sales@candorind.com

monics cancel. The high-frequency content of a square wave is significantly affected by the rise time of the waveform. Also, as the frequency increases, the amplitude decreases. In the real world, one needs to consider the maximum bandwidth of a signal, including harmonics, rather than assume the perfect square wave fundament frequency model.

Surprisingly, even at very low frequency, an old-fashioned telegraph line is a transmission line simply because the wire length is comparable to the signal rise time. In recent years, edge rates have become much faster, to the point where short traces, on a PCB, are a small multiple of the edge rates propagating through them. As such, one should consider these PCB traces to be transmission lines and analyze their signal integrity.

In general, all drivers whose trace length (in inches) is equal to or greater than the rise time (in nanoseconds) should be considered critical and treated as high-speed transmission lines. It is the signal rise/fall time, rather than the signal clock frequency, that determines the critical signal speed. However, a steep rise/fall time may be slowed by loading the signal line with a damping/back-matching resistor close to the source.

Impedance is the key factor that controls the stability of a design—it is the core issue of both the signal and power integrity methodology. At low frequencies, a PCB trace is almost an ideal circuit with little resistance, and without capacitance or inductance. Current follows the path of least resistance. But at high frequencies, alternating current circuit characteristics dominate causing inductance and capacitance to become prevalent. Current then follows the path of least inductance. The impedance of an ideal, lossless transmission line is related to the capacitance and inductance:

$$Zo = \sqrt{L/C}$$

But this is very simplistic and the impedance should be simulated by a field solver to obtain accurate values, of impedance, for each signal layer of the substrate. The impedance of the trace is extremely important, as any mismatch along the transmission path will result in a reduction in quality of the signal and possibly radiation of noise. For perfect transfer of energy, the impedance at the source must equal the impedance at the load. However, this is not usually the case and terminations are generally required, at fast edge rates, to limit ringing.

50 to 60 ohms characteristic impedance is often used in high-speed designs. Lower impedance values cause excessive dI/dt crosstalk and can double the power consumed to create a heat dissipation problem. Higher impedances not only produce high crosstalk, but also produce circuits with greater electromagnetic emissions and sensitivity. However as core voltages drop, rise times become faster and frequency increases, and a lower impedance is more desirable. For example, DDR3/4 memory buses use 40 ohm characteristic and 80 ohm differential impedance.

Figure 3 details the actual input impedance measured with a vector network analyzer (VNA), looking into a one inch transmission line with the other end open. This looks remarkably similar to the AC impedance of a plane cavity's resonance, which also has no termination. However, the plane pair has more area and therefore much more capacitance and less inductance than a trace, making the resonance lower in frequency and providing a very low impedance path. So, planes simply act as big, fat, unterminated transmission lines.

This transmission line was designed to have a characteristic impedance of 50Ω but the frequency dependant losses impact on the quality of the signal. The frequency domain transmitted and reflected data is respectively referred to as insertion and return loss. The characteristic impedance (Zo), that is commonly used to specify trace impedance, is defined as the instantaneous impedance of a lossless transmission line.

The most fundamental signal integrity analysis involves defining the board stackup, including appropriate dielectric constants and layer thicknesses, and determining the appropriate trace width (and clearance for differential signals) that corresponds with the target characteristic and differential impedance for the traces. However, selecting the right impedance, and other transmission line characteristics, are essential to generating accurate results.

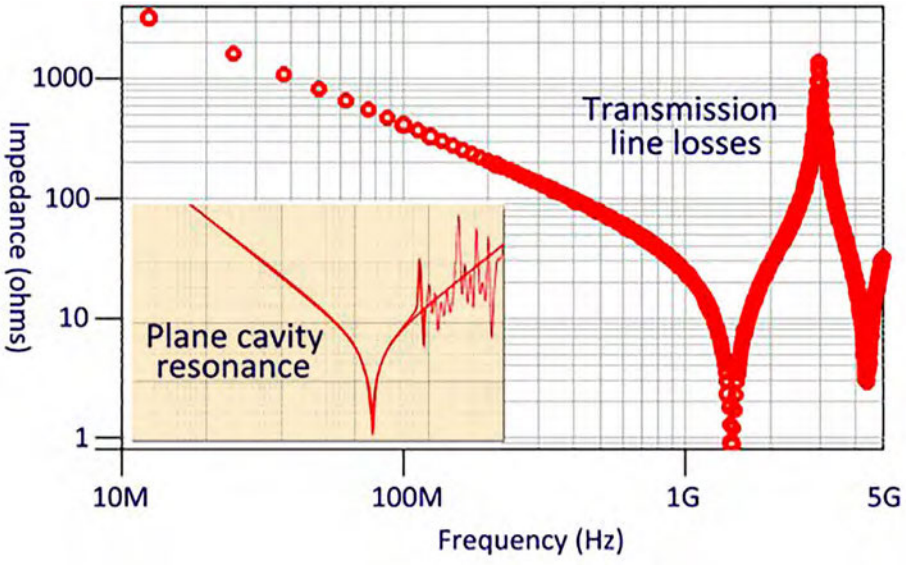


Figure 3: A 50Ω, 1-inch trace measured with a vector network analyzer (source: Eric Bogatin).

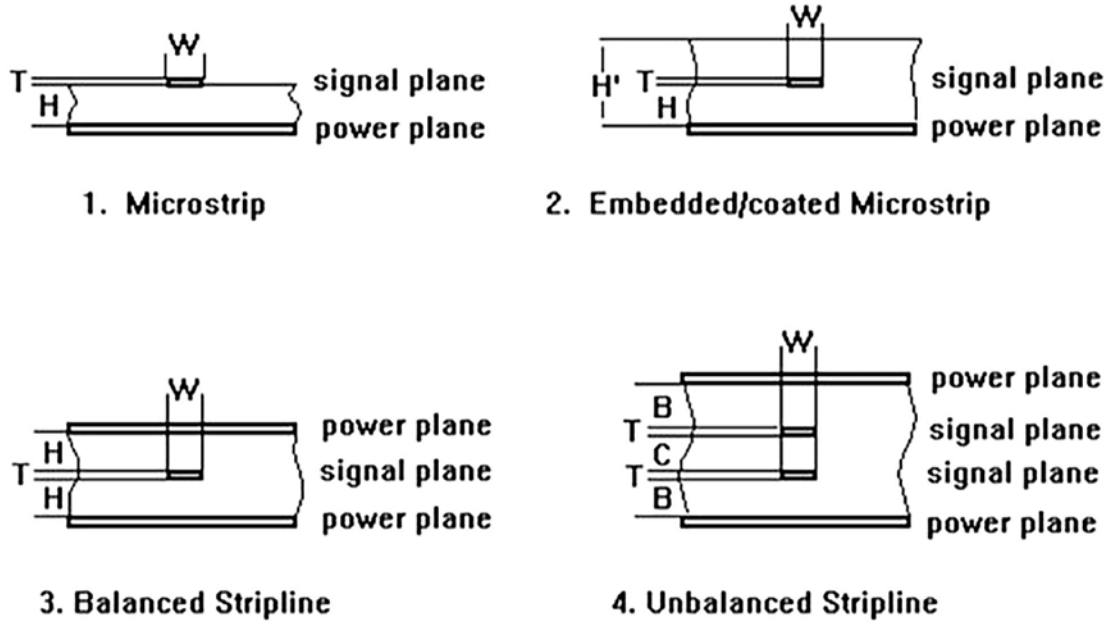


Figure 4: The four main configurations of impedance structures (source: IPC-2251).

Multilayer PCBs are ideally suited for providing interconnection wiring that is specifically designed to provide desired levels of impedance control. Techniques commonly referred to as microstrip and stripline are employed for impedance control. There are four basic types of transmission line constructions, as shown in Figure 4:

1. Microstrip
2. Embedded microstrip (with solder mask or conformal coating)
3. Balanced stripline (aka symmetric stripline)
4. Unbalanced or dual embedded stripline (aka asymmetric stripline)

It is important to note the variation in dielectric constant (Er or Dk) that different materials can exhibit. For instance, air has an Er = 1, whereas an aluminum stiffener may have an Er = 10 and then there are barium oxides that go up to 600. Standard FR-4 has an Er = 4 and dielectrics specifically designed to be used for high-speed designs have a very low dielectric constant. For instance, Isola Astra-MT77 100GHz material has an Er = 3. The dielectric constant has a direct impact on impedance and the signal propagation through the substrate. That is why the dielectric constant for a specific material should always be obtained from the supplier's specification (or a reliable source) that lists the Er at different frequencies. Please note that datasheets generally list the dielectric constant as Dk.

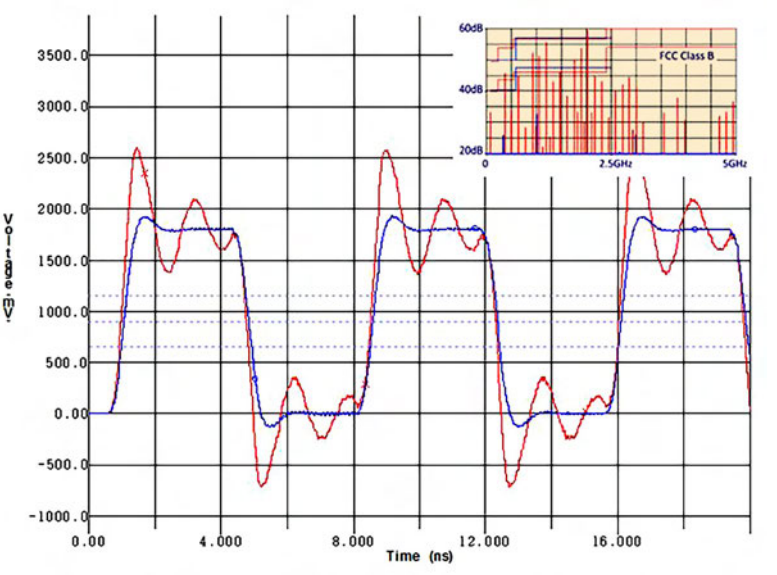


Figure 5: Ringing is reduced dramatically by adding a series terminator (simulated in HyperLynx).

Closed-form equation-based impedance calculators have been around for many years, but unfortunately, they are extremely limited in accuracy. Many examples can be found on the internet and generally their results are just rough estimations but where they all come totally unstuck is in the calculation of dual embedded (asymmetric) stripline. IPC published impedance equations in the original IPC-D-317 and later in the IPC-2251 standard. The later was based on Brian C. Wadell's book Transmission Line Design Handbook, but even these quite elaborate equations are unable to cope with wide unbalances in surrounding dielectric in the stripline configuration. Since impedance is the key factor that controls the stability of a design, one should never compromise the accuracy required, for high-speed design, and the use of a precision field solver is mandatory.

I mentioned earlier that a steep rise/fall time may be slowed by loading the signal line with a damping/back-matching resistor close to the source. This also serves to match the impedance of the driver to the transmission line. Unfortunately, using mainstream PCB layout software, one really has no idea what the driver impedance is, let alone the capability to match the driver to the impedance of the transmission line. Driver impedance is typically low, compared to a typical 50 ohm transmission line, but adding a series resistor, of the correct value, solves this issue.

The need to terminate a PCB trace is based on several design criteria. The most important being an electrically long trace, when the length exceeds one sixth of the electrical length of the rising edge rate. But even if the trace is short, termination may still be required if the load is capacitive or highly inductive to prevent ringing. Series termination is excellent for point-to-point routes, one load per net. It also works well for traces that are electrically short and is used to fanout multiple loads radially from a common source (star routed) without affecting other circuits in the network. Series termination reduces ringing and ground bounce. It is the most common termination used for high-speed design.

Revisiting the real-world rise time edge rate (Figure 1), by placing a series terminator (close to the source) the ringing is reduced dramatically. This will reduce crosstalk and also knock off the radiation. In Figure 5, the red waveform is the original, ringing signal, and the blue waveform demonstrates the damping effect of a series resistor taking us back to a near ideal waveform. The insert is the projected emissions in the frequency domain.

High-speed digital design is all about controlling impedance. The impedance of the transmission lines needs to be matched and maintained at a constant value along the entire length of the interconnect. Also, the power distribution network needs to provide a low impedance path, through the planes, across the entire frequency bandwidth of the signal. These seemingly unrelated disciplines control the stability and reliability of the product. Get it right and your high-speed design is off to a great start; get it wrong and you are in for a (real) world of pain.

Points to Remember

- At high frequencies the PCB trace now behaves as a distributed system with parasitic inductance and capacitance characterized by delay and scattered reflections.
- The transmission line effects create under and over shoot resulting in ringing in the signal.
- The Fourier series expansion of a square wave is made up of a sum of odd harmonics.
- A trace becomes a transmission line simply when the length is comparable to the signal rise time.
- All drivers whose trace length (in inches) is equal to or greater than the rise time (in nanoseconds) should be considered critical and treated as high-speed transmission lines.
- Impedance is the key factor that controls the stability of a design; it is the core issue of both the signal and power integrity methodology.
- For perfect transfer of energy, the impedance at the source must equal the impedance at the load.
- Terminations are generally required, at fast edge rates, to match the impedance and limit ringing.
- As core voltages drop, rise times become faster and frequency increases, and a lower impedance is more desirable.
- The measured input impedance of a transmission line looks remarkably similar to the AC impedance of a plane cavity's resonance which also has no termination.
- The characteristic impedance (Zo), is defined as the instantaneous impedance of a lossless transmission line.
- The most fundamental signal integrity analysis involves defining the board stackup, which is essential to generating accurate results.
- Dielectrics, specifically designed to be used for high-speed design, have a very low dielectric constant.
- Closed-form equation based impedance calculators are extremely limited in accuracy and the use of a precision field solver is mandatory.
- A series resistor can be used to match the driver to the impedance of the transmission line.
- Termination is required if the trace length exceeds one sixth of the electrical length of the rising edge rate.
- High-speed digital design is all about controlling impedance. **PCBDESIGN**

References

1. Barry Olney's Beyond Design columns: Controlled Impedance Design, Impedance Matching: Terminations, Signal Integrity Parts 1, 2 & 3

2. What's the Difference Between Signal Integrity and Power Integrity? by Patrick Carrier

3. The Critical Length of a Transmission Line, by Eric Bogatin

4. Bandwidth Basics, Wavelength Electronics

5. IPC-2251–Design Guide for the Packaging of High-Speed Electronic Circuit

6. High-Speed Digital Design, by Howard Johnson

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN and CPW Planner. The software can be downloaded from www.icd.com.au. To contact Olney, or read past columns, click here.

Practical Modeling of High-Speed Backplane Channels

by Bert Simonovich
LAMSIM ENTERPRISES

As Dave Dunham of Molex Corp. likes to say, "When designing high-speed serial links beyond 10 GB/s, everything matters." And part of that everything is accurate modeling of transmission line losses.

Failure to account for conductor roughness can ruin you day especially if you are trying to push 28 GBaud/s (56 GB/s) PAM-4 signaling down your channel. As shown in Figure 1, with just 1.4 dB delta in insertion loss, at 14 GHz Nyquist frequency, results in an average reduction of 38% in eye height, and 4.3% increased jitter across all three eyes, when conductor roughness is taken into account. On top of that, failure to correct dielectric constant (D_k) from manufacturers' data sheets due to conductor roughness can lead to inaccuracy in phase delay[1].

To ensure first time success at these speeds, using the right parameters for dielectric and conductor roughness to feed into modern EDA tools is a prerequisite. This is especially true for long backplane channels.

Many EDA tools include the latest and greatest models for conductor surface roughness and wide-band dielectric properties. But obtaining the right parameters to feed the models is always a challenge. So how do we get these parameters?

One way is to follow the design feedback method which involves designing, building and measuring a test coupon. After modeling and tuning various parameters to best fit measured data, D_k, D_f and roughness parameters can be extracted. They are then used in

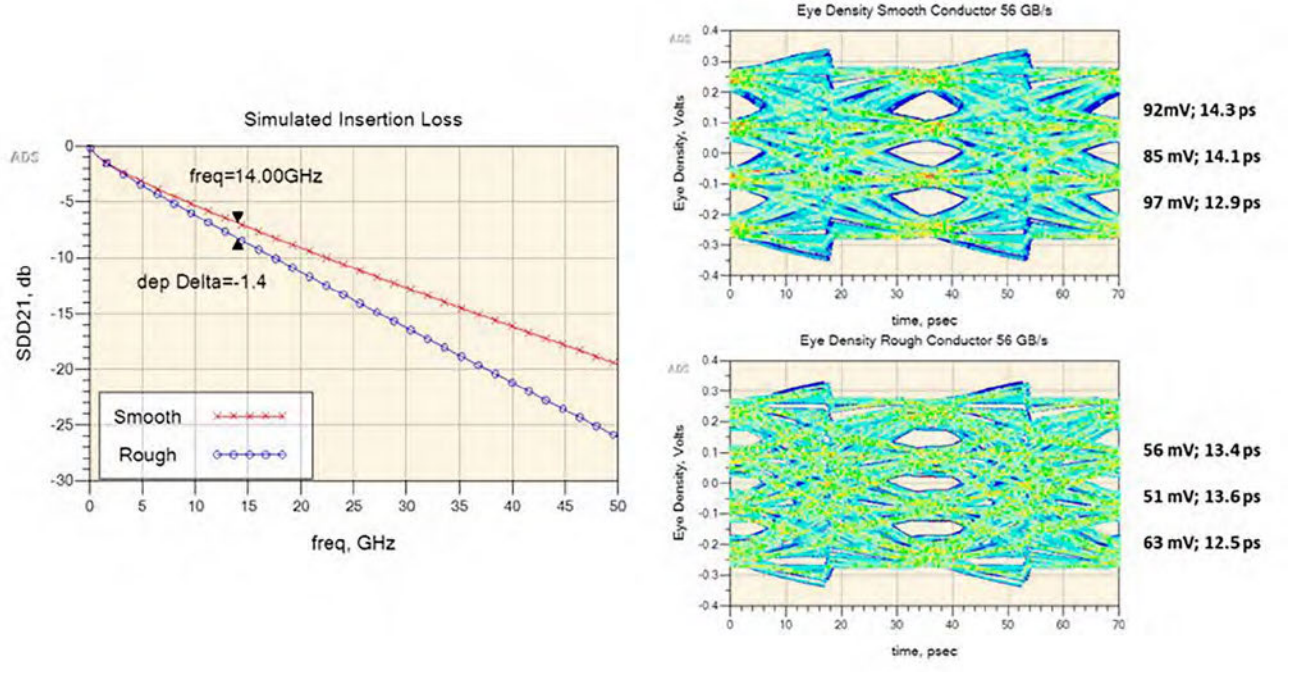


Figure 1: Simulated results of a differential transmission line with and without conductor roughness taken into account. With just 1.4 dB delta in insertion loss, as shown on the left, results in an average reduction of 38% in eye height and increase of 4.3% in jitter across all three eyes, as shown on the right.

Your signal needs to get around the world fast... Why go halfway around the world to get your high-speed PCBs?

ACE: your high-speed experts right here at home, specializing in microwave and hybrid PCBs.

ACE
ACCURATE
CIRCUIT
ENGINEERING

Accurate Circuit Engineering
3019 Kilson Dr
Santa Ana, CA 92707

(714) 546-2162 • sales@ace-pcb.com

For technical assistance, call:
James Hofer
(714) 227-9540

www.ace-pcb.com

RoHS & WEEE compliant • Certified AS9100, ISO, ITAR, MIL-PRF-31032 & 55110

channel modeling software to design the final product.

The benefits of this method are that it is practical and accurate—if you use the exact same material, glass style and copper foil in your final board stack-up. On the down side, a significant amount of expertise and equipment is required to design, build and measure the test coupon, which takes significant amount of time and money.

But, as my friend Eric Bogatin often likes to say, "Sometimes an OK answer now is better than a good answer later." As a high-speed signal integrity practitioner and backplane architect, I often must come up with an answer sooner rather than later, because of the impact to time and cost to my clients. And that's why I have been motivated over the last few years to research and develop a simple methodology to accurately determine parameters to feed into modern EDA tools.

Often the only sources are from manufacturers' data sheets. In most cases, the numbers do not translate directly into parameters needed for the EDA tools. One example is modeling copper foil roughness parameters.

Many tools include the Hammerstad model[3] and more recently the Huray model[4] to correct conductor loss due to roughness. The Hammerstad model has been used for decades, since all that was required was the RMS value of the peak to valley roughness parameter from data sheets. But it loses accuracy after 3-15 GHz, depending on the roughness of copper foil.

The Huray model has gained popularity over the last few years. It is based on non-uniform distribution of spheres resembling "snowballs" applied to a matte base. Although it is quite accurate, it is always difficult to obtain the right parameters for number of spheres, sphere radius and tile base area.

It is theoretically possible to build an accurate snowball model of the surface roughness by extracting parameters through detailed analysis of scanning electron microscopy (SEM) photographs. But practically, it is beyond the capabilities of most companies who do not have access to such equipment, and doesn't help you if you want that "OK answer now."

The Cannonball-Huray Model

This leads into what I like to call my Cannonball-Huray model. Using the concept of cubic close-packing of equal spheres, the spheres radius (a_i) and tile area (A_{flat}) parameters for the original Huray model can now be easily estimated solely by the roughness parameters published in manufacturers' data sheets[2].

The Cannonball-Huray model can be used to optimally represent the surface roughness. As illustrated in Figure 2 there are three rows of spheres stacked on a square tile base. Nine spheres are on the first row, four spheres in the middle row, and one sphere on top. The height of the Cannonball stack is equal to the 10-point mean roughness R_Z as published in the foil manufacturer's datasheets.

If we can peer into the stack, and visualize a pyramid lattice structure connecting to all the

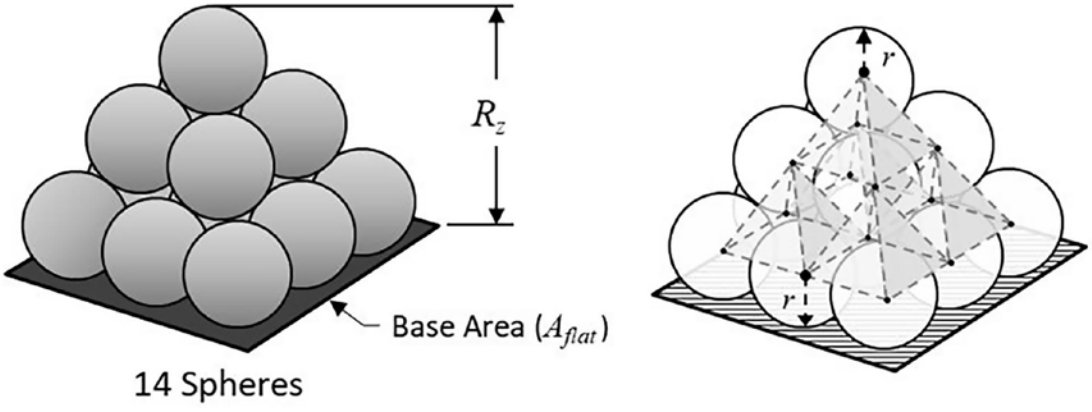


Figure 2: The Cannonball-Huray physical model.

centers of the spheres, then the total height of the Cannonball stack is equal to the height of two pyramids plus two radii.

Through simple geometry and a little bit of algebra we can approximate the radius of a single sphere (r) as[2]:

$$r \approx 0.06 R_z \qquad \text{Equation 1}$$

And base area (A_{flat}) as:

$$A_{flat} = (6r)^2 \qquad \text{Equation 2}$$

Because the model assumes the ratio of A_{matte}/A_{flat} = 1, and there are only 14 spheres, the Cannonball-Huray model can therefore be simplified as:

$$K_{SR}(f) = 1 + \frac{84\pi r^2}{A_{flat}} \div \left(1 + \frac{\delta(f)}{r} + \frac{\delta^2(f)}{2r^2}\right) \qquad \text{Equation 3}$$

Where: K_{SR} (f) = roughness correction factor, as a function of frequency; δ (f) = skin-depth, as a function of frequency in meters; r = the radius of spheres in meters; A_{flat} = base area in sq. meters.

Effective Dk Due to Roughness

Everyone involved in the design and manufacture of PCBs knows that one of the most important properties of the dielectric material is D_k. We often assume the value reported in manufacturers' data sheets is the intrinsic property of the material. But in fact, it is the effective dielectric constant (D_{keff}) generated by a specific test method. When you compare simulation against measurements, you will often see a discrepancy in D_{keff}, due to increased phase delay caused by surface roughness.

If D_k and R_z roughness parameters from the manufacturers' data sheets are known, then the effective D_k due to roughness (D_{keff_rough}) of the fabricated core laminate can now be easily estimated by [1]:

$$D_{keff\_rough} \approx \frac{H_{smooth}}{(H_{smooth} - 2R_z)} \times D_k \qquad \text{Equation 4}$$

Where: H_{smooth} is the thickness of dielectric from data sheet; R_z is 10-point mean roughness from data sheet; Dk is dielectric constant from data sheet.

As I mentioned earlier, there are many EDA tools that implement the Huray model. The Polar Instruments Si9000e 2017 field solver [5] now includes the Huray roughness model, and it is now one of my go-to tools for helping me get an "OK answer now." I especially like it because the user interface is so intuitive and easy to use.

Practical Modeling of a High-speed Backplane Channel Case Study

A traditional high-speed serial link backplane channel model has three separate parts. They are two plug-in circuit cards and a backplane. Neglecting vias, the high-speed channel can be quickly modeled as three separate transmission line segments with connectors in-between.

Each transmission line segment is modeled separately using Polar Si9000e field solver. The S-parameters are then saved as touchstone format to be brought into a channel modeling software tool like Keysight ADS [6].

The best way to demonstrate this is through a practical case study example. I will use the Amphenol-FCI Examax demo platform. This is a platform I helped design in 2013 to showcase the Examax connector performance at 28GB/s NRZ.

A picture of the platform is shown in Figure 3. Among other test structures designed into the backplane, there are four channels with different overall lengths. For simplicity only one channel topology shown will be used for comparison in this case study. The PCBs were fabricated with Nelco N4000-13epsi material [7] clad with VSP foil from Oak-Mitsui [8]. The respective transmission line design and data sheet parameters are summarized in Table 1.

The first step is to determine the effective D_k due to roughness for the cores and prepregs used on the daughter cards and backplane. By applying Equation 4 to the respective values in Table 1, the D_{keff} results are summarized in Figure 4.

The next step is to determine the radius of spheres and base tile area for Huray model, as summarized in Figure 5. Because electro-deposited (ED) foil has a matte side and drum side,

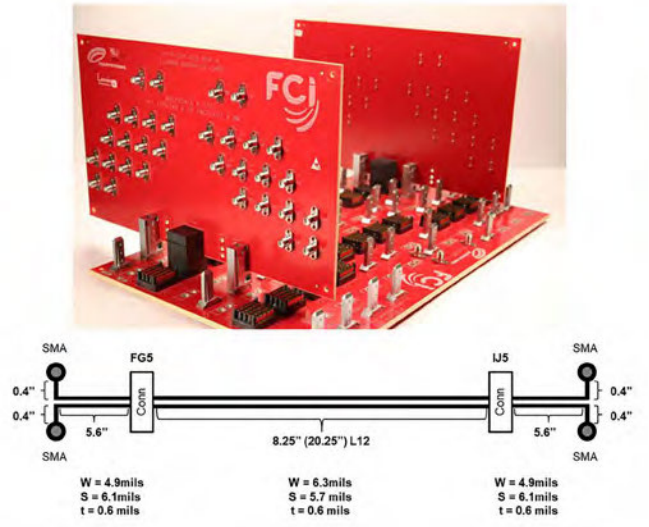


Figure 3: Amphenol-FCI Examax demo platform and channel topology summary used for case study.

Parameter	N4000-13EPSI Backplane	N4000-13EPSI Daughter Card
D_k Core/prepreg @ 10GHz	3.08/3.06	3.04/3.06
D_f Core/prepreg @ 10GHz	0.0083/0.0084	0.0085/0.0084
R_z Matte side	2.5 μm	2.5 μm
R_z Drum side	1.5 μm	1.5 μm
Trace thickness, t	0.6 mils	0.6 mils
Trace width, w_1	6.3 mils	4.9 mils (Diff) 5.4 mils (SE)
Trace width, w_2	5.7 mils	4.3 mils (Diff) 4.8 mils (SE)
Trace separation, s	5.7 mils	6.1 mils
Core thickness, H1	6 mils	4 mils
Prepreg thickness, H2	5.8 mils	5.8 mils

Table 1: Design parameters and data sheet summary.

Daughter Card

$$D_{keff\_prepreg} = \frac{H_{smooth}}{\left(H_{smooth} - 2R_{z\_drum}\right)} \times D_{k\_prepreg}$$
$$= \frac{6.2mils \times 25.4}{\left(6.2mils \times 25.4 - 2 \times 1.5\mu m\right)} \times 3.06$$
$$= 3.12$$

$$D_{keff\_core} = \frac{H_{smooth}}{\left(H_{smooth} - 2R_{z\_matte}\right)} \times D_{k\_core}$$
$$= \frac{4.0mils \times 25.4}{\left(4.0mils \times 25.4 - 2 \times 2.5\mu m\right)} \times 3.04$$
$$= 3.20$$

Backplane

$$D_{keff\_prepreg} = \frac{H_{smooth}}{\left(H_{smooth} - 2R_{z\_drum}\right)} \times D_{k\_prepreg}$$
$$= \frac{6.2mils \times 25.4}{\left(6.2mils \times 25.4 - 2 \times 1.5\mu m\right)} \times 3.06$$
$$= 3.12$$

$$D_{keff\_core} = \frac{H_{smooth}}{\left(H_{smooth} - 2R_{z\_matte}\right)} \times D_{k\_core}$$
$$= \frac{6.0mils \times 25.4}{\left(6.0mils \times 25.4 - 2 \times 2.5\mu m\right)} \times 3.08$$
$$= 3.18$$

Figure 4: Effective D_k due to roughness summary of cores and prepregs used on the daughter cards and backplane.

with different roughness parameters, we must calculate the sphere radius for each side separately. But most Huray models in EDA tools, including Polar Si900e, only allow one input for radius so I just take the average of the two for an effective radius (r_{eff}). Once we have that then it is easy to get the area (A_{flat}) of the flat tile base.

For each length of transmission line of the topology shown in Figure 3, we would create and save a separate Polar file by following steps for each file:

1. The first step for modeling each transmission line segment is to select the "Lossless Cal-

A BETTER IDEA

Valor® NPI
DFM JUST GOT EASIER!

Valor NPI software is industry's only automated PCB DFM solution, seamlessly connecting PCB design, fabrication, assembly and test processes.

With the latest version of Valor NPI, setup time for DFM rules can be reduced from weeks to days, and DFM results viewing time can be reduced by up to 50 percent.

LEARN MORE AT **HTTP://WWW.MENTOR.COM/NPI**

Mentor®

A Siemens Business

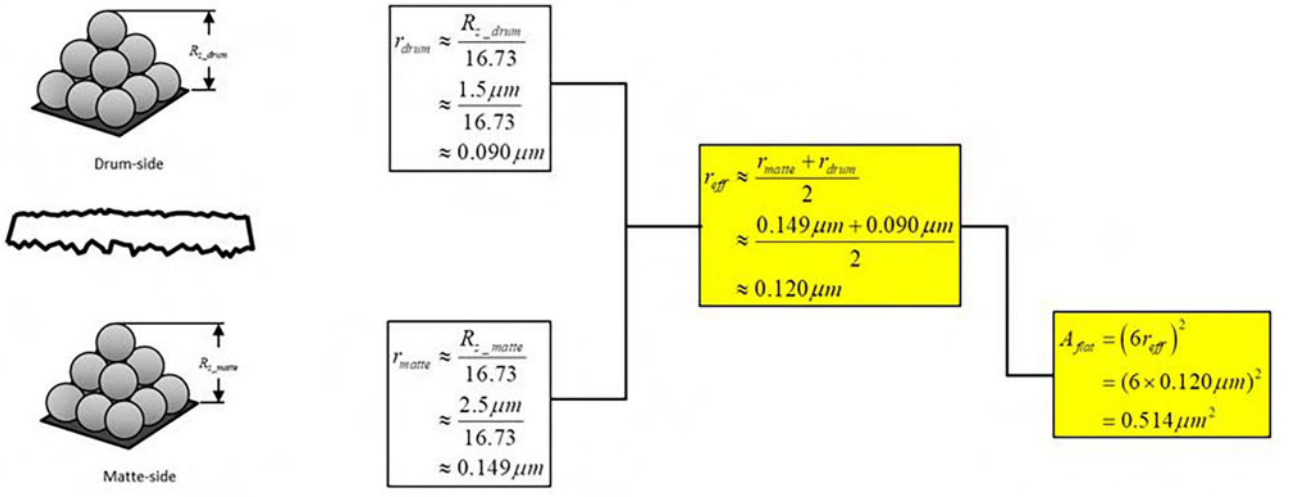


Figure 5: Summary to determine effective sphere radius (r_{eff}) and flat tile area (A_{flat}) parameters for input into a Polar Si900s Huray model.

culation" tab at the bottom of the Si9000e main input window. When the pop-up window appears, choose the appropriate transmission line geometry from the pallet along the left-hand side, and then enter the specific design parameters in the boxes. Change the various parameters until the desired impedance is reached

2. The next step is to select the "Frequency Dependent Calculation" tab at the bottom of the input panel and enter line length, conductivity and frequencies in the appropriate boxes in the main window.

3. Under the "Extended Substrate Data" section, choose "Causally Extrapolate Er / TanD" radio button and click "Edit" to enter the D_{keff} parameters in a pop-up window as shown. Click "Calculate" to view causal D_{keff} over frequency. Click "Close" to return to main window.

4. Under the "Surface Roughness Compensation" section from the main window, select Huray radio button and click "Edit" to enter the appropriate roughness parameters in the pop-up window. Enter r_{eff} and A_{flat} in the boxes shown. Enter 1.00 for "Ratio of Areas" and 14 for the "Number of Balls in Area" boxes. Click "Apply" to return to main window.

5. In the main window, hit calculate. Once the simulation has run, then export the respective touchstone file under the "File" menu.

After repeating this for each transmission line segment of the topology, there should be three touchstone files generated. One file is for the single-ended traces on the daughter card. Another one is for the differential pair on the daughter card and the last one is for the differential pair on the backplane.

Keysight ADS is used to model and simulate the entire backplane channel, as shown in Figure 7 . The two schematics in Figure 7A use the S-parameter pallet to model and compare the channel in the frequency domain. The two schematics in Figure 7B use the "ChannelSim" pallet for transient simulation and eye diagram analysis. All the Polar generated s-parameter files are concatenated together, as shown, including the Examax connector s-parameter files. Via and coax connector models are not included, because I want that "OK answer now." You can always model and add them later to get that "good answer later" if need be.

The results of the simulation are plotted in Figure 8. As you can see there is excellent correlation for both differential SDD21 insertion loss on the left and differential time-domain reflectometry (TDR) TDD11on the right.

Figure 9 shows plots of transmit eyes on top and receive eyes on bottom at 28GB/s. The simulated channel is on the left and the measured channel is on the right. Even though the measured transmit eye on the top right shows slightly more noise and jitter, the received eyes are virtually the same, suggesting the "OK

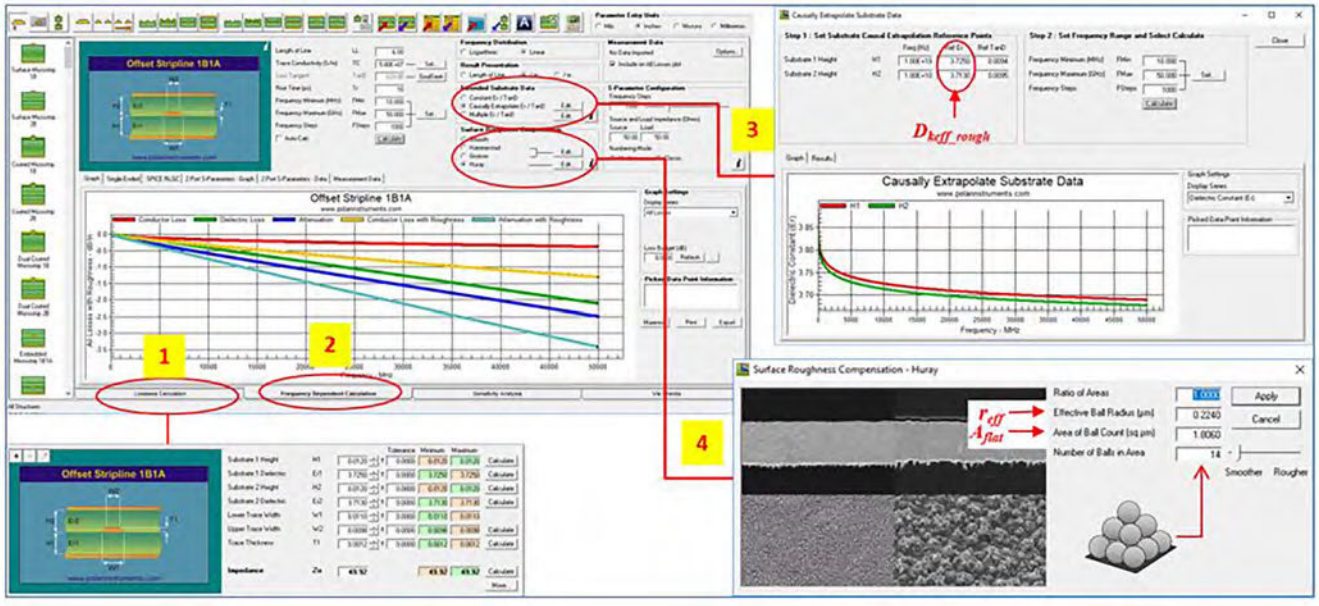


Figure 6: Generic Polar Si900e user interface window and pop-up panels to enter required parameters.

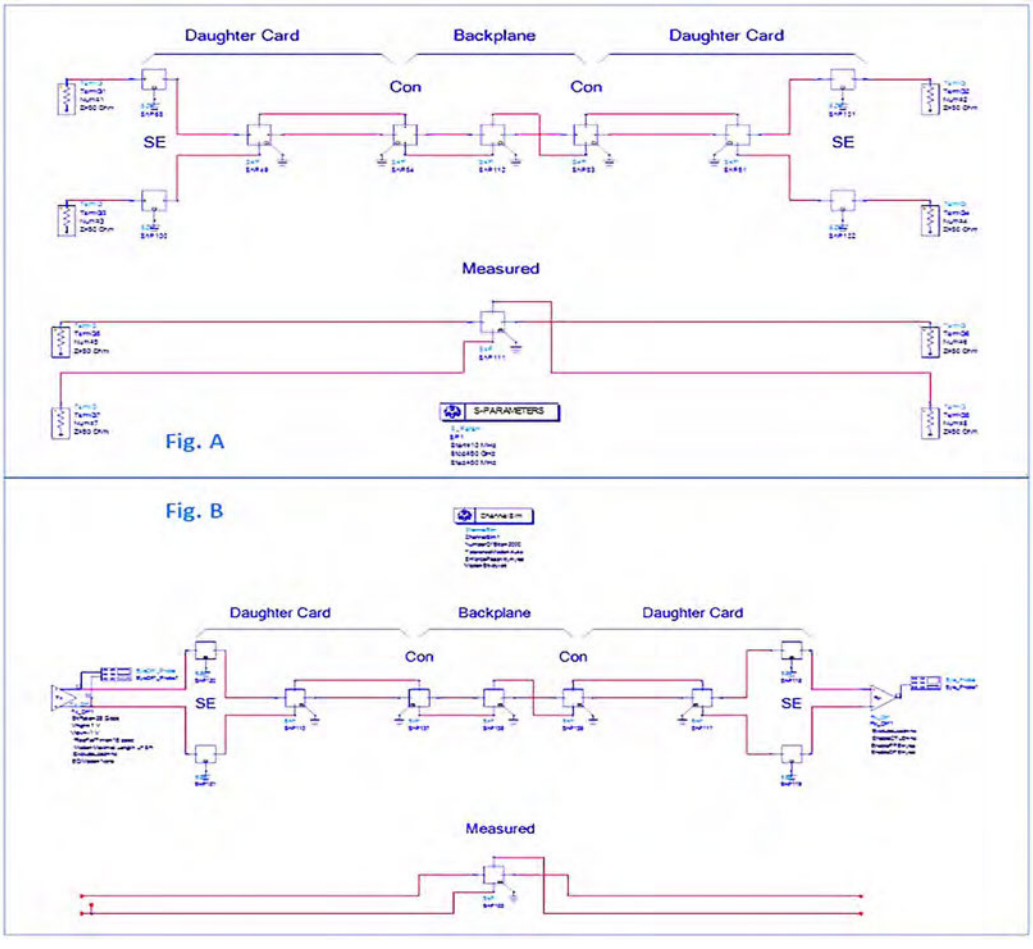


Figure 7: Keysight ADS generic topology models for frequency domain (A) and transient channel simulation analysis (B).

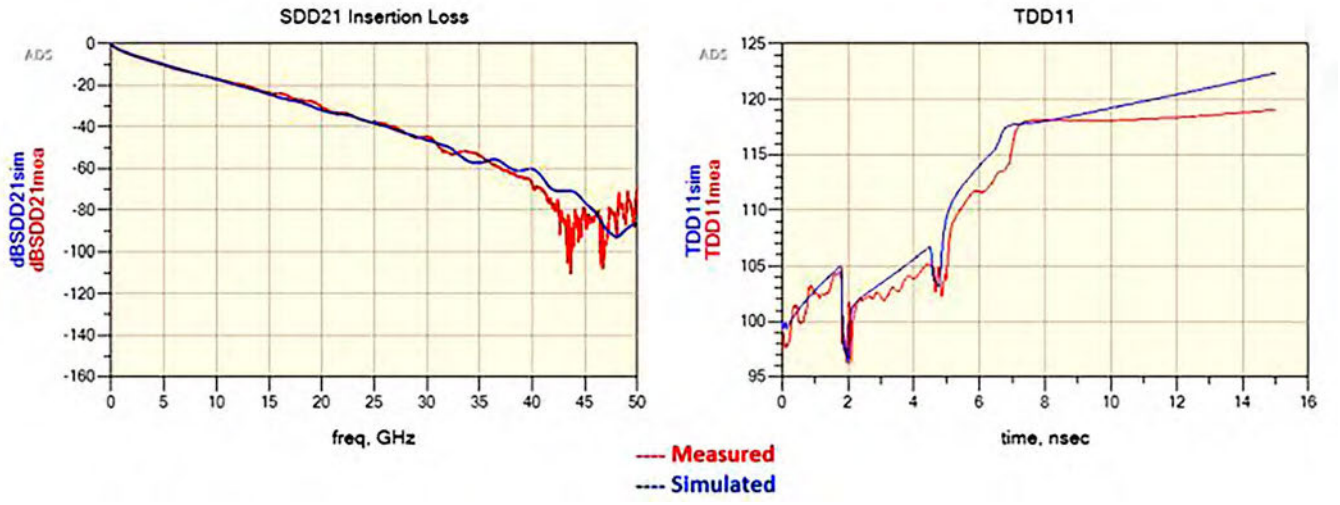


Figure 8: Simulated differential insertion loss (SDD21) shown on left and differential TDR (TDD11) shown on right.

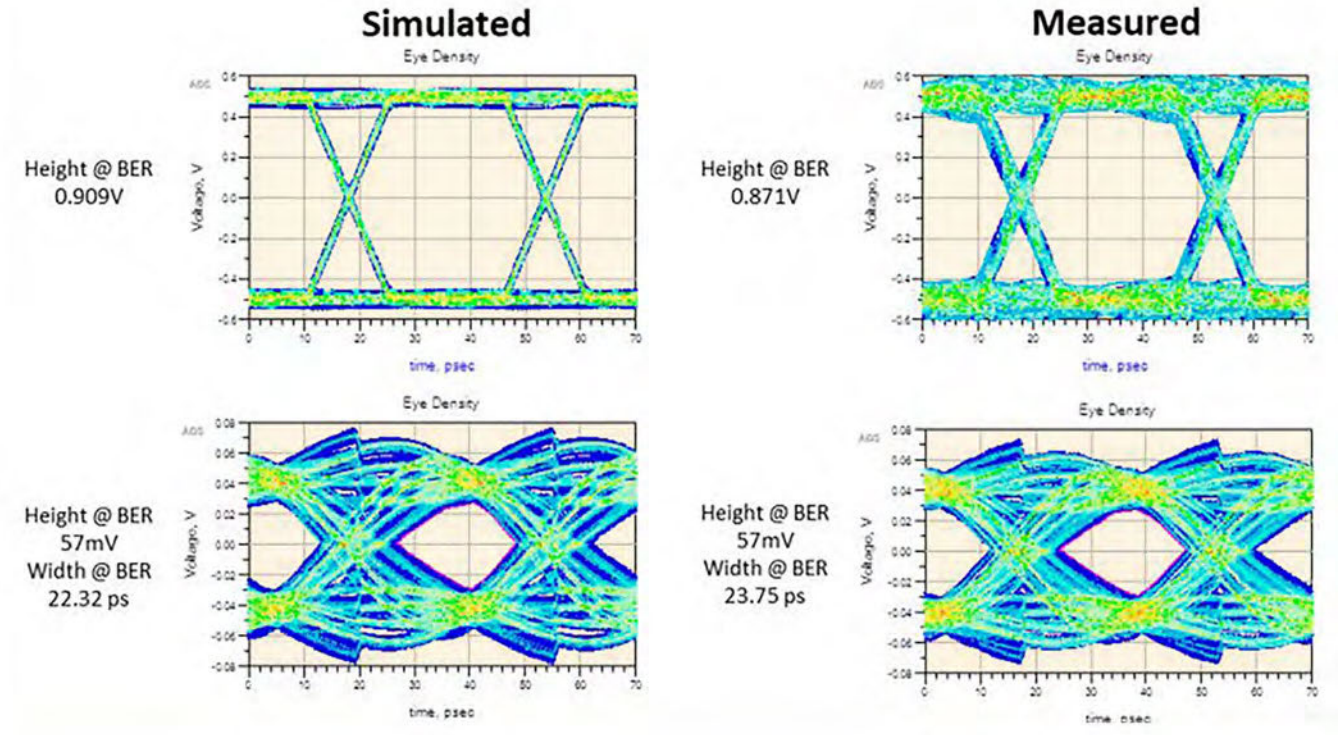


Figure 9: Channel simulation at 28 GB/s. Total length = 20.25".

answer NOW!" is probably good enough to make an engineering decision.

Summary

By using the Cannonball-Huray model, with copper foil roughness and dielectric material properties obtained solely from manufacturers' data sheets, a practical method of modeling high-speed channels is now achievable using commercial field-solving software employing Huray model.

If you need an OK answer now instead of a

good answer later, then this method might be right for you. **PCBDESIGN**

References

1. Bert Simonovich, "A Practical Method to Model Effective Permittivity and Phase Delay Due to Conductor Surface Roughness," DesignCon 2017 Proceedings, Santa Clara, California, 2017.

2. Bert Simonovich, "Practical Model of Conductor Surface Roughness Using Cubic Close-packing of Equal Spheres," EDICon 2016, Boston, Massachusetts.

3. Hammerstad, E.; Jensen, O., "Accurate Models for Microstrip Computer-Aided Design," Microwave Symposium Digest, 1980 IEEE MTT-S International, pp.407,409, 28-30 May 1980 doi: 10.1109/MWSYM.1980.1124303.

4. Huray, P. G. (2009) "The Foundations of Signal Integrity," John Wiley & Sons Inc., Hoboken, NJ, USA., 2009.

5. Polar Instruments Si9000e Version 2017.

6. Keysight Advanced Design System (ADS) Version 2016.

7. Park Electrochemical Corp. Nelco Digital Electronic Materials.

8. Oak-Mitsui.

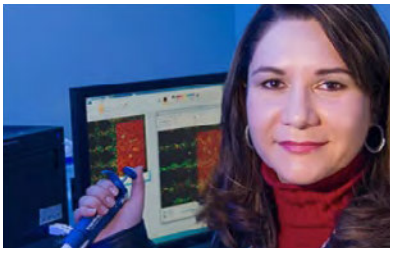
Bert Simonovich is the founder of Lamsim Enterprises, where he provides innovative signal integrity and backplane solutions to clients. His current research interests include signal integrity, high-speed characterization, and modeling of high-speed serial links associated with backplane interconnects. To contact him or read past columns, click here.

Hybrid Biological Cell Separations Technology for Lab-On-Chip Medical Devices

Research being done at Rochester Institute of Technology to refine lab-on-chip devices will provide more detailed and timely information to detect diseases such as cancer.

Blanca Lapizco-Encinas, a faculty-researcher in RIT's Kate Gleason College of Engineering, is improving the process of separating biological cells and biomolecules using chromatography principles, a well-established technique for separating proteins, combined with a newer technique called dielectrophoresis, a process that uses electrical current to separate biomolecules.

In biomedical analysis, clinicians may have to analyze complex blood samples consisting of cells, proteins and other micron-sized particles, in an effort to separate healthy and diseased cells. Improved microfluidic techniques with the potential to separate cells found in bio-fluids, are useful in settings where rapid results are essential such as testing for food and water safety or clinical analysis of disease.



"You put into a device a sample with six or seven different types of particles and you can separate them, in some cases in less than two minutes, just by applying electric fields," Lapizco-Encinas explained.

The new research, utilizing electroosmotic flow is expected to drive particles across the microchannel. This process of electroosmotic flow offers the potential for the biomolecules to be manipulated in real-time, allowing for dynamic separation schemes. This work expands Lapizco-Encinas' previous research that focused on the development of multi-channel devices where fluid samples are assessed after being exposed to electrical currents that cause the bio-particles to separate for more efficient analysis. Through past research, she and her team advanced device system designs and determined an optimal threshold of electrical fields applied to adequately manipulate the fluids and ensure that live cells are not damaged. Adding chromatographic principles to this foundational work is underway.

Causal Power Plane Models

by Istvan Novak
ORACLE

Causal and frequency-dependent models and simulations are important for today's high-speed signal integrity simulations. But are causal models also necessary for power integrity simulations? When we do signal integrity eye diagram simulations, we define the source signals, so if we use the correct causal models for the passive channel, we will get the correct waveforms and eye reduction due to distortions on the main path and noise contributions from the coupling paths.

The details of the simulated waveforms will make a difference in the accuracy of the eye closure; in such cases the causality of the passive component models is important. At the other end of the spectrum, when we do point-of-load PDN simulations, causality today is much less important, not because we don't care for the accuracy of the result, but primarily because the excitation signal, the signature of the current demanded by the load as a function of time, is usually not known very well. One of the areas in between, which involves PDN models and requires good causal models is when we do SI-PI co-simulation. For instance, when we want to simulate the eye closure due to simultaneous switching noise and PDN noise on memory signals, the memory excitation signals are set by us and therefore it makes sense to use good causal models for the PDN to get accurate results. This article shows you a few important points how you can achieve it.

For any interconnect, which has non-negligible delay for the particular application (in technical terms: which is not electrically short), we need to use a simulation model that describes not only the interconnect impedance, but its propagation delay as well. Extrapolating from the world of lumped circuits, cascaded segments of series inductance and parallel capacitance is a simple and brute-force approach to model both impedance and delay. A simple ladder circuit shown in Figure 1 can be used to simulate the approximate behavior of package pins, connector pins, traces and cables.

This model represents a lossless interconnect with 50-ohm characteristic impedance and 150 ps delay in each segment, a total of 450 ps delay for the three cascaded segments. The model works well if the equivalent rise time of the signal we want to pass through this circuit is much longer than the delay in one segment. If all what we want to accurately simulate is the rise time of the signal passing through this circuit, this ratio can be as low as three to four. If we need good accuracy of the entire waveform,

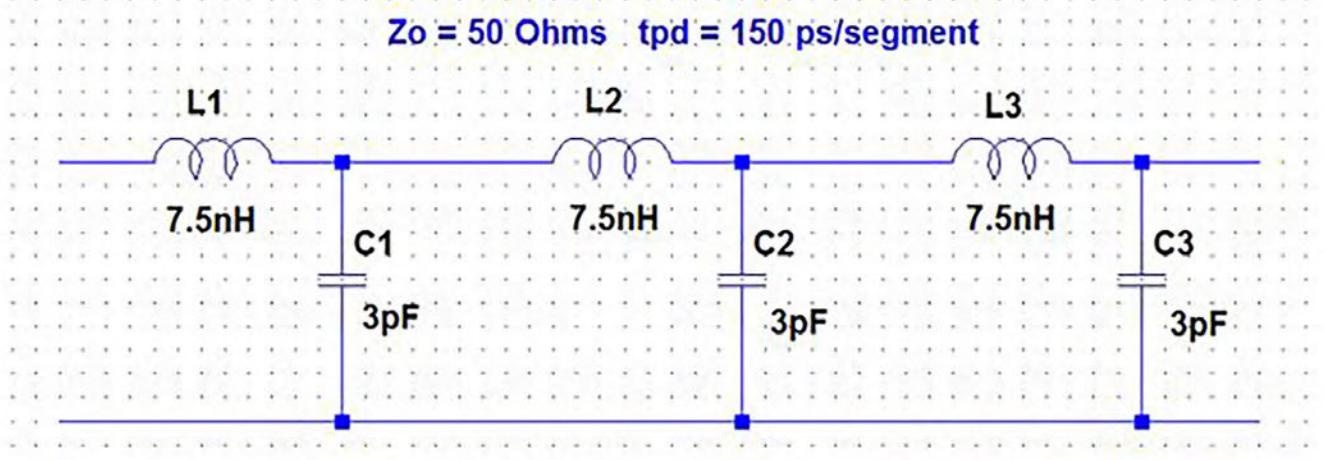


Figure 1: Ideal one-dimensional LC ladder.

It's the little things.

The flat-track racing champions at Vance & Hines know: when you're rocketing down the racetrack at nearly 200 mph, a lot of little things, like a gust of tailwind or a well-tuned exhaust system, can add up to victory — or defeat.

The same is true for PCB prototyping and production. **Little things, done right, add up to a competitive advantage for your business.**

From our design recommendation that helped get their new fuel management **product to market faster** — to the proactive phone call from one of our meticulous employees that **saved an entire production run** of unusable boards and **prevented a gap in inventory**. These little things are what keeps Vance & Hines coming back to Sunstone Circuits for over a decade.

Learn more at: www.sunstone.com/littlethings

*"Instead of robotically manufacturing boards, Sunstone has a thought process behind their work... We have more opportunities to **gain competitive advantage** because we know our PCB partner can handle anything..."*

Larry Hinds

MANUFACTURING MANAGER,
VANCE & HINES

SUNSTONE CIRCUITS

Contact us at: 1-800-228-8198
or via e-mail at support@sunstone.com

say down to one percent, we need a ratio of ten to twenty. If we take the tighter accuracy estimate of twenty, the signal passing through this example network should have a rise time of 20 * 150 ps = 3 ns, or longer. This limits the bandwidth to approximately 100 MHz. If we need wider bandwidth, we can proportionally scale the L and C values.

For instance, using L = 0.75 nH and C = 0.3 pF will produce a 50-ohm interconnect model with a bandwidth of 1 GHz, but if we need the same 450 ps end-to-end delay, we will need to use ten times more, namely thirty cascaded segments. This model is so simple that any circuit simulator can take it, but to achieve high accuracy and high bandwidth at the same time, we may end up with a lot of circuit nodes and considerable run time. Of course, for the ideal lossless case we have in Figure 1, we could just use a single SPICE Tline element with the required characteristic impedance and total delay, but that way we would lose the horizontal connectivity [1].

Package or connector pins, traces and cables are one-dimensional transmission lines in the sense that most of the signal will only propagate along the conductor. Power planes are two-dimensional transmission lines: any signal (mostly the power noise) can and will propagate in any direction on the plane. To model this two-dimensional nature, we can take the ladder equivalent circuit from Figure 1 and turn it into a two-dimensional grid circuit. Figure 2 shows the conceptual circuit diagram.

Each subcircuit in the grid can be one LC segment from Figure 1 with appropriate L and C values. The calculation of the subcircuit element values is explained in [2]. If we have plane outlines or slots/cutouts in the planes that cannot be easily approximated with rectangular shapes, the same grid concept can be extended to utilize variable-size grid cells [3]. The simulation models based on grid equivalent circuits will provide results at each of the circuit nodes; in between circuit nodes we need to rely on interpolation. Alternately, for simple plane shapes, analytical formulas can also be used to simulate the self and transfer impedance of planes at any arbitrary point [4].

Of course, today we have a number of commercial 2.5D tools available that can simulate two-dimensional structures [5], [6], [7]. We could also use 3D tools, though simulating electrically very large structures that way is not really feasible.

Turning our attention back to causality: the model in Figure 1 is fully causal, but it is not only band limited, it represents only lossless interconnects. This means no series resistance representing the conductor losses, no parallel conductance to capture the dielectric losses, and as a result, the capacitance and inductance values are frequency independent constants. If we

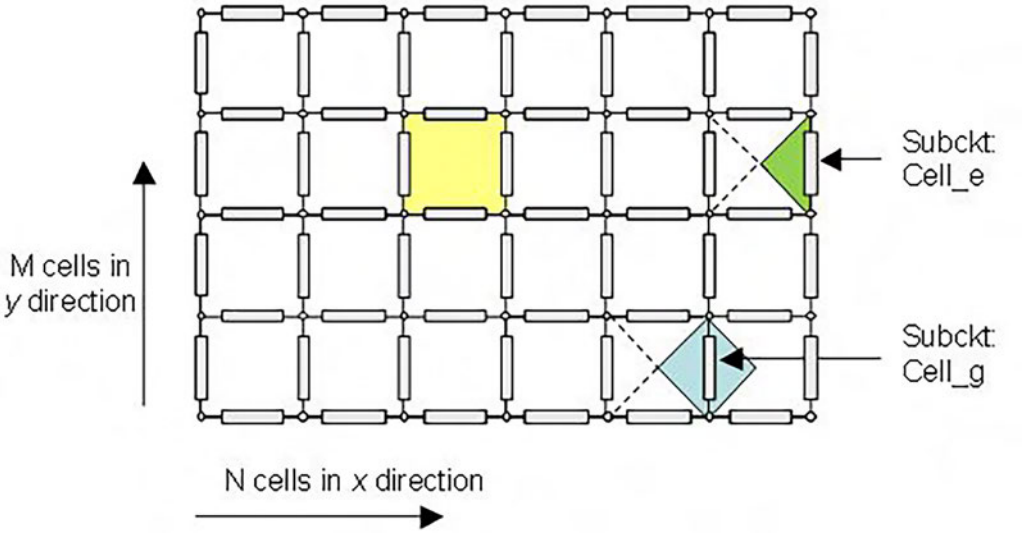


Figure 2: A two-dimensional SPICE grid network to simulate a pair of rectangular planes.

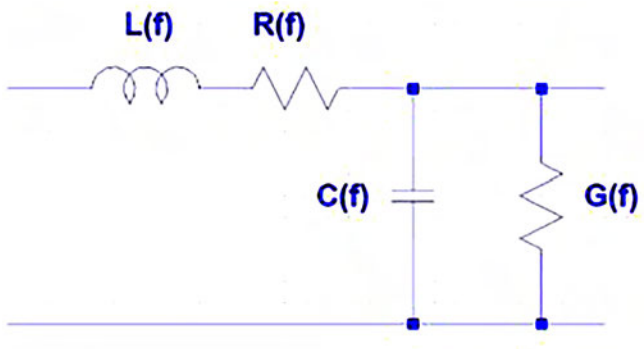


Figure 3: One segment of a generic, causal, lossy interconnect model.

want causal, lossy models, each segment needs to be represented with an RLGC network, where all four parameters are frequency dependent.

For the frequency-dependent C(f) capacitance and G(f) conductance we can use one of the causal dielectric models, for instance the wide-band multi-pole Djordjevic-Sarkar model [8]. The material constants can be taken from the laminate data sheet or from measurements [9]. For instance, based on the data sheet [10], a glass-reinforced FR406 4-mil core laminate at 1 GHz will have a Dk and Df value of 3.95 and 0.0161, respectively. If we chose an unreinforced HK04J25 1-mil polyimide laminate [11], the Dk and Df data sheet values at 1 MHz are 3.5 and 0.005, respectively. If one segment of the plane model represents one square inch area, the FR406 laminate model at 1 GHz will have 226 pF capacitance and 0.022815 S conductance; the HK04J25 laminate model at 1 MHz will have 800 pF capacitance and 0.0257 S conductance. For a causal model, we need these parameters as a function of frequency, which can be readily calculated based on the chosen wide-band multi-pole model [12].

Figure 4 and Figure 5 show the causal dielectric parameters as a function of frequency for the FR406 and HK04J25 laminates. On both figures the red dots on the left chart indicate the values provided by the data sheets.

To obtain the series elements of the equivalent circuit, we can start with the DC sheet resistance and asymptotic high-frequency spreading inductance of the planes. The DC sheet resistance depends on the thickness and conductivity of the conductor.

Assuming one-ounce (30 um) pure copper for each plane, the sheet resistance is approximately 0.6 mOhms for each square in each plane layer. The high-frequency spreading inductance is approximately 33 pH for each milli-inch dielectric thickness, resulting in a 132 pH for the 4-mil FR406 example and 33 pH

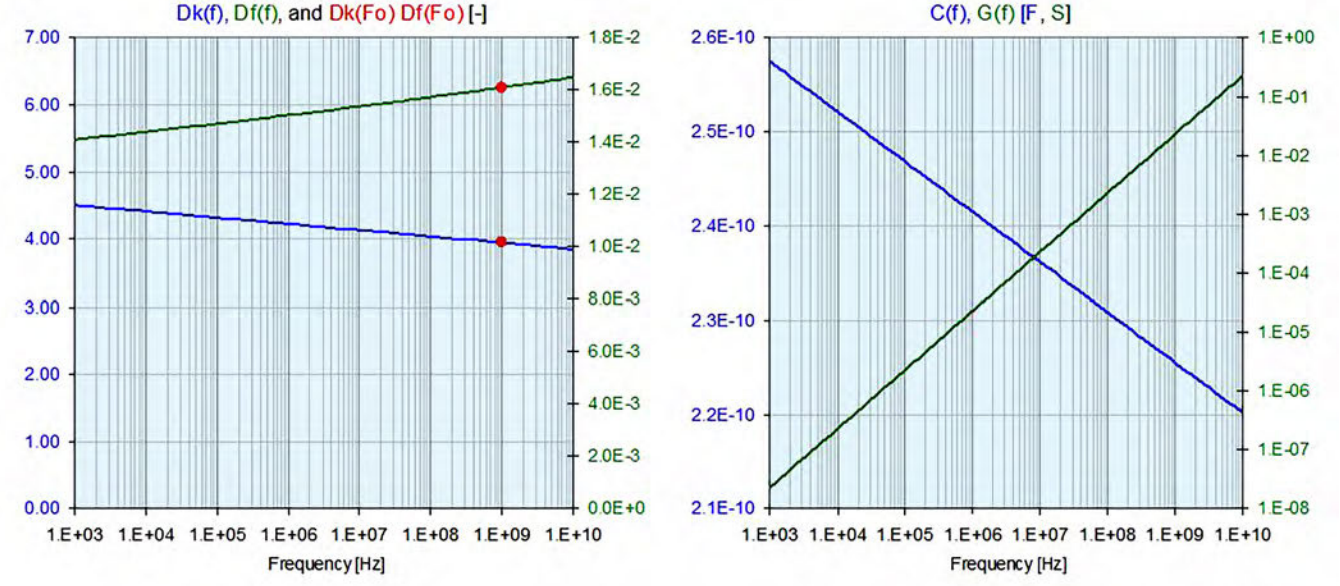


Figure 4: FR406 Dk(f) and Df(f) as a function of frequency (on the left) and C(f) and G(f) as a function of frequency for a one square inch of laminate (on the right).

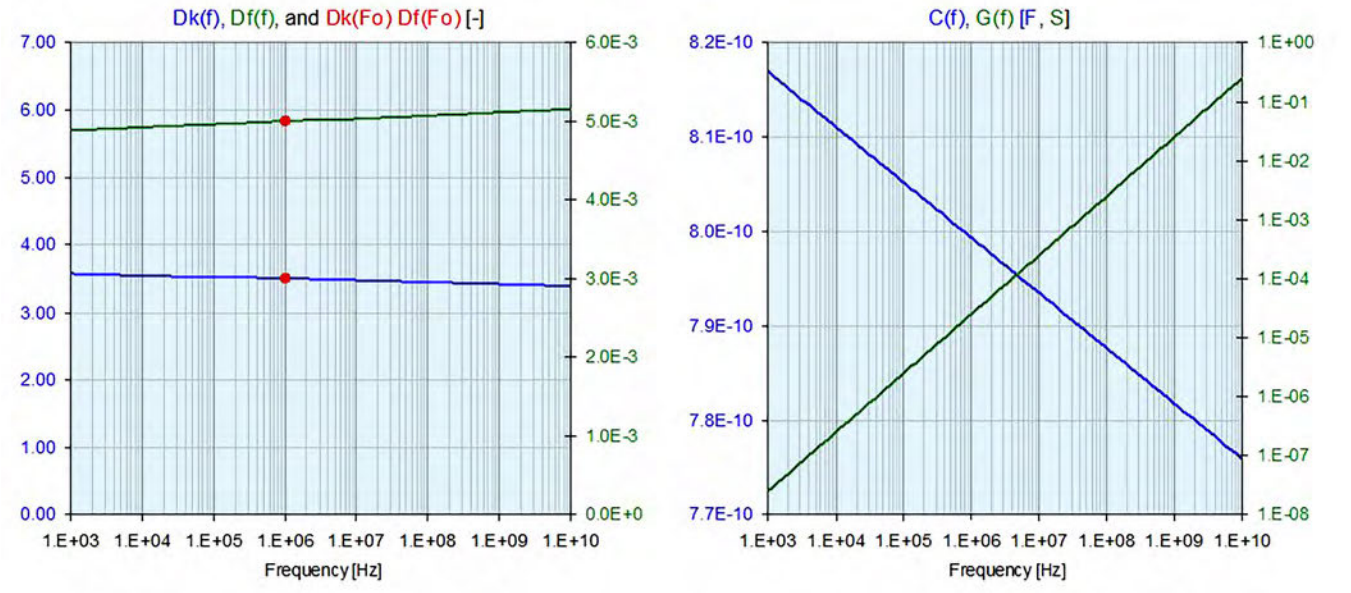


Figure 5: HK04J25 Dk(f) and Df(f) as a function of frequency (on the left) and C(f) and G(f) as a function of frequency for a one square inch of laminate (on the right).

for the 1-mil HK04J25 laminate example. Note that the resistance is given so far at zero frequency, whereas the starting point of the inductance is calculated at infinite frequency. The calculations assume that at DC the current penetrates vertically the plane thickness uniformly (large skin depth), but at infinite frequency the current flows only on the facing surfaces of the planes (very small skin depth).

At interim frequencies the current penetration depends on the ratio of the skin depth and conductor thickness. At each frequency we can calculate an effective plane separation, which is the dielectric thickness and the sum of the equivalent layer thickness values in the upper plane and lower plane. Similar calculations can be applied to obtain the

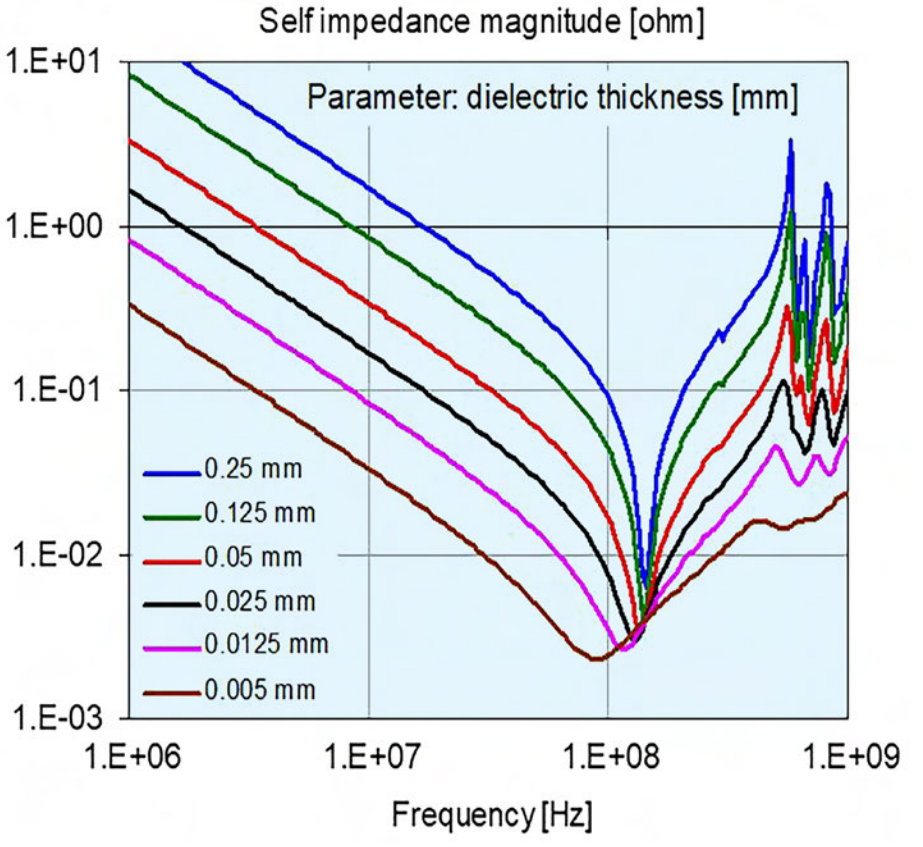


Figure 6: Self-impedance magnitude in the middle of a 10" x 10" FR-4 dielectric sheet between one ounce copper planes. The parameter is the dielectric thickness.

Ensure PCB Manufacturing Success!

CAM350®

Verify and Optimize PCB Designs for Successful Manufacturing.

BluePrint-PCB®

Create comprehensive documentation to drive PCB fabrication, assembly and inspection.

DFMStream™

Verify Design and Manufacturing Rules Any Time During the PCB Design Cycle.

©2016 DownStream Technologies, LLC. All rights reserved. All trademarks and registered trademarks are the property of their respective owners.

At DownStream Technologies we are committed to delivering comprehensive solutions and workflow process improvements for all your PCB design post processing needs.

Visit downstreamtech.com
or call 800-535-3226

DownStream Technologies

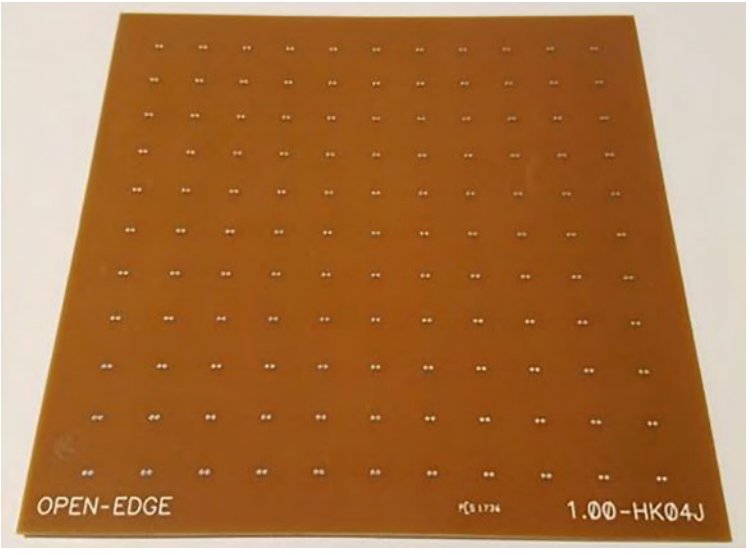


Figure 7: Photo of a 6" x 6" laminate test board, courtesy of DuPont.

AC resistance on the planes. If needed, corrections for surface roughness can be added, too.

The resulting causal grid model can be simulated in circuit simulators that can take frequency dependent components. Unfortunately, the original free Berkeley SPICE does not have this option, but as long as we need only AC simulations, there is a straightforward, though tedious workaround. We can calculate the actual RLGC values separately at each frequency point and then run SPICE AC simulations at those single frequencies. From the output files, we can put together the full frequency dependent causal response.

To illustrate the potentials of causal and frequency dependent plane models, Figure 6 shows how the lossy causal model captures the gradual suppression of modal resonances as the laminate gets thinner. We can see that with 10-mil (0.25 mm) plane separation the impedance swings are substantial at the resonance frequencies, and as we go to 1-mil or thinner, we get a significant reduction. As signal vias may go through these power-ground cavities, capturing the plane resonance correctly in frequency and magnitude becomes important, especially when we combine the plane models with signal interconnects for SI-PI co-simulation.

In a future column we will show the correlation between simulated and measured data for different test boards with different laminates. A peek preview of one such board is shown in Figure 8, courtesy of DuPont. The 6" x 6" open-edge board has a 1-mil HK04J25 laminate with one ounce copper.

So, the next time you do memory eye simulations with PDN effects included, make sure your models are causal and your tools can properly handle them. **PCBDESIGN**

References

1. "Be careful with Tlines in plane models"
2. "Simulating Planes with SPICE"
3. "Simulating Complex Power-Ground Plane Shapes with Variable-Size Cell SPICE Grids," 11th Topical Meeting on Electrical Performance of Electronic Packaging, October 21–23, 2002, Monterey, CA
4. Istvan Novak's home page
5. Cadence Design Systems
6. Ansys
7. Mentor
8. "Wideband frequency-domain characterization of FR-4 and time-domain causality," IEEE Trans. Electromagn. Compat., vol. 43, no. 4, pp. 662–667, Nov. 2001.
9. "Frequency domain analysis and electrical properties test method for PCB dielectric core materials," DesignCon 2003 East, Boston, MA, Jun. 2003.
10. Isola
11. DuPont
12. Istvan Novak's home page

Dr. Istvan Novak is a distinguished engineer at Oracle, working on signal and power integrity designs of mid-range servers and new technology developments. With 25 patents to his name, Novak is co-author of "Frequency-Domain Characterization of Power Distribution Networks." To contact Novak or read past columns, click here.

IPC-2581 CONSORTIUM

Axiom has built over 500 different designs that were handed off by their customers in IPC-2581 format. Use of IPC-2581 streamlines our process of preparing the machines for a job by over 30%. We believe that the IPC-2581 standard enhances the complete supply chain, helping all electronic industry sectors bring sophisticated electronic assemblies to market at a reduced time and cost through streamlined communications.

Jim Pierce
Axiom Electronics LLC

To learn more about IPC-2581 Consortium, please visit **www.ipc-2581.com**

Axiom Electronics

PCB007 Highlights

One World, One Industry: The Future of Electronics in the Automotive Industry

Automotive electronics is not a new topic. While there is a trend for both performance and luxury electronics, many of the recent conversations tend to focus on self-driving/autonomous vehicles. While the technology is exciting, it is just the tip of the iceberg.

Punching Out! Making the Process Easy (M&A Process Engineering)

In the M&A world, there are companies that make it easy (or at least easier) and those that make it difficult. By making the process easier, sellers should see better valuations and terms, and have a smoother deal process.

Flex Talk: Knowledge is Power

"What can I do to help drive cost from my design?" This is a question that I am asked routinely. That question is often followed by, "Can I get these faster?" Both questions are even more predominant when talking about flexible circuits or rigid-flex.

'Global Wisdom. Local Presence' the Theme of HKPCA & IPC Show 2017

The 2017 International Printed Circuit & APEX South China Fair (2017 HKPCA & IPC Show) will again be staged at the Shenzhen Convention & Exhibition Center, China. This year's edition will run from December 6–8, 2017. With the theme of "Global Wisdom. Local Presence," it is hoped that global collective intelligence can be drawn to the show for assisting industry insiders to apply those high-end technologies into local production and enhance their business development.

Weiner's World—August 2017

IPC is planning to hold a special meeting on automotive electronics for senior executives during IPC APEX EXPO 2019. The meeting will be planned and produced by the IPC Ambassador Council. Its presentations will feature senior members of the entire automotive electronics supply chain.

It's Only Common Sense: Train the Youngsters and Reveal the Possibilities

There is no doubt there is a shortage of young people in our business. As we all get older, the challenge of finding young people to replace us is getting more severe. Last week in this column, we talked about finding young people in our own organizations and then nurturing them to become an integral part of our companies.

Hamed El-Abd: A New Beginning, Part 1

While in China recently, Barry Matties joined longtime I-Connect007 friend and contributor Hamed El-Abd of WKK to congratulate him on his upcoming retirement. They reflected on his time spent in the industry, specifically in China, how far it's come, and where it might be headed next.

EPTE Newsletter: Semi-Annual Review of the Global Circuit Industry

Every piece of electronic equipment uses printed circuit boards. The circuit board industry posted mixed results for the first half of the year. Listed below is a quick snapshot of the global results as well as business trends for consumer electronics.

Scottish FPCB Manufacturer Flexible Technology Awarded EN9100

Rothesay-based PCB manufacturer, Flexible Technology, has just been awarded the coveted aerospace and defence approval, EN 9100, better known as AS9100.

All Flex Launches Analytical Service for Flexible Circuitry

All Flex assists users of flex circuits in understanding how to best apply and utilize flex. Analytical Service will help OEMs identify sources of failures and reliability risk of poorly designed flex.

COAST TO COAST CIRCUITS, INC.

TECHNOLOGY FROM COAST TO COAST

For over 40 years, we have been producing advanced solutions for our customers in many industries across the globe including Defense, Medical, RF/Microwave, Semiconductor and Down Hole Exploration among others. How can we add value to your next project?

LEARN MORE | CHECK OUT OUR CAPABILITIES

COAST to COAST CIRCUITS

Two Facilities. One Integrated Solution.

NEW YORK OPERATION
585.254.2980
sales@c3circuits.com

CALIFORNIA OPERATION
714.898.4901
sales@c3circuits.com

www.c3circuits.com

SiSoft Preparing for DDR5 Simulation Next Year

by Andy Shaughnessy
I-Connect007

DDR5 is expected to double the memory bandwidth and density of DDR4. I recently spoke with SiSoft Chief Scientist Walter Katz about his company's efforts to hit the market with this game-changing technology in 2018.

Andy Shaughnessy: I understand SiSoft is preparing for the upcoming DDR5 standard. What does this mean for the user?

Walter Katz: DDR5 is expected to range from 3,200 million transfers/second (MT/s) to 6,400 MT/s. These high data rates, when combined with the discontinuities inherent in DDR5 system topologies, will cause significant Inter Symbol Interference (ISI). This ISI will require that active equalization techniques be used in both the controller and memory I/O buffers to recover a usable signal, similar to what we have seen in serial channels for some time now. JEDEC is setting the standard for the equalization used in the memory chips, while equalization methods for the controller will be determined independently by each controller manufacturer. So let's focus on the memory devices. Currently, there is no requirement for equalization on the memory's driver (the memory read operation), while we expect to see a requirement for a four-tap decision feedback equalization (DFE) on the memory's receiver for both DQ write and address/command operations. A four-tap DFE adds (or subtracts) a voltage to the voltage at the receiver pad based on the values of the previous four symbols (bits) that have been received. There is also some consideration of including a peaking filter before the DFE in the memory's receiver; we'll have to wait and see how that plays out.

Shaughnessy: We're hearing about AMI models being used to model DDR5 data transfers. Can you give a brief summary of how an AMI works?

Katz: The IBIS-AMI, or AMI (Algorithmic Modeling Interface) was created in 2007 to help analyze high-speed SerDes (serialize/deserialize) channels. Today, those channels operate between 3 Gbps and 56 Gbps, and IBIS-AMI

Flexible, reliable Supply Chain Solutions

high quality copper clad laminates & prepreg bonding materials

ventec
INTERNATIONAL GROUP
騰輝電子

Ventec International Group is a world leader in the production of high quality and high performance copper clad laminates and prepregs, with full R&D and product development capabilities. Our global distribution means we can readily supply our products to all markets in all geographic areas.

productronica
Visit us in Hall B3 Booth 244

Ventec - wherever technology takes you, we deliver

Ventec International Group
179 Ward Hill Ave,
Ward Hill, MA 01835,
United States
T: 978-521-9700
E: ordersCA@ventec-usa.com
Follow @VentecLaminates

www.**venteclaminates**.com

Walter Katz

has been used to create hundreds of IBIS-AMI models for systems designers to use with their design simulations. At these frequencies, both ISI and loss are significant impairments, and the energy from a specific transition can affect the signal at the receiver from before the main body of signal itself arrives and for many unit intervals (UI) afterwards. Millions of bits need to be simulated to properly evaluate channel behavior, which is why IBIS-AMI has supplanted traditional SPICE methods for serial link analysis. AMI assumes that the I/O buffer analog models are linear and time invariant (LTI). The interconnect between the buffers is also LTI, which means the combination of the analog I/O and channel can be characterized using circuit simulation techniques and then combined with equalization models to predict the overall link behavior. The AMI models describe transmit (Tx)/receive (Rx) equalization behavior and are supplied as executable models in the form of dynamically linked libraries (DLL in Windows, shared objects in Linux) that are linked directly into EDA simulators at simulation runtime. The IBIS Open Forum is the industry organization responsible for the management of the IBIS-AMI specification. These executable models therefore model the detailed equalization behaviors of both the transmitter and receiver, while protecting the device manufacturer's IP because they are supplied as executable code. AMI models can be used to do two different types of simulations: statistical and time domain. Statistical simulations can predict the performance of simulations for essentially all possible patterns. Time domain simulations can more accurately handle non-linear and adaptive behavior in the buffers, but are typically limited to simulations that are 10 million UI long.

Shaughnessy: How would AMI models be used to model DDR5 topologies?

Katz: Serial channels are differential, point to point topologies with the clock embedded as part of the signal, while DDR5 channels are single ended, multi-drop topologies that use separate signals for data and the strobe (clock) signal used to sample the data. So, while we can apply AMI techniques to DDR5 analysis, we need to pay careful attention to the differences between the original applications of AMI modeling and how we apply those techniques to DDR5 applications. In its simplest form, we could approach DDR5 modeling with AMI the same way we approach serial channel modeling: characterize the analog channel, derive an impulse response and then process it with the algorithmic models to determine the effects of equalization. We simulate the analog channel in SPICE with a small rise time step to extract a step response with adequate resolution, then differentiate that to create the impulse response we need for algorithmic processing.

However, we should note that IBIS-AMI currently uses a single impulse response to model the channel, which is a good assumption for long serial channels with balanced drivers. With shorter channels, signal-ended signaling and rise/fall asymmetries we see in DDR5 applications, we'll have to see whether differences in rising and falling edges will be adequately described by adding impairments to the analysis such as jitter and adjusted eye masks or whether we need to characterize rising/falling responses separately. If we need to derive separate impulse responses for rising and falling edges, that will drive a lot of additional complexity into the IBIS-AMI specification and the analytical process.

Shaughnessy: So, AMI models were originally developed for serial channels. How do they compare to DDR5 topologies, and how does that matter from an equalization standpoint?

Katz: Serial channels tend to be long and lossy, while DDR channels tend to be short and reflective by comparison. The development of serial channel equalization techniques has mostly focused on overcoming loss. TX FIR and RX CTLE filters, the first two types of equalization used for serial channels, are designed to compensate for high frequency loss in the channel.

The problem with DDR5 topologies tends to be ringing—not loss. Serial channels are point to point, and discontinuities are stubs are sharply minimized to maximize signal quality. DDR5 topologies, by comparison, cannot afford to manage impedance and discontinuities as tightly—it's just not economically feasible. Because DDR5 topologies are multi-drop, multi-DIMM, stubs are long and reflections are huge by comparison. That's why we're so interested to see how the use of DFE plays out in DDR5, because DFE technologies are uniquely suited for dealing with significant reflections in the few bit times that precede the main signal.

Shaughnessy: How would users use AMI models to determine the best equalization settings for their systems?

Katz: There are two users, and they want to know two different things: The systems designer wants to know that for a given channel there is a best set of equalization settings that will optimize the DDR5 channel performance (smallest BER, largest time and voltage margins), and that the BER and timing and voltage margins meet the system performance requirements. They also want to know that whatever training algorithm the controller uses to optimize the channel at hardware runtime will end up with the settings needed to properly equalize the channel. So the systems designer wants to be able to predict the effect of the hardware training algorithm on system margin without necessarily modeling that training algorithm literally.

But the device vendor wants to design and validate the hardware training algorithm and prove that it will reach or at least come close to the best performance of the channel. They do want to model the training algorithm literally, or very nearly so.

Shaughnessy: It sounds like this whole thing has a lot of layers. Maybe we should talk again after DDR5 launches, to see how people are doing with this?

Katz: This is an incredibly detailed and interesting problem. What the actual hardware does and what the simulation models do will not be the same. Effectively managing the details of those differences will be critical to maximize the design's chance for success.

Shaughnessy: Thanks for your time, Walter.

Katz: Thank you, Andy. **PCBDESIGN**

Scientists Develop Shape-Shifting 'Superhero' Robot

Researchers have created a miniature 'superhero' robot capable of transforming itself with different 'outfits' to perform a variety of tasks.

Inspired by origami, scientists from the University of York and the Massachusetts Institute of Technology (MIT) have developed a magnet-controlled shape-shifting device which can walk, roll, sail on water or glide.

Dubbed "Primer," the cube-shaped robot carries out these actions by wearing different exoskeletons—accessories which start out as sheets of plastic that fold into specific shapes when heated. After Primer finishes its task, it can shed its "skin" by immersing itself in water, which dissolves the exoskeleton.

Professor Daniela Rus, Director of MIT CSAIL and Principal Investigator on the project, said: "If we want robots to help us do things, it's not very efficient to have a different one for each task. With this metamorphosis-inspired approach, we can extend the capabilities of a single robot by giving it different accessories to use in different situations."

While robots that can change their form or function have been developed at larger sizes, generally it's been difficult to build such structures at much smaller scales. What is also new about Primer is its ability to switch between many, rather than several, different forms.

Insulectro Teams with Isola to Address Signal Integrity Needs

by Andy Shaughnessy
I-CONNECT007

Insulectro and Isola recently shared a combined booth during PCB West 2017. Insulectro has distributed Isola materials for years, and the companies wanted to focus on Isola's line-up of high-speed, low-loss material sets. Insulectro's Chris Hunrath, VP of Technology, and Norm Berry, Director of Laminates and OEM Marketing, sat down with me to discuss the challenges facing signal integrity engineers today, and some of the Isola low-loss, low-Dk materials that can help with their signal integrity requirements. You might find Chris and Norm speaking to a group of PCB designers near you.

Andy Shaughnessy: I'm here at PCB West with Chris Hunrath and Norm Berry from Insulectro. Chris, why don't you start off by telling us a little bit about what you're finding in the field when it comes to signal integrity.

Chris Hunrath: One of the things that comes up with my customers a lot in the industry is signal performance. That boils down to a lot of different things, but signal loss and signal skew are two very important things. From a material standpoint, we have a lot of different offerings. What we try to do is help customers match the right product with their application. One of the things that was done many times to help mitigate skew, is to rotate the image on the panel, but that makes for very poor panel utilization or material utilization. Very popular right now are square glasses. Some of the square glasses have better performance than others for a lot of different reasons. A lot of that is design related, but there are ways to work around that as well.

Shaughnessy: Are you focusing more on this from a single integrity standpoint? I know you've had the recent release, you talked about that.

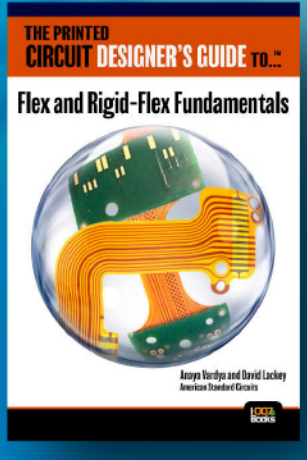
Norm Berry: As Chris mentioned, all the work has been done to mitigate differential pair skew, but there are so many other factors involved. Copper roughness certainly; we've been driving that down lower and lower and lower. Our primary offering now is a two-micron roughness, but it's going even farther south than that. Ev-

100% Commitment.

We have expanded the scope of our military qualification to include flex and rigid -flex circuits, having earned MIL-PRF-50884F and MIL-PRF-31032C certifications.

We are also approved for FR-4, polyimide, GF-homogeneous hydrocarbon/ceramic and GF-homogeneous hydrocarbon/ceramic mixed-base materials.

VIEW ALL OUR CERTIFICATIONS



A FREE BOOK FROM THE ASC EXPERTS

We are 100% committed to making flex and rigid-flex as easy as possible, so we wrote an eBook that you can download for free.

FREE EBOOK DOWNLOAD

American Standard Circuits

Creative Innovations In Flex, Digital & Microwave Circuits

Intertek

ITAR

www.asc-i.com

ery time it gets smoother, obviously, signal loss improves substantially and measurably, so we continue to drive that down. We also work with other suppliers who have offerings that help mitigate the roughness in the copper, which improves the loss and it mitigates skew. We've done a lot of research and we do present it. We presented this a number of times to IPC Designers Councils and have been invited to speak in front of many design groups to help provide that information in an effort to mitigate the problems they're going have with their designs once they become real time and real life.

Norm Berry

Shaughnessy: Like the saying goes, if you don't have signal integrity problems now, you will.

Berry: That's true. I saw that in print actually. Because of that, we've become an asset to many of our fabricators, where their sales and front-end engineering groups are working with designers, CMs, OEMs, and we've been invited many, many times this year to travel with them and present and support some of their offerings to designers who have this skew or loss issue.

Shaughnessy: Now we see all these boutique and hybrid materials coming out. I know materials like PTFE are hard for the fabricator to work with, but they have really low loss.

Hunrath: PTFE has been a good material for signal integrity, but mechanically it's not very good. It comes with a lot of baggage. As Norm mentioned, the trend to go to smoother coppers has its trade-offs too, because the adhesion is not the same. Our customers need to understand that. If there's a work-around or a way of making a mixed-material package to get what they need, but still also have the board manufacturable and have it built for assembly without any problems, you need to put all that together.

Chris Hunrath

Shaughnessy: So, where do you think are some of the big opportunities in the future for Insulectro?

Hunrath: Well, certainly the higher-performing materials from Isola and DuPont are a growing part of our business. We've been working hard to make sure our customers have access to a quick access. We do a lot of same-day deliveries for those materials, but that's a growing part of our business. We're putting a lot more variety in our inventory, so we can get these materials out there.

Shaughnessy: Designers and signal integrity engineers sometimes complain that materials companies release these new materials without fully testing and characterizing them. But still, it can take companies 18 months to get one material set ready and out the door.

Berry: Well, when you consider the requirements of a laminate set, first of all, it has to be thermally robust. It has to be able to be assembled in a lead-free environment. In addition to that, it has to be manufacturable. The board shop has got to be able to laminate it, drill it, clean the holes out, and do it cost-effectively. It all boils down to the cost of ownership, so that you have something that is manufacturable, that the board shop can use. One of the points you called out was hybrid construction. On some of these more expensive low-Dk, low-Df products, they're very expensive, so wherever possible people are putting in lower cost FR4 for the power planes, so that they can reduce the cost. Now you have a hybrid. You've got to make sure that those are all compatible with each other. Isola has spent an extraordinary amount of time working to make sure that

their resin systems are going to be compatible with each other. They lend themselves, actually, to that hybrid construction.

Shaughnessy: And with hybrids, you don't want to have a lot of different warp and twist rates…

Berry: The vast majority of the Isola's high-performance and high-speed digital products have very similar press cycles, which lend themselves to the hybrid package construction.

Hunrath: If the materials are very different, you'll end up with a potato chip at the end of the process, which is impossible to run through assembly, so it's important that the materials do work well together.

Berry: At that elevated temperature, CTE mismatch is going to give in-plane shear stress, for instance.

Hunrath: One of the other things we're seeing with the square glass materials is that it's not just about signal integrity. There is a trend to use those materials on standard resin systems where signal loss or skew is not so important, but the people want to get higher reliability, single-ply constructions, or they want to have better, quicker laser drilling. The square glass eliminates some of the glass bundle knuckles and makes it easier to laser drill, faster to laser drill. Productivity and reliability in single-ply construction are also driving more square glass constructions.

Shaughnessy: Is there anything else you would like to add?

Berry: We're dedicated to working with our fabricator customers to get out and educate their customer base, so that they make the right choices, close in on their revenue goals, and that we're all successful together.

Shaughnessy: I appreciate your time.

Hunrath: Thank you, Andy. **PCBDESIGN**

A Zero-Index Waveguide

In 2015, researchers at the Harvard John A. Paulson School of Engineering and Applied Sciences (SEAS) developed the first on-chip metamaterial with a refractive index of zero, meaning that the phase of light could be stretched infinitely long.

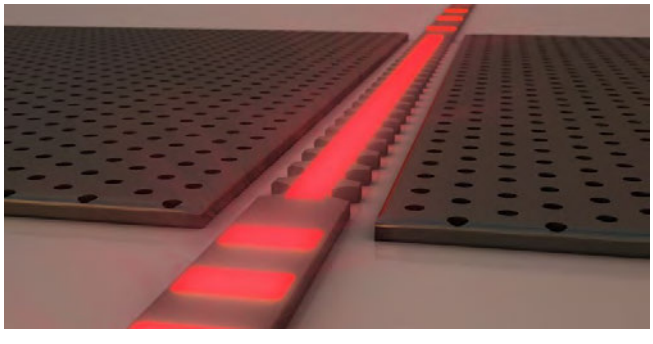
Now, SEAS researchers have pushed that technology further, developing a zero-index waveguide compatible with current silicon photonic technologies. In doing so, the team observed a physical phenomenon that is usually unobservable—a standing wave of light.

When a wavelength of light moves through a material, its crests and troughs get condensed or stretched, depending on the properties of the material. How much the crests of a light wave are condensed is expressed as a ratio called the refractive index: the higher the index, the more squished the wavelength.

When the refractive index is reduced to zero the light no longer behaves as a moving wave, traveling through space in a series of crests and troughs, otherwise known as phases. Instead, the wave is stretched infinitely long, creating a constant phase. The phase oscillates only as a variable of time, not space.

Imagine strings on a guitar, pinned on either side. When a string is plucked, the wave travels through the string, hits the pin on the other side and gets reflected back, creating two waves moving in opposite directions with the same frequency. This kind of interference is called a standing wave.

This may be the first time a standing wave with infinitely-long wavelengths has ever been seen.



The Impact of Final Plated Finishes on RF PCB Performance

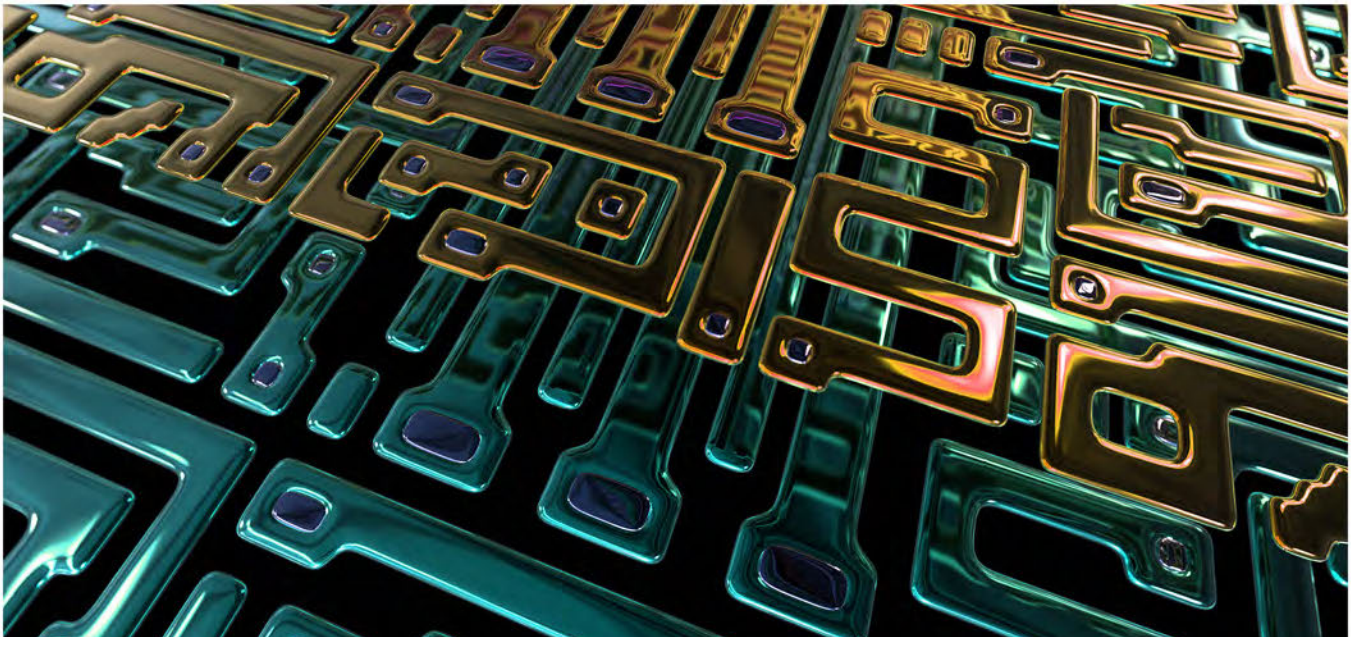
by John Coonrod
ROGERS CORPORATION

Final plated finishes are used on PCBs for many different reasons. These include protecting the copper from tarnishing, improving long-term reliability, and enhancing assembly efficiency. Whatever the reason, the final plated finish can have an impact on a PCB's RF performance. Most notably, insertion loss is often increased due to the final plated finish. For some PCB configurations, the plated finish affects insertion loss substantially and other configurations are less affected. The final finish can have more or less impact on insertion loss due to several potential variations of the PCB construction and/or the design of the circuit.

Most final plated finishes have lower electrical conductivity than copper, with one exception being silver. A common finish is electroless nickel immersion gold (ENIG), which can cause increased insertion loss because nickel has approximately ¼ the conductivity of copper. Aside from the conductivity issue, nickel is also ferromagnetic and has the potential to increase losses due to magnetic field interactions.

Using a simple two copper-layer microstrip circuit as an example, most of the electric fields and higher current density areas are between the signal plane and the ground plane. Due to that configuration, many people may assume that adding metal to the copper will not impact the electrical performance because the interface between the signal and ground plane is unaffected by the added metal. However, if simple electromagnetic modeling is performed on a microstrip transmission line circuit, it will be seen that there is high current density at the edges of the signal conductor and that is also where more electric fringing fields reside. It is at these corners of the signal conductor and where it meets the substrate surface that the composite conductivity of the copper and the final plated finishes can cause differences in the conductor loss of the circuit.

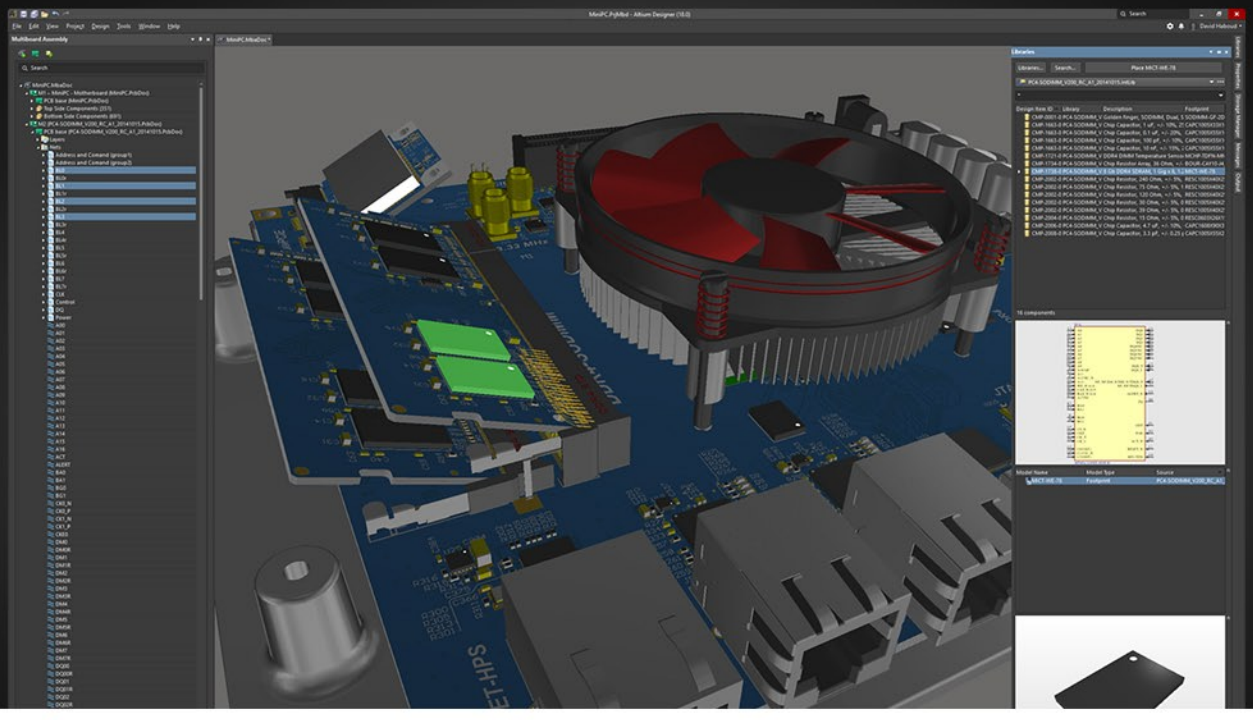
Conductor loss is a component of insertion loss (the total RF loss of the circuit) and an increase in conductor loss will cause the insertion loss to increase. When the circuit is short in



ALTIUM
DESIGNER 18

The Easy, Powerful, Modern PCB Design Solution

COMING SOON



For more information please visit:

www.altium.com/altium-designer/coming-soon

Altium

physical length, the additional loss due to the final plated finish effect at the corners of the conductor can be minimal. However, this corner effect is accumulative and the same circuit design with increased length will have much more insertion loss due to the final finish.

Another consideration is the thickness of the circuit and again a reference will be given to the simple microstrip circuit as example. A thinner circuit is more dominated by conductor loss than a thicker circuit. The final plated finish is affecting the conductor loss of the circuit, and for a thick circuit where conductor losses are minimal, a change to conductor loss due to the final plated finish will be less significant. However, a thinner circuit which is much more sensitive to differences in conductor effects, will certainly be more impacted by the effect of final plated finish on insertion loss.

> "A thinner circuit is more dominated by conductor loss than a thicker circuit."

There are also circuit design related issues. A stripline circuit, where most of the fields are contained within the body of a multilayer PCB are not significantly impacted by the final plated finish which is applied to the outer layers of the PCB. A microstrip circuit will have insertion loss affected by the final plated finish as previously discussed, however, a grounded coplanar waveguide (GCPW) will typically have more insertion loss due to the plated finish. The GCPW has coupled fields between the ground-signal-ground configuration, which is on the top copper layer or signal layer of the circuit. These coupled fields are basically using four layers of the final plated finish, which is between the side walls of these coupled conductors. Additionally, if the GCPW is tightly coupled (with a small space between ground-signal-ground), the increased loss due to the final plated finish will be more than if it were a loosely coupled GCPW circuit.

There is also a frequency dependency for the effects of final plated finish on insertion loss, due mostly to skin depth. The skin depth of an RF circuit is the amount of the conductor being used by the RF current. At higher frequencies, the current will use less of the cross-sectional area of the conductor and at very high frequencies only the "skin" of the conductor is used by the current. As a basic example, using the microstrip circuit again, at low frequencies, the composite conductivity at the corners of the signal conductor is made up of the conductivities of copper, nickel and gold for a circuit using ENIG plated finish. As the frequency increases, the skin depth will decrease and at some point, only the nickel and gold will be used by the RF current. At this point, the composite conductivity has become worse because the good conductivity of copper is no longer being used by the RF current. When the frequency increases even more, the skin depth is causing the RF current to mostly use the layer of gold, which is a pretty good conductor. However, at these very high frequencies, there are other circuit-RF properties which change and cause more loss not related to the final plated finish.

The difference of insertion loss due to final plated finishes is dependent on the circuit thickness, the design and frequency. Basically, a thinner circuit is more sensitive to differences related to conductor effects and a change in insertion loss will be more significant with a thin circuit as compared to a thick circuit of the same design. Additionally, GCPW will have more insertion loss change due to final plated finish than a microstrip circuit. And finally, as the frequency increases, the losses related to the finish can become more significant as the skin depth becomes thinner and uses less of the conductor. **PCBDESIGN**

John Coonrod is the technical marketing manager at Rogers Corporation. To contact Coonrod or read past columns, click here.

ME AND GERBER THE LIZARD 1986

We love PCBs.
We always have.

We are the geeks. The nerds. The passionate. We all think, talk and dream about that little green masterpiece. We call it **Your Key Component**. Because that's what it is. And our mission is to **produce PCBs for demanding customers, on time, with zero defects, and at the lowest total cost.**

We are the NCAB Group. One of the world's leading producers of PCBs. We have been producing PCBs, and only PCBs since 1993.

Today our U.S. locations are in:
California Florida Illinois New Hampshire Texas Washington

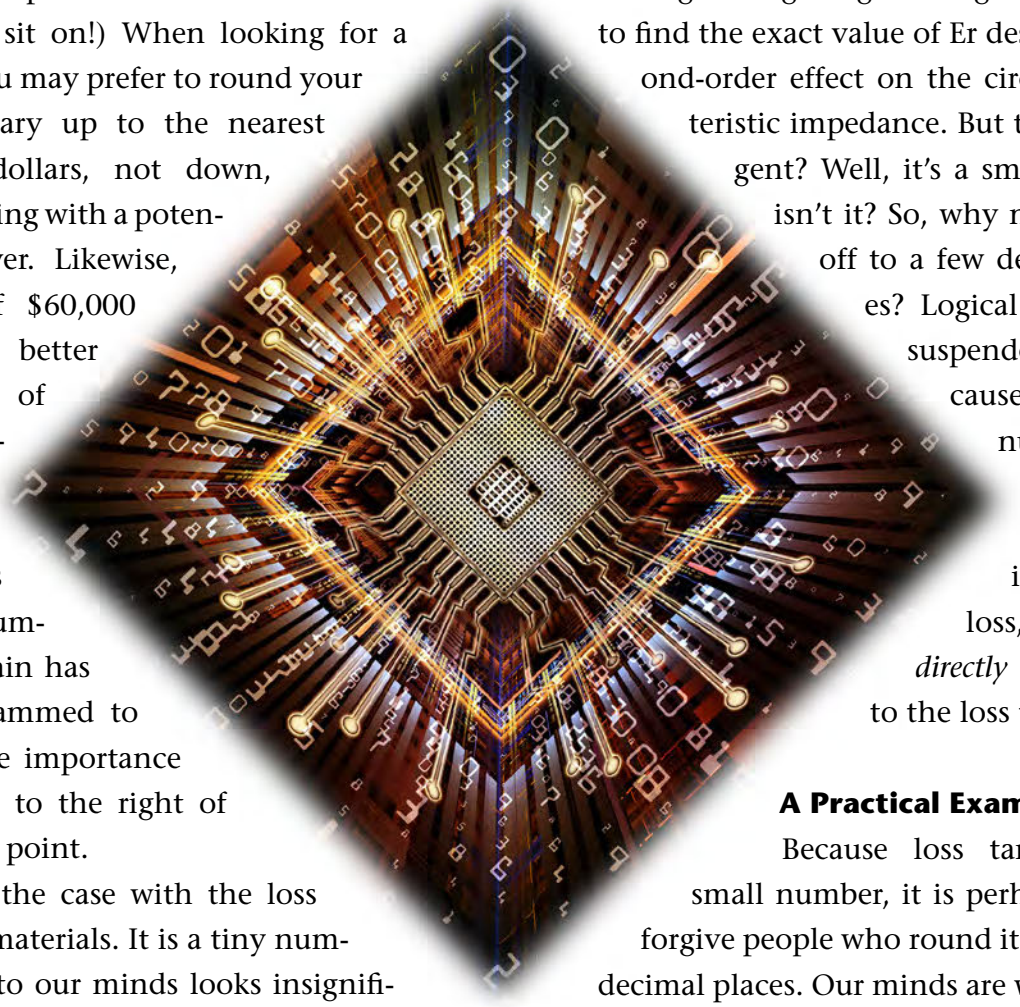
www.ncabgroup.com

NCAB GROUP
Integrated PCB Production

Tangential Thoughts: Loss Tangent Values

by Martyn Gaudion
POLAR INSTRUMENTS

Numbers are fascinating things and the way they are presented can influence our thinking far more than we would like to admit, with $15.99 seeming like a much better deal than $16.00 (though it depends which side of the transaction you sit on!) When looking for a new job, you may prefer to round your existing salary up to the nearest thousand dollars, not down, when speaking with a potential employer. Likewise, a salary of $60,000 sounds better than one of $0.061 million, even though the latter is a larger number. Our brain has been programmed to suppress the importance of numbers to the right of the decimal point.



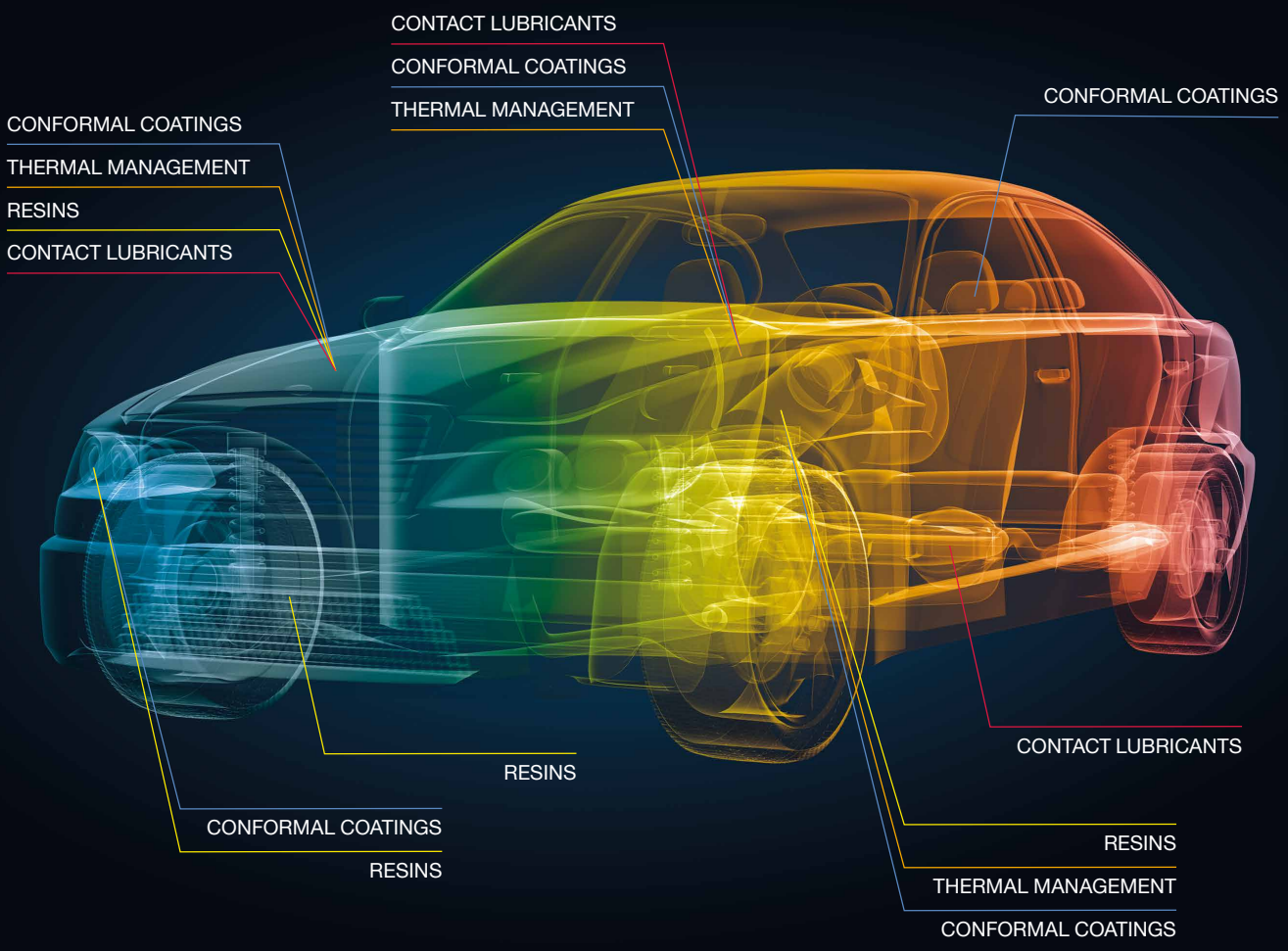
Such is the case with the loss tangent of materials. It is a tiny number and so to our minds looks insignificant, but it has a directly proportional effect on the energy loss suffered by a dielectric. I am always curious that engineers seem to obsess over dielectric constant [1], the ability of a substrate to store energy and its effect on impedance, which is a one over root effect i.e., – so this is a *second order* impact on Z_0.

Yet engineers go to great lengths to attempt to find the exact value of Er despite its second-order effect on the circuit characteristic impedance. But the loss tangent? Well, it's a small number, isn't it? So, why not round it off to a few decimal places? Logical thought is suspended just because it is a small number, but when you are modeling insertion loss, the loss is *directly proportional* to the loss tangent [2].

A Practical Example

Because loss tangent is a small number, it is perhaps easy to forgive people who round it off to fewer decimal places. Our minds are wired to dismiss numbers far to the right of the decimal point. However, this can lead to unintended miscalculations when rounding small value

TOGETHER WE MAKE THE WORLD'S MOST INNOVATIVE ENGINEERING SOLUTIONS GO COMPLETELY UNNOTICED



Our innovative electro-chemical solutions serve a full spectrum of industries, from automotive and aerospace to electronics, health, the military, utilities, and more.

Working with some of the world's best known brands our specialists collaborate on research, development and manufacturing to implement solutions that meet and exceed industry and company standards, solving issues, affecting change, improving tolerances and increasing performance.

Combine our unique ability to offer the complete solution with our global presence and you have a more reliable supply chain and a security of scale that ensures you receive an always exemplary service.

Isn't it time you discovered how Electrolube can serve you?
Simply call, or visit our website to learn more.

productronica
innovation all along the line
November 14-17, 2017
Messe München
Hall A4, Stand 466

888-501-9203
www.electrolube.com

ELECTROLUBE
THE SOLUTIONS PEOPLE

Electronic & General Purpose Cleaning	Conformal Coatings	Encapsulation Resins	Thermal Management Solutions	Contact Lubricants	Maintenance & Service Aids

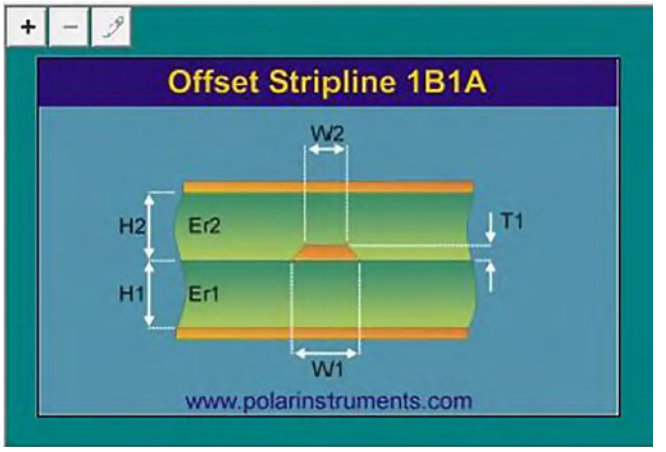


Figure 1: A field solver modeling loss in an offset stripline 1B1A controlled impedance structure.

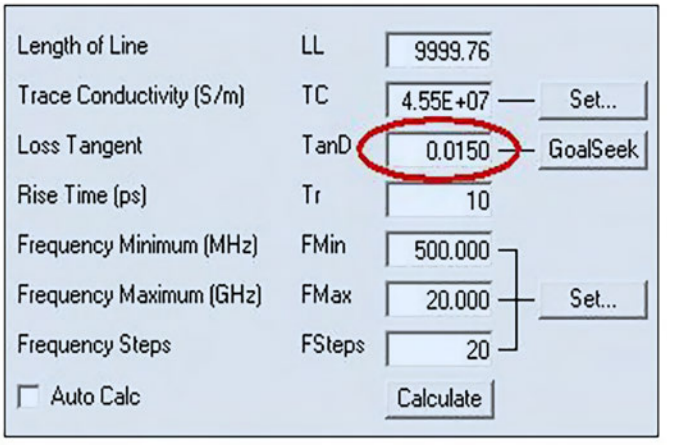


Figure 2: Next, specify a frequency range of 500MHz – 20GHz and a value of 0.015 for loss tangent (TanD).

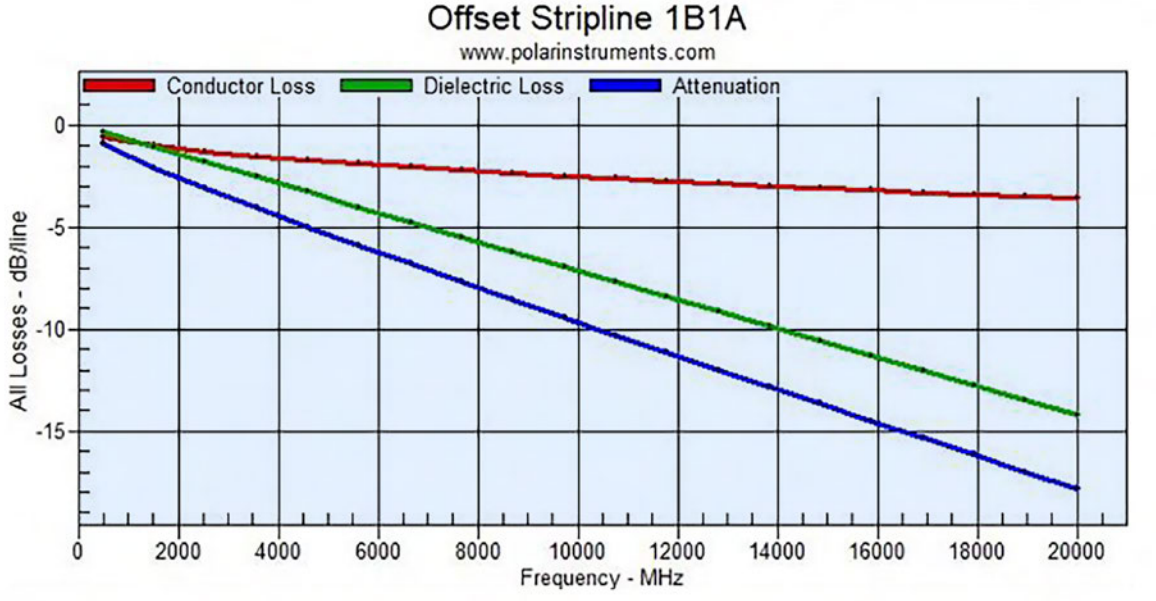


Figure 3: Finally, calculate and display the losses against frequency, in this case, a loss value of -14 dB.

parameters such as loss tangent which has a directly proportional effect on the insertion loss. A rounding to 2 decimal places of a TanD say, from 0.015 to 0.02 (quite legitimate, you may think) would actually lead to the modeling of insertion loss being overpredicted by a massive 33%.

You can see the effect when using a PCB field solver's frequency-dependent calculation feature to model loss in an offset stripline 1B1A controlled impedance structure (Figures 1-3).

Rounding the Value of Loss Tangent

How will the dielectric loss value change if the value of the loss tangent is rounded from 0.015 to 0.02? First, change the value of the loss tangent to 0.02 (Figure 4).

Note that rounding from 0.015 to 0.02 actually represents an increase in loss tangent value of 33%. This increase in turn results in a corresponding increase (Figure 6) in dielectric loss of 33%.

It might have been easier to visualize the real difference in loss tangent (and avoid unex-

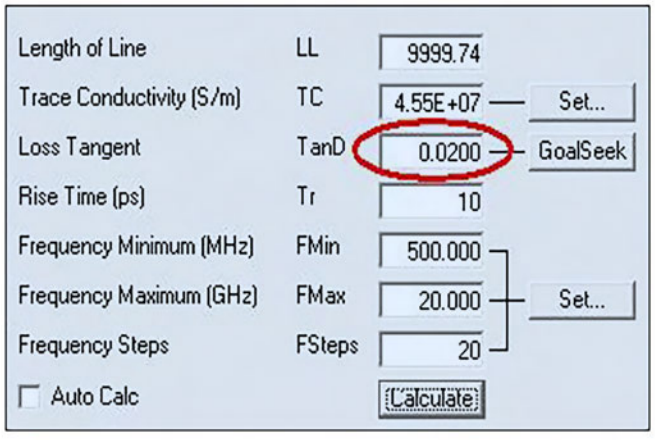


Figure 4: Change the loss tangent value to 0.02.

pected errors) if the values had been expressed in engineering notation. The actual value of loss tangent, 0.015, is expressed in engineering notation as 15 x 10^{-3}, but the rounded value, 0.02, is expressed as 20 x 10^{-3}, an obvious increase of 33%.

So perhaps a better way of displaying loss tangent would be in scientific notation instead of 0.015. You could say TanD = 15x10^{-3} or 15 milli TanD. But for some reason that I am unaware of, it seems that only tangible units (i.e., weight, mass, wavelength and frequency) are referred to in this way. Quantities that are ratios tend to be shown in fractional or decimal format.

Loss tangent is one of those "mystery" characteristics that isn't easy for fabricators to visualise or measure. The simplest way of thinking of loss tangent is to look at it as the ability (albeit undesired) to turn precious RF energy into heat. This is excellent if you are designing microwave ovens, but not so helpful if you are attempting to transmit small-amplitude high-speed signals from point A to point B along a PCB transmission line.

Because it is a tricky animal to measure, it comes as no surprise that there are a variety of measurement methods, and some more appropriate to some applications than others. Split post resonator methods, for example, are ideal for bulk measurement of loss tangent when manufacturing base materials. When choosing a value of loss tangent for use in signal integrity applications you will get best results if you use a value derived by using transmission line techniques. The loss tangent in a data sheet may have been measured in a variety of ways depending on application and frequency of measurement—most data sheets note this—but if in doubt, ask.

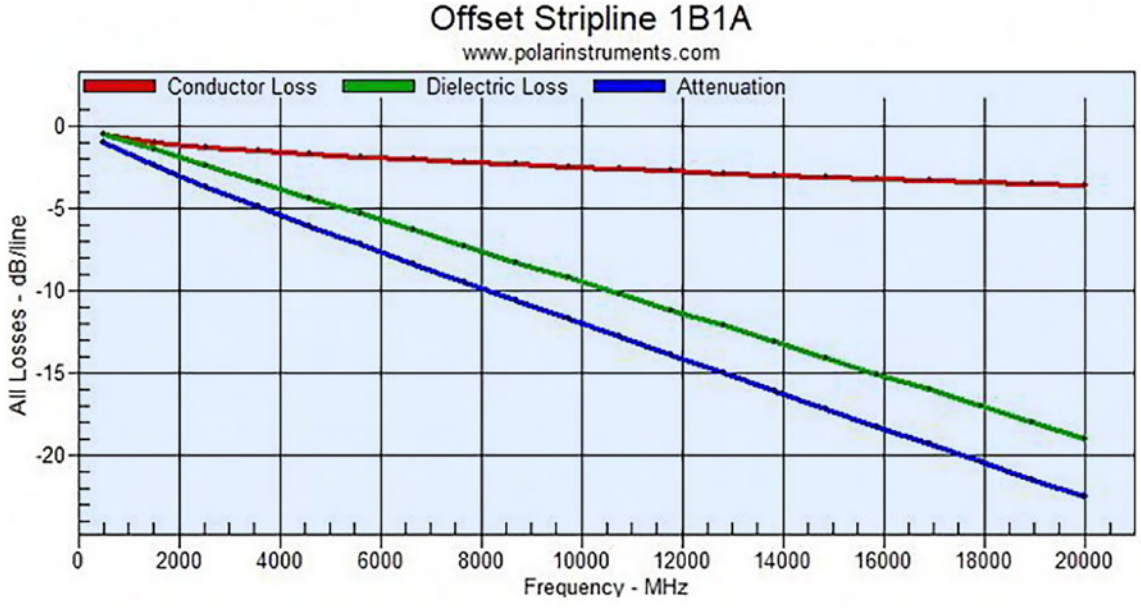


Figure 5: Recalculate and note the new loss value of -19 dB at the 20GHz data point on the dielectric loss series.

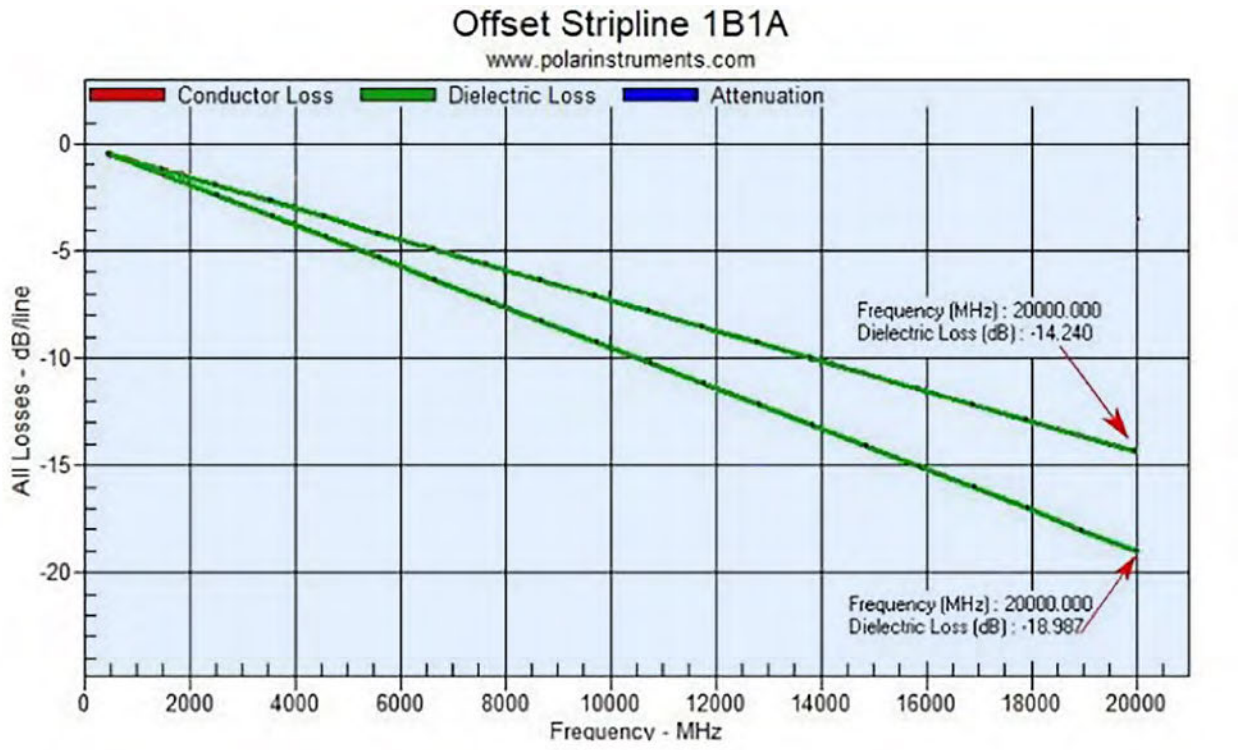


Figure 6: An increase in loss tangent value of 33% in turn results in a corresponding increase in dielectric loss of 33%.

Taking this one step further, if your data sheet uses one TanD measurement method at 100MHz, and another at 1GHz and a third at 10GHz, which should you use when modeling high-speed designs? Should you: a) guess; b) select the highest; c) select the one closest to your clock frequency; or d) use all three?

Note that in the previous paragraph I explained that some measurement methods are less appropriate than others for transmission line modelling, so if there is a measurement using a transmission line, then that is the best approach.

I can hear you asking, "But what if it is not at my clock frequency?" Fortunately, there are some mathematical techniques that can help you out here. Svensson-Djordjevic modeling uses mathematical models of the substrate to predict the value of both TanD and Er over frequency when given a single known frequency input (see Figure 7).

Using this type of modelling in your field solver to predict Er and TanD from a known spot frequency and measured with an appropriate model for use in a transmission line application is the optimum solution when faced with a variety of TanD values, methods and frequencies.

Back to the original message: The point I make here is that, whether you are concerned about insertion loss or any other quantity that is presented as a small ratio, it is vital that you use the number expressed with enough significant digits to yield an appropriately accurate calculation and a value obtained from a method appropriate to your application. **PCBDESIGN**

References

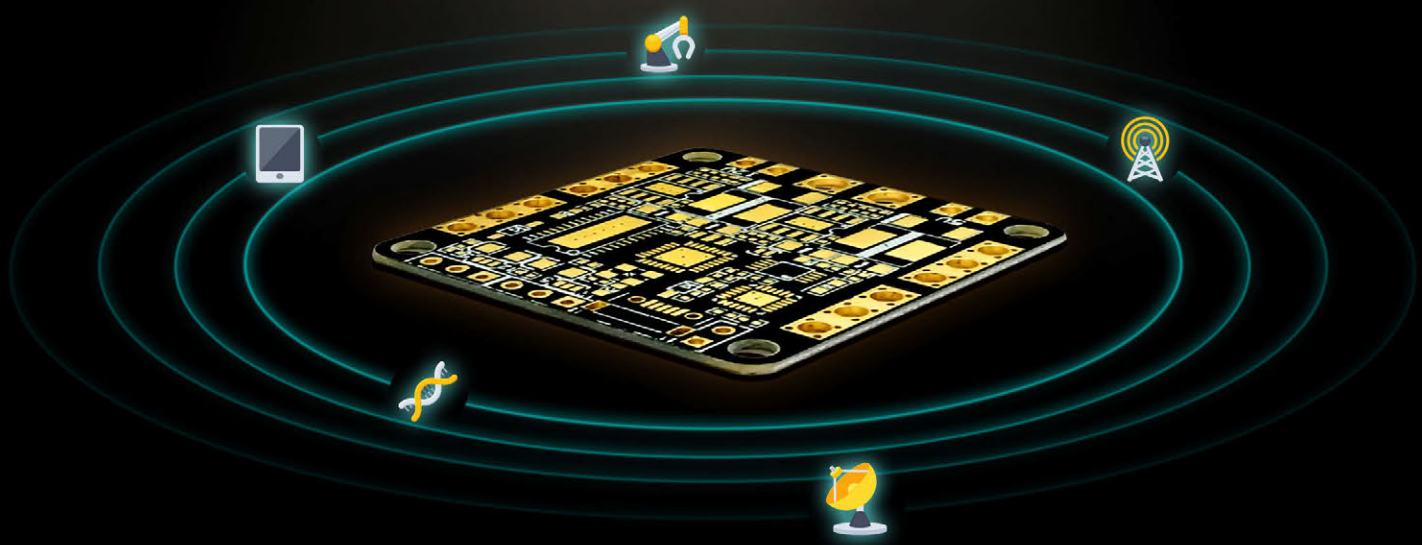
1. Dielectric constant: Think of this in layman's terms as simply a measure of how well a substrate can store electrical charge, often referred to with a variety of symbols as ε_r, Er, Dk, K.

2. Loss tangent: Think of this in layman's terms as simply the undesirable ability of a substrate to turn useful signal energy into heat (un-

Professional PCB Fabrication Service

for Telecommunication, Automation & Test and Measurement Applications

PCBCart has been serving worldwide companies of all sizes with quickturn PCB prototype and mass production services for over 10 years. Each year, we fabricate 23,000+ different PCB designs and we are committed to quality and performance on every circuit board we make.



Our Advantages:

- Easiest online quoting & ordering system
- Best overall PCB quality, customer services & competitive pricing
- Flexible PCB Assembly and Components Sourcing services available
- Advanced techniques including Gold fingers, Blind/Buried hole, Via in pad, etc.
- From FR4 PCBs to Aluminum PCBs, Flex PCBs, Flex-rigid PCBs, Rogers PCBs, etc.
- Free DFM Checking and other custom Electrical Tests (flying probe test, etc.)

ISO 9001 SGCC · LEAD FREE · UL

PCBCART

www.pcbcart.com

sales@pcbcart.com

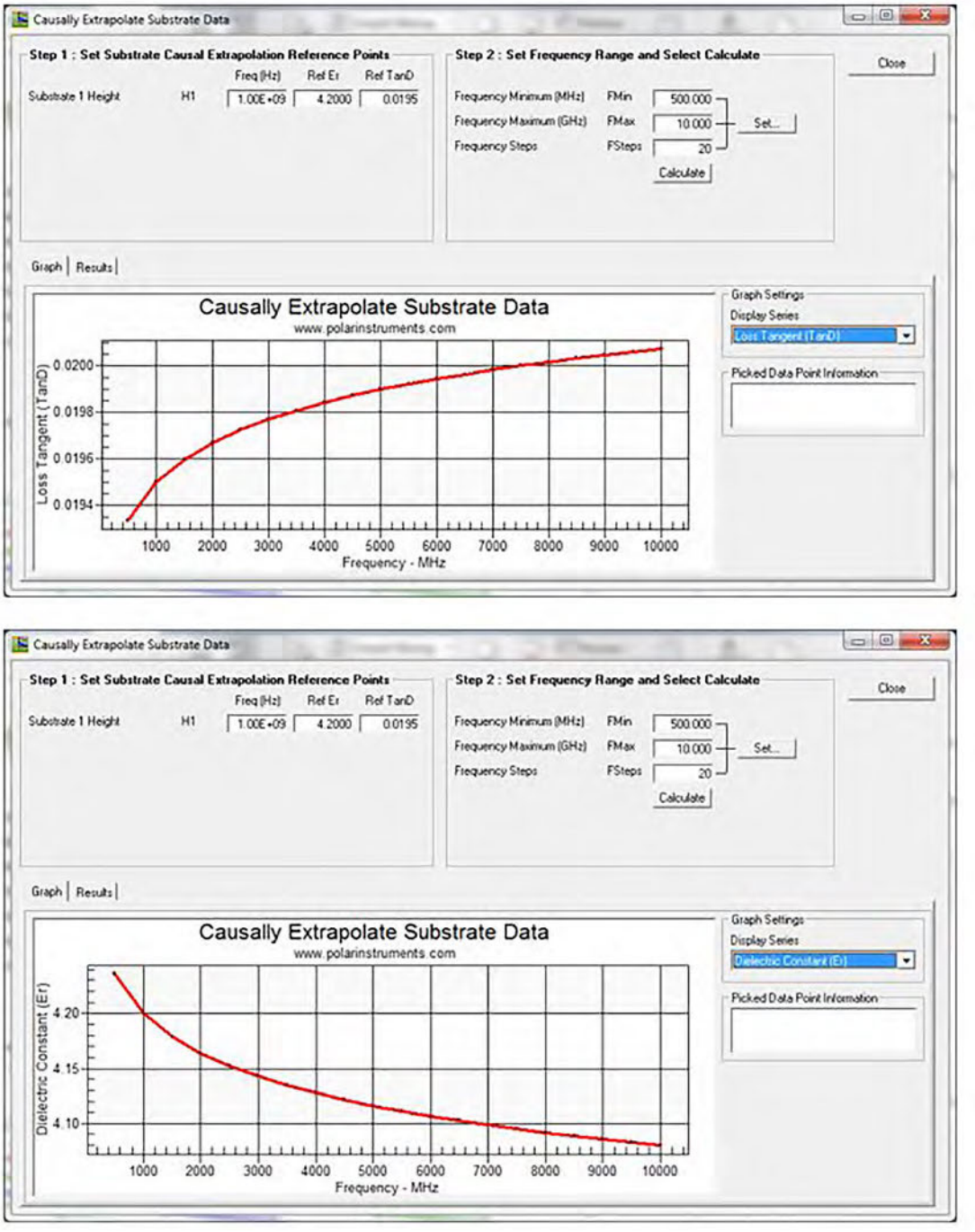


Figure 7a and 7b: Example of Svensson-Djordjevic modelling, which uses mathematical models of the substrate to predict the value of TanD and Er over frequency when given a single known frequency input.

less, that is, you are making a microwave oven.) Loss tangent is also referred to with a variety of terms: tanδ, Tan D, Df. From an SI perspective, the lower the better, but you must factor in the cost.

Martyn Gaudion is managing director of Polar Instruments. To read his past columns or contact him, click here.

2017 Programs

October 3–4
IPC & WHMA Wire Harness Manufacturing Conference
Conference
Paris, France

October 3–4
IPC Technical Education
Workshop
Paris, France

October 6
Manufacturing Day
National Event
Across the United States

October 10
IMPACT Europe
Meeting
Brussels, Belgium

October 11
Wisdom Wednesday
IPC-2581 and the Perfect BOM
IPC Members Only
Webinar

October 16
IPC Day
Networking Event
Minneapolis, MN

October 17–18
IPC Flexible Circuits-HDI Forum Tutorials and Technical Conference
Conference
Minneapolis, MN, USA

November 7
IPC Day
Networking Event
Raleigh, NC

November 7
IPC Technical Education
held in conjunction with PCB Carolina
Workshop
Raleigh, NC, USA

November 7–9
The Pb-Free Electronics Risk Management (PERM) Council Meeting No. 34
Philips Innovation
Meeting
Andover, MA

November 8
Wisdom Wednesday
Competitive Innovation: Best Practices
IPC Members Only
Webinar

November 14–17
IPC Committee Meetings
held in conjunction with productronica
Meeting
Munich, Germany

November 14–17
IPC Hand Soldering Championship
held in conjunction with productronica
Competition
Munich, Germany

December 6–8
HKPCA International Printed Circuit and Exhibition & APEX South China Fair
Conference
Shenzhen, China

December 13
Wisdom Wednesday
Strategies for Reducing Product Warranty and Liability Risk in Manufacturing Services Agreements
IPC Members Only
Webinar

For more information, **visit www.IPC.org/events**

MilAero007 Highlights

All About Flex: Flexible Circuits and Man-Made Satellites

The first satellite was launched by the USSR in 1957. The U.S. successfully launched its first satellite, Explorer 1, in 1958 while announcing the intention to "win" the race to outer space. Today satellites serve many vital purposes.

Let's Talk Testing: Professor Plum in the Library with the Candlestick...Right?

Who knew that a phrase from a decades-old popular board game could have some relevance in today's ever-changing world? In the game of Clue, simply put, evidence is collected and then used to solve a mystery. In my world, testing is performed to gather data/results (evidence) and then this information is used to determine the root cause of some issue that is under investigation (solving the mystery).

Saab and Adani to Collaborate on Aerospace and Defense Projects in India

Defense and security company Saab and Indian infrastructure conglomerate Adani Group announced a collaboration plan within aerospace and defense in India, aligned with the Government of India's Make in India initiative.

AT&S Enables "Cool" Designs for Miniaturized High-Power Applications

Miniaturization and increasing power densities are major concerns for modern electronic applications. The lifetime of electronic applications can be dramatically reduced by the increase of the working temperatures by just a few degrees.

The International Paris Air Show with ASC's Anaya Vardya

The International Paris Air show is the crème de la crème of the world's trade shows. This is the big one, where all the aircraft, airline and defense aerospace companies meet to introduce new products, discuss the future of aviation, and make deals. This year I decided to talk to my friend Anaya Vardya, ASC's president and CEO, about the show, why he goes, and what it's like.

Thin, Flexible Device Could Provide Efficient Cooling for Mobile Electronics—or People

Engineers and scientists from UCLA, and SRI International, a nonprofit research and development organization, have created a thin flexible device that could keep smartphones and laptop computers cool and prevent overheating.

New Cadence Allegro DesignTrue DFM Technology Accelerates New Product Development and Introduction Process

Cadence Design Systems, Inc. announced Cadence Allegro DesignTrue DFM technology, the industry's first solution to perform real-time, in-design DFM checks integrated with electrical, physical and spacing design rule checks.

DARPA Rolls out Electronics Resurgence Initiative

Transformative advances in electronics will come from a combination of six new programs, a portfolio of existing ones, and the country's largest funding program for basic university research in electronics.

Tracking Debris in Earth's Orbit with Centimeter Precision using Efficient Laser Technology

A research team at the Fraunhofer Institute for Applied Optics and Precision Engineering IOF in Jena, Germany, has now especially developed a fiber laser that reliably determines the position and direction of the space debris' movement to mitigate associated risks.

Increase in Aircraft Orders and Real-Time Data Need Drive Growth in Avionics Market

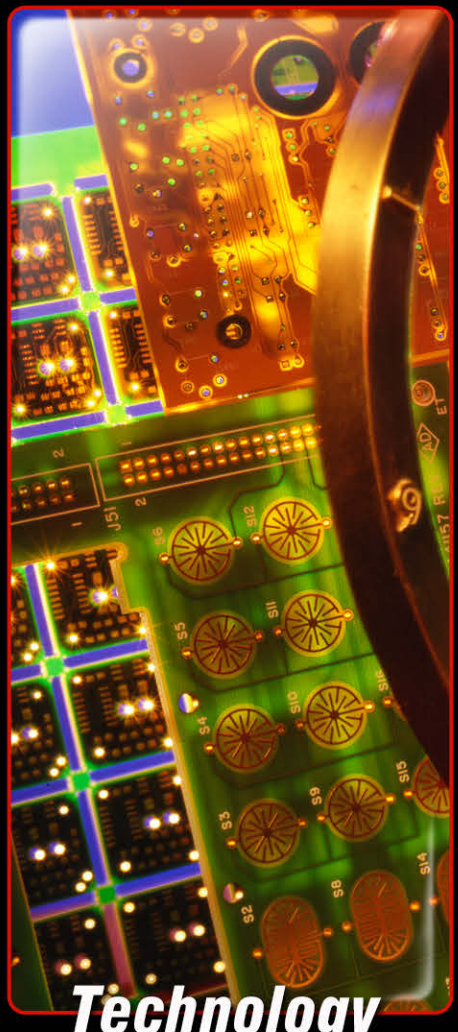
With NextGen and SESAR set for completion this decade, the global commercial avionics market is undergoing a transition from a ground-based system to a satellite-based air traffic control system and is headed towards more compute-intensive, high-speed, and high-bandwidth avionics.

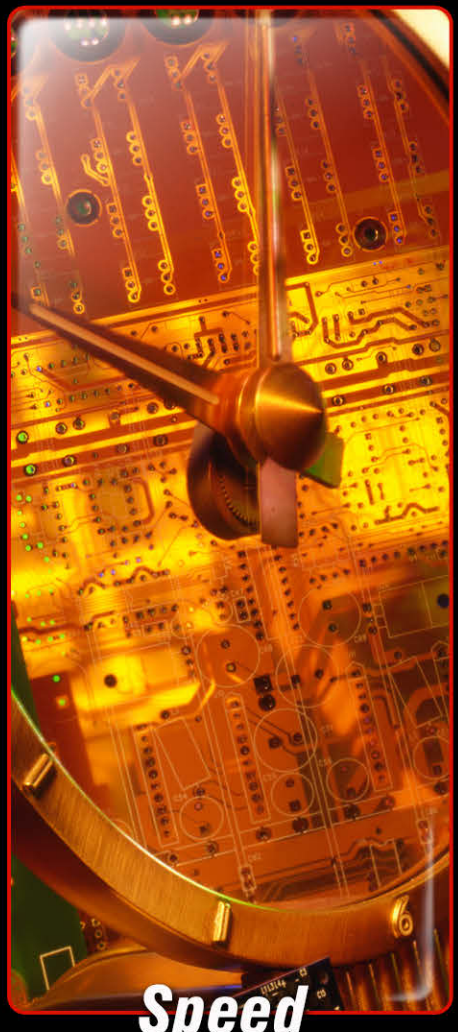
prototron.com

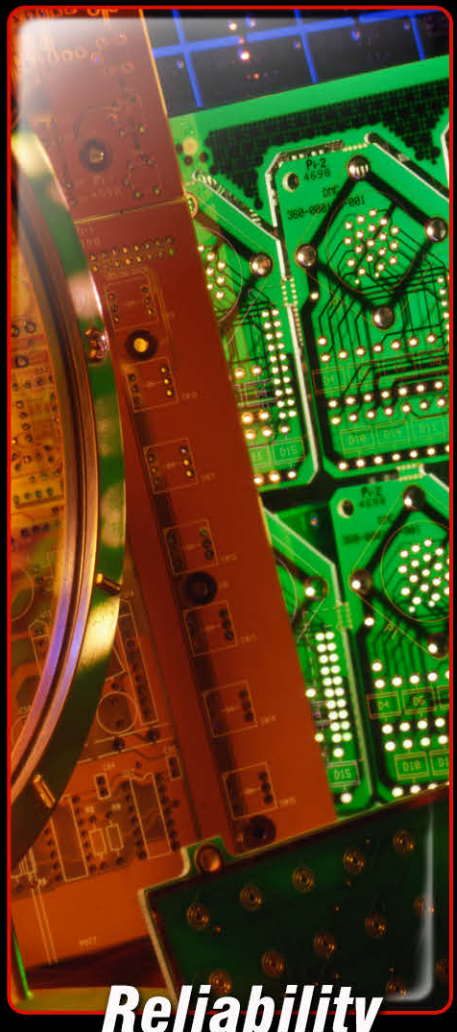
We're Hiring!

We Take the Time to do it Right

because you don't have the time to do it over.







Prototron Circuits

High quality quick turn manufacturing, just another reason we are

America's Board Shop

Prototron is Hiring! We are currently seeking candidates to fill positions for both a midwest sales professional and an experienced PCB process engineer. To apply, contact us at 425-823-7000 or email Russ Adams at russa@prototron.com for sales or Kirk Willams at kirkw@prototron.com for engineering.

Thermal Management for LED Lighting Manufacturers

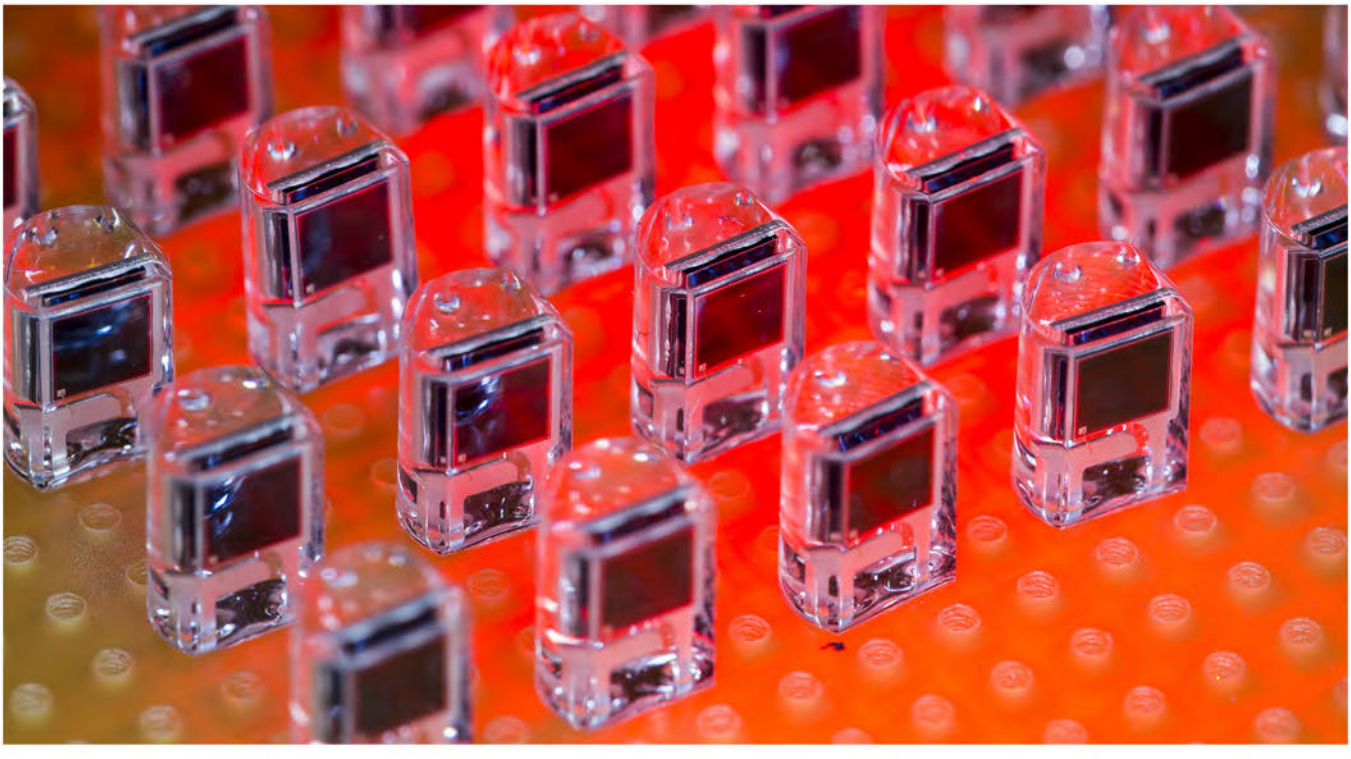
by Jade Bridges
ELECTROLUBE

Moving on from my overview of common thermal 'problems and solutions' published in last month's column, I'd like to focus more closely this month on a specific application area for thermal management solutions—and it's a 'hot' one, too: LED luminaires and their associated electronics. The LED lighting industry is a global growth phenomenon and the sector's demand for effective, high-quality electrochemicals is enormous.

While LEDs have been present in many electronic devices for a number of years, more recent developments have led to their use in all types of domestic, commercial and automotive lighting, signage and domestic appliance products. In offering alternatives to halogen, incandescent and fluorescent lighting systems for both interior and exterior applications, the growth of the LED lighting market alone is expected to grow into a $70 billion industry by 2020; this represents a growth from 18% market share to 70% market share in just over five years.

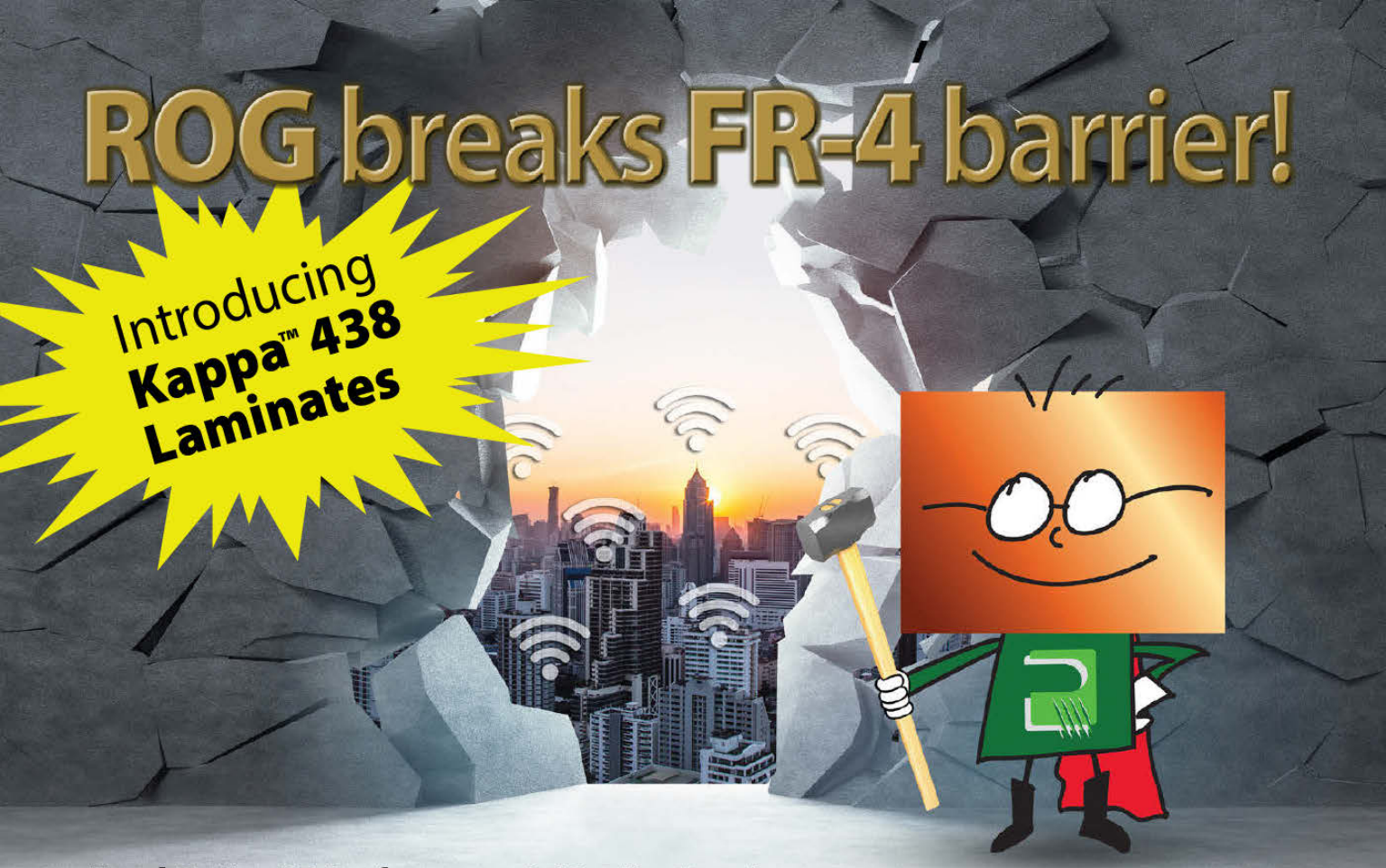
We are currently serving the LED industry in every aspect of product design and product protection, including areas such as potting, encapsulation, and conformal coating. For the purposes of this article, however, I'm going to concentrate on the thermal management of LED assemblies, and how materials selection and application can influence the life expectancy and long-term performance of LED lighting systems.

As in my first column on this subject, I'm going to return to my original FAQ format, based on the many queries that our customer support teams field every day on the telephone, at exhibitions and when visiting customers' premises. I've selected five common enquiries about LEDs followed by their respective responses.



ROG breaks FR-4 barrier!

Introducing **Kappa™ 438 Laminates**



Need Better RF Performance? FR-4 No More!

Demand for wireless data is growing exponentially, driving a need for substantially higher levels of mobile network capacity and performance. This demand will grow further in support of the upcoming 5G IoT ecosystem where billions of devices will be communicating with each other, and connectivity is immediate and uninterrupted. FR-4 was historically a material choice for many less demanding RF applications, but changes in the wireless infrastructure related to growing performance requirements, especially in small cells and carrier-grade WiFi/Licensed Assisted Access (LAA), have resulted in instances where the properties of FR-4 are lacking, and RF performance and consistency is compromised. There's no longer a need to sacrifice your PCB performance.

— Now There's Kappa™ 438 Laminates.

Wireless circuit designers can enjoy a true breakthrough with Kappa 438 laminates because they feature the performance of "mid-tier" circuit materials and they shatter the performance limits of FR-4, but at affordable prices. Kappa 438 laminates have low loss, excellent Dk tolerance, and tight thickness control and are engineered for outstanding, repeatable wireless performance.

PROPERTY	TYPICAL VALUE
Dk*	4.38
Df	0.005

*Design Dk; Differential Phase Length Method at 2.5 GHz

By having similar Dk to FR-4, your design transition to Kappa 438 laminates will be effortless! Visit **www.rogerscorp.com/kappa** to learn more.

productronica Hall B3, Booth 401

ROGERS CORPORATION

Advanced Connectivity Solutions

USA - AZ, tel. +1 480-961-1382 • EUROPE - BELGIUM, tel. +32 9 235 3611

www.rogerscorp.com/kappa

Does excess heat have an adverse effect on the LED and if so, how can thermal management materials mitigate this?

Heat adversely affects an LED by reducing both its efficiency and its life expectancy. By reducing the junction temperature by just a few degrees, the lifetime of an LED can be increased by thousands of hours. Moreover, a reduction in the temperature of the LED's surrounding environment will also impact on the junction temperature and, again, the useful life of the LED.

Thermal management materials are designed to dissipate heat away from critical areas. In LED arrays, they can help distribute the heat, which reduces the temperature at LED junctions. Thermal management materials can either be used beneath LEDs as an interface between the PCB and the outer casing (also sometimes acting as a heat sink), or they can be used to encapsulate up to the LED surface, spreading the heat both above and below the PCB surface. Which method is ultimately chosen will be dependent upon the design of the assembly. Thermal management materials can also be used to encapsulate associated electronic circuits such as LED drivers, again reducing operating temperatures and improving the efficiency of the LED unit as a whole.

What different types and varieties of thermal interface materials are available, and how do I select the most appropriate one for my LED application?

There are many ways to improve upon the thermal management of LEDs. Products range from thermally conductive encapsulation resins, offering both heat dissipation and environmental protection, to thermal interface materials used to improve the efficiency of heat conduction at the LED junction. Such compounds are designed to fill the gap between the device and the heat sink and thus reduce the thermal resistance at the boundary between the two.

The design of an LED array will also dictate an appropriate choice of thermal interface material. For example, if it is a large array, across which temperature fluctuations are likely, it may be beneficial to use a material that is not subject to movement during thermal cycling. A surface-curing thermal paste or one of the latest phase change materials would be ideal choices for these larger LED assemblies.

Other applications may require less localised heat dissipation and therefore a resin that covers the whole surface of the PCB may be more efficient at spreading the heat. An encapsulated PCB is also protected from adverse environmental influences such as mechanical shock or high humidity. And let's not forget thermally conductive bonding materials; for some applications, you might want both adhesive strength and thermal management, in which case a thermally conductive room temperature vulcanizing material would be the appropriate choice.

If I am seeking to dissipate heat away from other power components such as LED drivers, what would be an effective solution?

Encapsulation resins every time! These provide high levels of protection against adverse environmental factors as well as total heat dissipation; they also provide structural stability and flame retardancy.

Does the operating environment impact upon my choice of thermal interface material and what are the key considerations?

Temperature changes, as mentioned before, can be a key factor. Temperature fluctuations can cause the thermal interface material to move, which is clearly undesirable. The gap or distance between LED/PCB and the heat sink also needs to be considered. If it is too large, a non-curing thermal interface material introduced between the LED and its heat sink is more prone to movement.

LED lighting assemblies are in use just about everywhere these days and it is important to consider the ability of the thermal interface material to withstand the conditions under which it operates. For example, high ambient temperatures, poor or damaged waterproofing, condensation, high humidity and so on will all have an impact on its performance. As with any protective compound, you need to understand the operating environment and discuss with chemical suppliers to identify the most suitable materials for your application.

Superior Quality Begins Here.

Since we first began in 1985, delivering the highest quality products possible has been our first priority. Our quality control systems are certified and we renew our commitment to quality each and every day.

Delivering quality products on time, combined with timely and accurate communication from our customer service team is how we create lasting relationships with our customers.

Take a look at our quality »

COMMERCIAL • MILITARY • MEDICAL • BAREBOARD

U.S. Circuit, Incorporated
2071 Wineridge Place
Escondido, CA 92029
+1 (760) 489-1413
www.uscircuit.com

How important is ease of processing with my choice of thermal management material?

The design of your LED lighting unit will determine the type of thermal management material you choose, ensuring that it is correctly applied to the critical areas of the assembly. Processing requirements depend on production capabilities, volumes of manufacture and the prevailing conditions during application. For example, a thermal interface material should be applied in an even film, in as thin a layer as possible.

If it is not possible to apply a thin layer, it might be better to use a pre-cut thermal pad, for example. This will, however, be thicker than a thermal paste or phase change material, which will result in higher thermal resistance. So, in common with all engineering problem-solving exercises, a compromise must be made; in this case, the compromise is between your processing requirements and your expectations of performance in the end application.

Choosing an appropriate solution for your LED application is not exactly straightforward. I strongly recommend you get some expert advice before you settle on any particular material or processing method. Look out for more thermal management tips in my column next month. **PCBDESIGN**

Jade Bridges is the European technical support specialist for Electrolube.

Prototype Shows How Tiny Photodetectors Can Double Their Efficiency

Physicists at the University of California, Riverside have developed a photodetector, a device that senses light, by combining two distinct inorganic materials and producing quantum mechanical processes that could revolutionize the way solar energy is collected.

Photodetectors are almost ubiquitous, found in cameras, cell phones, remote controls, solar cells, and even the panels of space shuttles. Measuring just microns across, these tiny devices convert light into electrons, whose subsequent movement generates an electronic signal. Increasing the efficiency of light-to-electricity conversion has been one of the primary aims in photodetector construction since their invention.

Lab researchers stacked two atomic layers of tungsten diselenide (WSe2) on a single atomic layer of molybdenum diselenide (MoSe2). Such stacking results in properties vastly different from those of the parent layers, allowing for customized electronic engineering at the tiniest possible scale.

Within atoms, electrons live in states that determine their energy level. When electrons move from one state to another, they either acquire or lose energy. Above a certain energy level, electrons can move freely. An electron moving into a lower energy state can transfer enough energy to knock loose another electron.

UC Riverside physicists observed that when a photon strikes the WSe2 layer, it knocks loose an electron, freeing it to conduct through the WSe2. At the junction between WSe2 and MoSe2, the electron drops down into MoSe2. The energy given off then catapults a second electron from the WSe2 into the MoSe2, where both electrons become free to move and generate electricity.

"We are seeing a new phenomenon occurring," said Nathaniel M. Gabor, an assistant professor of physics, who led the research team.

"It's like a wave stuck between walls closing in," Gabor said. "Quantum mechanically, this changes all the scales. The combination of two different ultra-small materials gives rise to an entirely new multiplication process. Two plus two equals five."

iCD Design Integrity

Incorporates the iCD Stackup and PDN Planner software. Offers PCB Designers unprecedented simulation speed, ease of use & accuracy at an affordable price

Dielectric Materials Library
30,700 Rigid & Flex Materials to 100GHz

Termination Planner
Extracts IV Curves from IBIS Models
Calculates Series Terminator of the Distributed System including Loads

iCD Stackup Planner
Field Solver Accuracy, Characteristic Impedance, Edge & Broadside Coupled Differential Impedance

Allegro, Altium, Excel, HyperLynx, OrCAD, PADS, IPC-2581B Interfaces

Extensive Capacitor Library
5,650 Decaps Derived from SPICE Models

Matched Delay Optimization
Relative Signal Layer Propagation
Ideal DDRx Trace Delay Matching

iCD PDN Planner
AC Impedance Analysis & Plane Resonance

Integrated Stackup Planner, VRM Definition, Plane Resonance, Planar Capacitance & EMI to 100GHz

Heads-up Impedance Plots

PDN EMI Plot with EMC limits (FCC, CISPR) to 100GHz

iCD Stackup Planner - Offers Engineers & PCB Designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- Industry Leading 2D (BEM) Field Solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Relative Signal Propagation with 'Matched Delay Optimization'–ideal for DDRx design
- Termination Planner - series termination based on IBIS models & distributed system
- Unique Field Solver computation of multiple differential technologies per signal layer
- Extensive Dielectric Materials Library –over 30,700 rigid & flexible materials up to 100GHz
- Interfaces–Allegro, Altium, Excel, HyperLynx, OrCAD, PADS, Zmetrix TDR, Zuken & IPC-2581B

iCD PDN Planner - Analyze multiple power supplies to maintain low AC impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance and projected EMI
- Definition of plane size, dielectric constant & plane separation
- Extraction of plane data from the integrated iCD Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- PDN EMI Plot with FCC, CISPR & VCCI Limits. Frequency range up to 100GHz
- Extensive Capacitor Library –over 5,650 capacitors derived from SPICE models

"iCD Design Integrity software features a myriad of functionality specifically developed for high-speed design."
- Barry Olney

In-Circuit Design Pty Ltd

www.icd.com.au

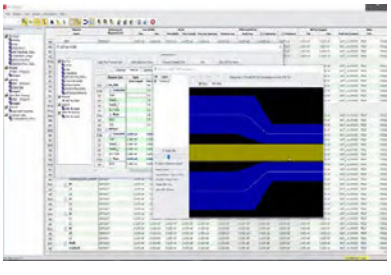
TOP TEN

Recent Highlights from PCBDesign007

1 Predictive Engineering: Happy Holden Discusses True DFM

Happy Holden has been involved in DFM for over 45 years, since he first started working at HP and optimized their PCB design and manufacturing processes. Naturally, for this issue, Barry Matties and Andy Shaughnessy made it a priority to get Happy's thoughts on DFM, and what true DFM entails.

2 New EMA Constraint Manager for OrCAD Brings True Collaboration to the Design Process



Constraint Manager for OrCAD stores constraints in the OrCAD Capture design file, so there is no need to manage constraints and designs. Since some constraints are dependent on layout specifics, Constraint Manager for OrCAD integrates with the Allegro Constraint Manager to share constraint information.

3 The Shaughnessy Report: Mistakes Were Made

We started planning the August issue with a survey sarcastically titled, "Whose fault is that bad board?" We asked a variety of questions regarding how the cause or causes of failure were determined, and what companies do to keep from making the same mistake again. We asked the question "If a board fails in the field, whose fault is it, typically?" Check out some of the answers.

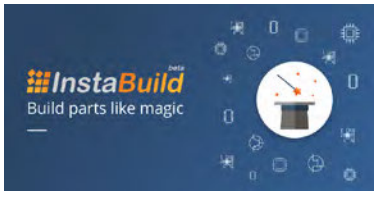
4 New Cadence Allegro DesignTrue DFM Technology Accelerates New Product Development and Introduction Process

Cadence Design Systems announced Cadence Allegro DesignTrue DFM technology, the industry's first solution to perform real-time, in-design DFM checks integrated with electrical, physical and spacing DRCs. The innovative new technology, integrated into the Allegro PCB Editor, enables PCB designers to identify and correct errors immediately, long before manufacturing signoff.

5 True Design Efficiency: Think Before You Click

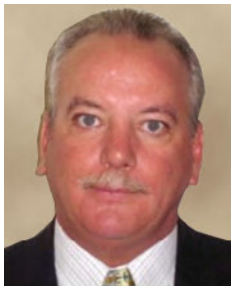
Over the years, I have seen a lot of different circuit board designs. In the service bureaus, I saw many different design technologies, while in companies with captive design departments I saw a lot of different design methodologies. Finally, as a CAD application engineer, I saw both different technologies and different methodologies.

6 SnapEDA Launches Instabuild, a Free Computer Vision-Based Part Builder



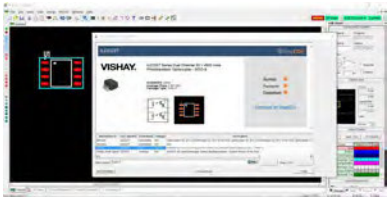
Using a datasheet as the input, InstaBuild automatically extracts symbol pinouts, understands whether a pin is an input, output or power pin, and auto-arranges the symbols based on SnapEDA's published symbol standards.

7 Beyond Design: When Legacy Products No Longer Perform



Faster edge rates mean reflections and signal quality problems. So, even when the package hasn't changed and the clock speed hasn't changed, a problem may exist for legacy designs. The enhancements in driver edge rates have a significant impact on signal quality, timing and crosstalk. This also has a direct impact on radiated emissions.

8 PCB123 Launches Access to Millions of Cloud-Based Symbols & Footprints



Sunstone Circuits has launched a new integration that allows designers to search for digital models directly inside the PCB123 design environment. With the release of PCB123 Version 5.6, designers can now search and download free, cloud-based symbols and footprints directly during design capture and layout.

9 Fault-Finding: It's All About Prevention, not Blame

There are thousands of things that can go wrong during the design and manufacture of a PCB assembly. One might say that it is an absolute miracle when a PCB goes through all of its phases—design, fabrication and assembly—and operates successfully!

10 IPC's CID Programme: Is it Worth the Effort?

IPC's Certified Interconnect Designer (CID) curriculum is the definitive training course for PCB designers and electronic design professionals, but with budgets tightening and time at a premium, is the investment of time, effort and finance worth it? We spoke to three recent delegates to find out their reasons for completing the course.

PCBDesign007.com for the latest circuit design news and information—anywhere, anytime.

Pssst!
Are You Looking for Someone?

Place your notice in our Help Wanted section.

For just $500, your 200 word, full-column—or, for $250, your 100 word, half-column—ad will appear in the Help Wanted section of all three of our monthly magazines, reaching circuit board designers, fabricators, assemblers, OEMs and suppliers.

Potential candidates can click on your ad and submit a résumé directly to the email address you've provided. If you wish to continue beyond the first month, the price is the same per month. No contract required. We even include your logo in the ad, which is great branding!

To get your ad into the next issue, contact:
Barb Hockaday at barb@iconnect007.com or +1.916.608.0660 (-7 GMT)

I-Connect007
GOOD FOR THE INDUSTRY

SMT007 pcb007 pcb design007

SALESPERSON WANTED · MAINLAND SOUTH CHINA

Work where you live!

The I-Connect007 China team is seeking an experienced salesperson to generate and manage a revenue stream for our Chinese publications.

Key Responsibilities include:

- Sell advertising contracts for monthly magazine
- Develop and cultivate new business
- Keep timely and accurate records
- Generate and follow up on all leads
- Manage contract renewals
- Account management: work with local and international team to provide customer support
- Phone and email communications with prospects
- Occasional travel

Qualifications

Successful candidates should possess a university degree or equivalent, experience with managing and cultivating leads, projecting, tracking and reporting revenue. We are looking for positive, high-energy candidates who work well in a self-managed, team-based, virtual environment.

Compensation

This is a base salary-plus-commission position. Compensation commensurate with experience.

Requirements

- Must be located in China Mainland, South China area preferred
- Good command of Chinese language, proficient with English speaking and writing
- Able to follow established systems and learn quickly
- Able to maintain professional external and internal relationships reflecting the company's core values
- 2-5 years' sales experience
- Experience with Microsoft Office products
- Must be highly motivated and target-driven with a proven track record for meeting quotas
- Good prioritizing, time management and organizational skills
- Create and deliver proposals tailored to each prospect's needs
- Experience in the electronics industry desirable

QUALIFIED CANDIDATES: CLICK HERE TO APPLY

I-Connect007
GOOD FOR THE INDUSTRY

pcb007中国 线上杂志 CHINA MAGAZINE

pcb007中国 每周通讯 WEEKLY NEWSLETTER

WWW.ICONNECT007CHINA.COM

MEIKO

Leading PCB Manufacturer Seeks Account Manager

Meiko Electronics, a global leader in PCB interconnect solutions for Tier I and II electronics companies, has expanded its global manufacturing footprint to include two campuses in China and two in Vietnam.

We are looking for a full-time account manager to introduce the company and our outstanding capabilities to new customers, primarily in the automotive space.

Key Responsibilities:

- Work directly with PCB sourcing teams to generate interest in our company
- Manage all customer relations, including scheduling onsite customer meetings with sourcing team decision makers, factory audit and qualification visits resulting in AVL status attainment
- Manage quality/engineering/logistics issues pertaining to key accounts

Qualifications:

- 3 years' professional experience in PCB sales or similar electrical component experience
- Excellent communication and relationship building skills
- Organizational skills, with a strong attention to detail
- Knowledge of Japanese or Mandarin languages a plus

Location:

The ideal candidate will have some initial prospective customers located nearby in the Midwest region and the ability to travel as needed to our Asia-based manufacturing locations.

Competitive compensation and benefits package, including competitive base salary, generous bonus/commission plan, medical/dental/vision and life insurance, matching 401k, PTO.

apply now

American Standard Circuits

Creative Innovations In Flex, Digital & Microwave Circuits

CAM Operator

American Standard Circuits is seeking a candidate to join its team in the position of CAM operator. Applicants will need experience in using Valor/Genesis (GenFlex) CAD/CAM software with printed circuit board process knowledge to edit electronic data in support of customer and production needs. Other requirements include:

- 5+ years of experience in PCB manufacturing
- Process DRC/DFMs and distinguish valid design and manufacturing concerns
- Modify customer supplied data files and interface with customers and engineers
- Release manufacturing tooling to the production floor
- Prepare NC tooling for machine drilling, routing, imaging, soldermask, silkscreen
- Netlist test, optical inspection
- Work with production on needed changes
- Suggest continual improvements for engineering and processing
- Read, write and communicate in English
- Understand prints' specifications
- Must be U.S. citizen or permanent resident (ITAR)
- High school graduate or equivalent

apply now

ventec
INTERNATIONAL GROUP
騰輝電子

Ventec Seeking U.S. Product Manager for tec-speed

Want to work for a globally successful and growing company and help drive that success? As a U.S.-based member of the product and sales team, your focus will be on Ventec's signal integrity materials, tec-speed, one of the most comprehensive range of products in high-speed/low-loss PCB material technology for high reliability and high-speed computing and storage applications. Combining your strong technical PCB manufacturing and design knowledge with commercial acumen, you will offer North American customers (OEMs, buyers, designers, reliability engineers and the people that liaise directly with the PCB manufacturers) advice and solutions for optimum performance, quality and cost.

Skills and abilities required:

- Technical background in PCB manufacturing/ design
- Solid understanding of signal integrity solutions
- Direct sales knowledge and skills
- Excellent oral and written communication skills in English
- Experience in making compelling presentations to small and large audiences
- Proven relationship building skills with partners and virtual teams

This is a fantastic opportunity to become part of a leading brand and team, with excellent benefits.

Please forward your resume to
jpattie@ventec-usa.com and mention
"U.S. Sales Manager—tec-speed"
in the subject line.

www.venteclaminates.com

apply now

ZENTECH

Experienced PCB/ Assembly Professionals Needed

Find a rewarding career and become a successful leader with Zentech Manufacturing. With locations in Baltimore, Maryland, and Fredericksburg, Virginia, Zentech is rapidly growing and seeking experienced professionals in all areas:

- Operations leadership
- Engineering
- Manufacturing engineering
- Program management
- Testing
- Quality assurance

Zentech offers an excellent benefits package, including an employer-matched 401(k) program.

Established in 1998, Zentech holds an ultimate set of certifications relating to the manufacture of mission-critical printed circuit card assemblies, including ISO:9001, AS9100, DD2345, ISO 13485, J-STD 001 with space certification, and is ITAR registered. Zentech was also the first in the U.S. to re-certify for IPC 610 trusted source QML status.

apply now

Altium

Application Engineer

The application engineer is the first contact for our customers who have technical questions or issues with our product. We value our customers and wish to provide them with highest quality of technical support.

Key Responsibilities:

- Support customer base through a variety of mediums
- Log, troubleshoot, and provide overall escalation management and technical solutions
- Create various types of topic based content, such as online help, online user guides, video tutorials, knowledge base articles, quick start guides and more
- Distill complex technical information into actionable knowledge that users can understand and apply
- Continually develop and maintain product knowledge

Requirements:

- Understanding of EDA electronic design software, schematic capture and PCB layout software
- Bachelor's degree in electronics engineering or equivalent experience
- Sales engineering and/or support engineering experience
- Circuit simulation and/or signal integrity experience
- Understanding of ECAD/ MCAD market segments
- Understanding of micro controllers, SoC architecture and embedded systems market
- Database experience preferred (i.e., MySQL, PostgreSQL, Microsoft Access, SQL, Server, FileMaker, Oracle, Sybase, dBASE, Clipper, FoxPro) etc.
- Experience with PLM/PDM/MRP/ERP software (Program Lifecycle Management) preferred
- Salesforce experience a plus

Salary based upon experience. Comprehensive benefits package and 401k plan. Openings in USA, UK, and Germany.

For more information, contact Altium.

apply now

CHEMCUT

BOUNDLESS INNOVATION | UNBEATABLE PRECISION

Field Service Technician

Chemcut, a leading manufacturer of wet-processing equipment for the manufacture of printed circuit boards for more than 60 years, is seeking a high-quality field service technician. This position will require extensive travel, including overseas.

Job responsibilities include:

- Installing and testing Chemcut equipment at the customer's location
- Training customers for proper operation and maintenance
- Providing technical support for problems by diagnosing and repairing mechanical and electrical malfunctions
- Filling out and submitting service call paperwork completely, accurately and in a timely fashion
- Preparing quotes to modify, rebuild, and/or repair Chemcut equipment

Requirements:

- Associates degree or trade school degree, or four years equivalent HVAC/industrial equipment technical experience
- Strong mechanical aptitude and electrical knowledge, along with the ability to troubleshoot PLC control
- Experience with single and three-phase power, low-voltage control circuits and knowledge of AC and DC drives are desirable extra skills

To apply for this position, please apply to Mike Burke, or call 814-272-2800.

apply now

MacDermid
PERFORMANCE SOLUTIONS

Do you have what it takes?

MacDermid Performance Solutions, a Platform Specialty Products Company, and daughter companies manufacture a broad range of specialty chemicals and materials which are used in multi-step technological processes that enhance the products people use every day. Our innovative materials and processes are creating more opportunities and efficiencies for companies across key industries – including electronics, graphic arts, metal & plastic plating, and offshore oil production. Driving sustainable success for companies around the world, and at every step of the supply chain, takes talent. Strategic thinking. Collaboration. Execution.

The people of MacDermid Performance Solutions stand united by a guiding principle: If it doesn't add value, don't do it. This belief inspires a unique culture where each team member has opportunities to imagine, create, hone and optimize. Do you have what it takes? Join our growing team of over 4,000 professionals across more than 50 countries with openings in research, finance, customer service, production and more.

MacDermid Performance Solutions and its affiliates are Equal Opportunity/ Affirmative Action Employers.

apply now

INDIUM®

Technical Content Specialist

Indium Corporation is seeking a technical content specialist to guide the development of data-rich, high-level content for the company's semiconductor and advanced assembly materials (SAAM) sales and technical literature. The technical content specialist will work with multiple departments to ensure that all externally-facing technical and sales collateral and internal training materials are consistent in format and of superior quality.

The technical content specialist will:

- Assist in the development of key content and ensure consistency of message and format across platforms
- Develop a technically-detailed understanding of Indium Corporation materials and offerings to the SAAM industry
- Curate a library of technical conference papers and associated materials, including content related to Indium Corporation materials and their performance
- Assist in the development of, and ensure consistency for SAAM promotional materials, such as product datasheets (PDS), images, brochures, whitepapers and presentations (technical and sales)
- Attend at least one technical conference and its paper session per year

Requirements:

- Technical undergraduate degree (BS in Chemistry/Physics/Metallurgy/Materials Science or Engineering discipline)
- 5 years of work experience in semiconductor assembly or advanced electronics assembly
- Excellent written and spoken English language skills; fluency in Chinese desirable
- Proven ability to work independently with verbal or written instructions

apply now

NCAB GROUP
Integrated PCB Production

Outside Sales/ Key Account Managers

NCAB Group USA is adding to our existing outside sales team in various U.S. locations:

- Ontario, California
- Itasca, Illinois
- Vancouver, Washington

This is a sales position that requires the ability to convert those cold calls into high-value customer meetings. What we are looking for:

- A "hunter" mentality
- The ability to create solid customer relationships
- A desire to excel and not settle for mediocrity
- 5+ years of experience in the PCB or semiconductor industry
- An excellent ability to present a product and do the "deep dive" during customer visits by asking open ended questions and identifying customer pain points
- The energy to move from prospecting to cold calls to getting the win
- Knowledge of "SPIN" selling
- A college degree
- Willingness to travel, domestically and globally
- U.S. citizens with a valid U.S. passport

Interested? Send your resume.

apply now

Visit us at www.NCABGroup.com

ACE
ACCURATE
CIRCUIT
ENGINEERING

PCB Process Planner

Accurate Circuit Engineering (ACE) is an ISO 9001:2000 certified manufacturer of high-quality PCB prototypes and low-volume production for companies who demand the highest quality in the shortest time possible. ACE is seeking a skilled individual to join our team as a PCB process planner.

Responsibilities will include:

- Planning job travelers based on job release, customer purchasing order, drawings and data files and file upon completion
- Contacting customer for any discrepancies found in data during planning and CAM stage
- Consulting with director of engineering regarding technical difficulties raised by particular jobs
- Informing production manager of special material requirements and quick-turn scheduling
- Generating job material requirement slip and verify with shear clerk materials availability
- Maintaining and updating customer revisions of specifications, drawings, etc.
- Acting as point of contact for customer technical inquiries

Candidate should have knowledge of PCB specifications and fabrication techniques. They should also possess good communication and interpersonal skills for interfacing with customers. Math and technical skills are a must as well as the ability to use office equipment including computers, printers, scanners, etc.

This position requires 3 years of experience in PCB planning and a high school level or higher education.

apply now

TECHNICA, U.S.A.
Fulfilling Manufacturing Needs
Throughout the Electronics Industry

Southern California Territory Sales Engineer

Technica, USA, a Western regional manufacturer's representative/distributor, has an open sales position for our Southern California territory. The position will be responsible for selling and servicing our entire product line within the specified territory to the PCB manufacturing industry.

This position requires a highly self-motivated, hands on, confident individual of the highest integrity.

Required Skills:

- BA/BS degree-desired, in a technical area is preferred
- Two years of outside/inside sales or manufacturing experience in the PCB manufacturing environment is desired
- Self-motivated self-starter with the ability to initiate and drive business with little supervision
- Independent worker with a strong commitment to customer satisfaction
- Understanding of consumable sales process
- Ability to organize activities and handle multiple projects simultaneously with effective and timely follow-up
- Ability to solve problems and make decisions for which there are no precedents or guidelines and be resourceful in nature
- Positive attitude while operating under pressure and be an independent problem-solver
- Computer skills in Windows, Outlook, Excel, Word and PowerPoint
- Must have a valid driver's license with good driving record

Please send resume.

apply now

TECHNICA, U.S.A.
Fulfilling Manufacturing Needs
Throughout the Electronics Industry

Western Regional Equipment Service Technician

Technica, USA, a Western regional manufacturer's representative/distributor has an opening for an equipment service technician covering the Western USA, including but not limited to, California, Oregon, Washington, Utah, Colorado, and Arizona. The position will be responsible for servicing our PCB fabrication equipment product line, including installation, troubleshooting, repair service, rebuild service, etc. This position requires a highly self-motivated, hands on, confident individual of the highest integrity.

Key responsibilities are to install and service equipment, conduct equipment audit, and provide technical service when appropriate to solve problems.

Required Skills:

- 2+ years of experience in a PCB manufacturing environment or similar
- Willingness to travel
- Positive "whatever it takes" attitude while operating under pressure
- Self-motivated self-starter with the ability to initiate action plans
- Ability to work independently with a strong commitment to customer satisfaction
- Excellent communication and interpersonal skills
- Strong ability to use all resources available to find solutions
- Computer skills with ability to write detailed service and equipment reports in Word
- Understanding of electrical schematics
- Able to work in and around equipment, chemical, and environmental conditions within a PCB manufacturing facility

Please send resume.

apply now

BLACKFOX
Premier Training & Certification

IPC Master Instructor

This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.

apply now

AD SPACE AVAILABLE NOW

For information, please contact:
BARB HOCKADAY
barb@iconnect007.com
+1 916.365.1727 (-7 GMT)

I·Connect007
GOOD FOR THE INDUSTRY

Prototron Circuits

Experienced PCB Sales Professional

With more than 30 years of experience, Prototron Circuits is an industry leader in the fabrication of high-technology, quick-turn printed circuits boards. Prototron of Redmond, Washington, and Tucson, Arizona are looking for an experienced sales professional to handle their upper Midwest Region. This is a direct position replacing the current salesperson who is retiring after spending ten years with the company establishing this territory.

The right person will be responsible for all sales efforts in this territory including prospecting, lead generation, acquiring new customers, retention, and growth of current customers.

This is an excellent opportunity for the right candidate. Very competitive compensation and benefits package available.

For more information, please contact Russ Adams at 425-823-7000, or email your resume.

apply now

Process Engineer (Redmond, Washington)

With more than 30 years of experience, Prototron Circuits is an industry leader in the fabrication of high-technology, quick-turn printed circuits boards. We are looking for an experienced PCB process engineer to join the team in our Redmond, Washington facility. Our current customer base is made up of forward-thinking companies that are making products that will change the world, and we need the right person to help us make a difference and bring these products to life. If you are passionate about technology and the future and believe you have the skills to fulfill this position, please contact Kirk Williams at 425-823-7000 or email your resume.

apply now

ARLON

Arlon EMD, located in Rancho Cucamonga, California is currently interviewing candidates for **manufacturing** and **management positions.** All interested candidates should contact Arlon's HR department at 909-987-9533 or fax resumes to 866-812-5847.

Arlon is a major manufacturer of specialty high performance laminate and prepreg materials for use in a wide variety of PCB (printed circuit board) applications. Arlon specializes in thermoset resin technology including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, high density interconnect (HDI) and microvia PCBs (i.e., in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001:2008 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customer's requirements.

more details

LENTHOR ENGINEERING
MAKING THINGS FLEXIBLE IN A RIGID WORLD®
311 Turquoise Street Milpitas, CA 95035 (Phone) 408-945-8787

SALES ACCOUNT MANAGER

This is a direct sales position responsible for creating and growing a base of customers. The account manager is in charge of finding and qualifying customers while promoting Lenthor's capabilities to the customer through telephone calls, customer visits and use of electronic communications. Experience with military and medical PWB/PWA a definite plus. Each account manager is responsible for meeting a dollar level of sales per month and is compensated with salary and a sales commission plan.

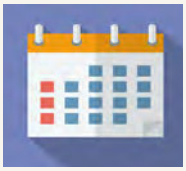
Duties include:

- Marketing research to identify target customers
- Initial customer contact (cold calling)
- Identifying the person(s) responsible for purchasing flexible circuits
- Exploring the customer's needs that fit our capabilities in terms of:
  - Market and product
  - Circuit types used
  - Quantity and delivery requirements
  - Competitive influences
  - Philosophies and finance
  - Quoting and closing orders
  - Bonding
- Submitting quotes and sales orders
- Providing ongoing service to the customer
- Problem solving
- Developing customer information profiles
- Developing long-term customer strategies to increase business
- Participate in quality/production meetings
- Assist in customer quality surveys
- Knowledgeably respond to non-routine or critical conditions and situations

Competitive salaries based on experience, comprehensive health benefits package and 401(k) Plan.

apply now

Events



For IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out The PCB Design Magazine's event calendar.

electronicAsia
October 13–16, 2017
Hong Kong

IPC Flexible Circuits: HDI Forum
October 17–19, 2017
Minneapolis, Minnesota, USA

TPCA Show 2017
October 25–27, 2017
Taipei, Taiwan

productronica 2017
(IPC Committee meetings held in conjunction with productronica)
November 14–17, 2017
Munich, Germany

HKPCA/IPC International Printed Circuit & South China Fair
December 6–8, 2017
Shenzhen, China

47th NEPCON JAPAN
January 17–19, 2018
Tokyo Big Sight, Japan

DesignCon 2017
January 30–February 1, 2018
Santa Clara, California, USA

EIPC 2018 Winter Conference
February 1–2, 2018
Lyon, France

IPC APEX EXPO 2018 Conference and Exhibition
February 27–March 1, 2018
San Diego, California, USA

China International PCB and Assembly Show (CPCA)
March 20–22, 2018
Shanghai, China

KPCA Show 2018
April 24–26, 2018
Kintex, South Korea

Medical Electronics Symposium 2018
May 16–18, 2018
Dallas, Texas, USA

PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

SALES MANAGER: **BARB HOCKADAY**
(916) 608-0660; barb@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**
(916) 266-9160; tobey@iconnect007.com

EDITORIAL:

MANAGING EDITOR: **ANDY SHAUGHNESSY**
(404) 806-0508; andy@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

MAGAZINE PRODUCTION CREW:

PRODUCTION MANAGER: **SHELLY STEIN**

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **SHELLY STEIN, MIKE RADOGNA, TOBEY MARSICOVETERE**

INNOVATIVE TECHNOLOGY: **BRYSON MATTIES**

COVER: **SHELLY STEIN**

COVER IMAGE: © **JRSALIDO218, ADOBE STOCK**

THE pcb design MAGAZINE

The PCB Design Magazine® is published by BR Publishing, Inc., PO Box 50, Seaside, OR 97138
©2017 BR Publishing, Inc. does not assume and hereby disclaims any liability to any person for loss or damage caused by errors or omissions in the material contained within this publication, regardless of whether such errors or omissions are caused accidentally, from negligence or any other cause
October 2017, Volume 6, Number 10 • The PCB Design Magazine© is published monthly by BR Publishing, Inc.

ADVERTISER INDEX

Accurate Circuit Engineering..... 27
Altium..... 55
American Standard Circuits..... 51
Candor Industries..... 21
Coast to Coast Circuits, Inc..... 45
Downstream Technologies..... 9, 41
Eagle Electronics..... 11
Electrolube..... 59
EMA Design Automation.....13
General Circuits..... 63
I-Connect007 eBooks..... 2, 3, 17
In-Circuit Design Pty Ltd..... 73
IPC..... 65
IPC-2581 Consortium..... 43
Isola..... 5
Mentor, a Siemens Business..... 31
Miraco..... 7
NCAB..... 57
Prototron Circuits..... 67
Rogers Corporation..... 69
Sunstone Circuits..... 37
US Circuit..... 71
Ventec International Group..... 47

I-Connect007

GOOD FOR THE INDUSTRY

FREE SUBSCRIPTION

my I-Connect007

myiconnect007.com

007 Media Kit

mediakit.iconnect007.com

EDITORIAL CONTACT

Andy Shaughnessy
andy@iconnect007.com
+1 404.806.0508 GMT-5

SALES CONTACT

Barb Hockaday
barb@iconnect007.com
+1 916 365-1727 GMT-7

pcb design 007 | pcb 007 | SMT 007 | mil aero 007 | flex 007 | ein 007 | RTW

www.iconnect007.com